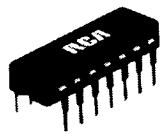

14-Lead Dual-in-Line Plastic Package

H-1517

RC Phase-Lock-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- *Low distortion [THD]: 0.3% typ.*
- *Excellent SCA [storecast] rejection: 75 dB typ.*
- *RC oscillator*
- *High audio channel separation: 40 dB*
- *Operates from a wide range of power supplies: 8 to 16 V dc*
- *Requires only one adjustment for complete alignment*
- *Drives a stereo indicator lamp up to 75 mA - surge current limiting*
- *Stereo separation maintained with 8-volt supply voltages*

RCA-CA1310A is a monolithic silicon integrated circuit RC phase-lock-loop stereo decoder intended for FM solid-state stereo multiplex systems. It is a direct replacement for industry types MC1310P, LM1310, and SN76115N.

This decoder uses a minimum of external components. In addition the stereo decoder requires only one adjustment (oscillator frequency) for complete alignment.

The CA1310A is unilaterally interchangeable with the CA1310 and offers improved and controlled distortion characteristics. A maximum limit of 1% is guaranteed over the V_{cc} range of 8 to 16 volts under any conditions of modulation (L = R, L = -R, L = 1, R = O, or L = 0, R = 1). The local oscillator stability has also been improved so that stereo separation is maintained with supply voltages as low as 8 volts.

The CA1310A is supplied in a 14-lead dual-in-line plastic package and operates over an ambient temperature range of -40 to +85° C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE	16 V
CURRENT (LAMP) AT TERM. 6	75 mA
DEVICE DISSIPATION:	
Up to T_A = 25° C	625 mW
Above T_A - 25° C derate linearly	5 mW/° C
AMBIENT TEMPERATURE RANGE:	
Operating	-40 to +85° C
Storage	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max	+265° C

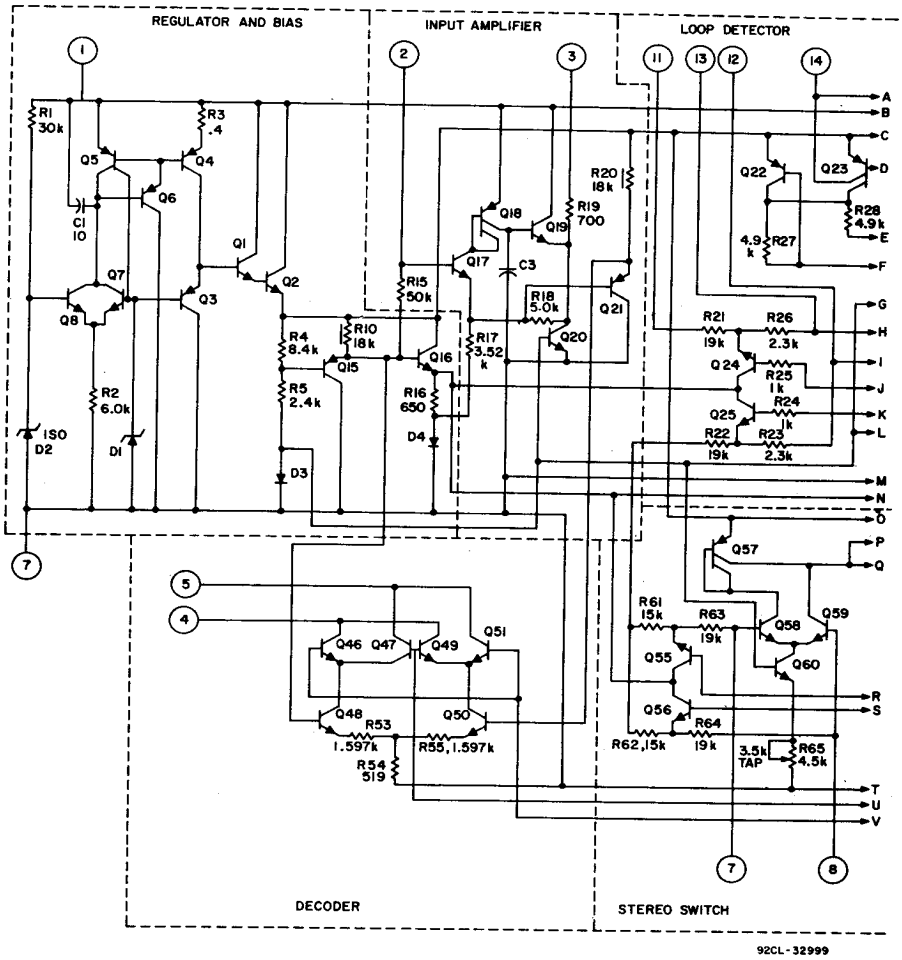

Fig. 1— Schematic diagram of the CA1310A.

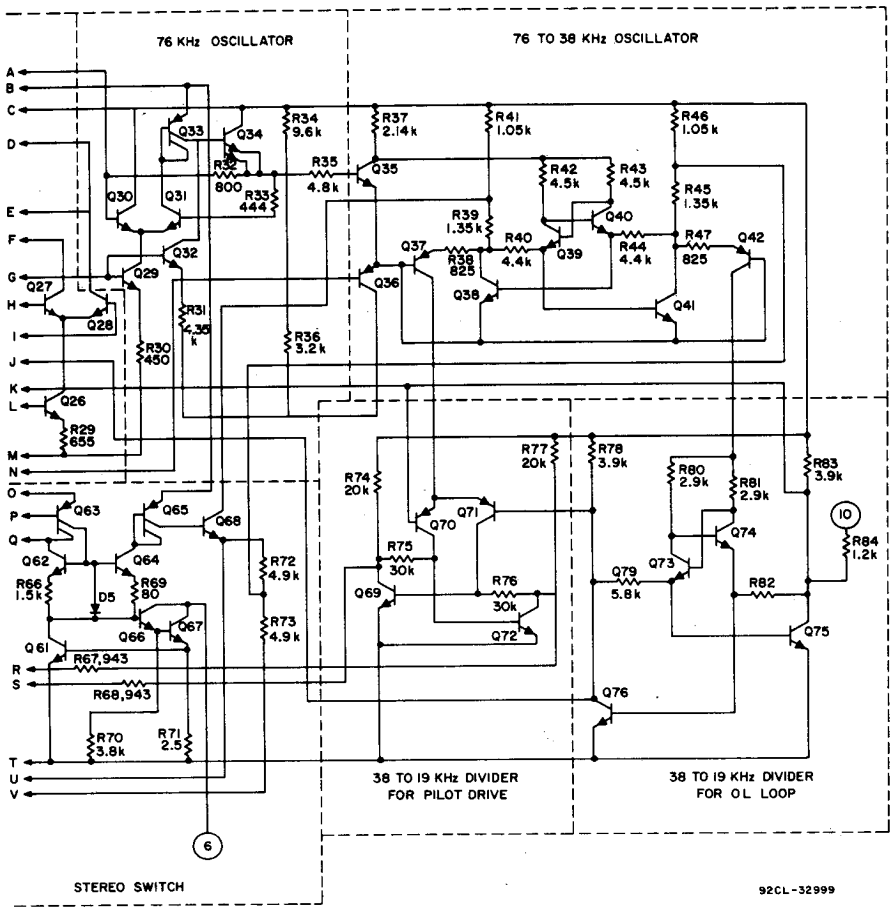

Fig. 2—Schematic diagram of the CA1310A (cont'd).

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3) V+ = 12 V, T_A = 25 °C, Composite Multiplex Input Signal 2.8 V p-p.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics					
DC Supply Voltage	For 8-V operation, reduce load to 2.7 kΩ	8	—	16	V
Total Current	Lamp "OFF"	—	13	—	mA
Dynamic Characteristics					
Input Impedance		20	50	—	kΩ
Channel Separation (Stereo)	50 Hz — 15 kHz	30	40	—	dB
Audio Output Voltage (For any one channel)		—	485	—	mV RMS
Channel Balance (Monaural)	Pilot Tone "OFF"	—	—	1.5	dB
Capture Range (Permissible tuning error of internal oscillator		—	± 3.5	—	%
Total Harmonic Distortion		—	0.3	1.0	%
Ultrasonic Frequency Rejection: 19 kHz		—	34.4	—	dB
38 kHz		—	45	—	dB
SCA (Storecast) Rejection	f = 67 kHz, 9-kHz beat note measured with 1-kHz modulation "OFF"	—	75	—	dB
Stereo Switch Level: 19-kHz Input Level (For lamp on)		—	—	20	mV RMS
19-kHz Input Level (For lamp off)		5	—	—	mV RMS

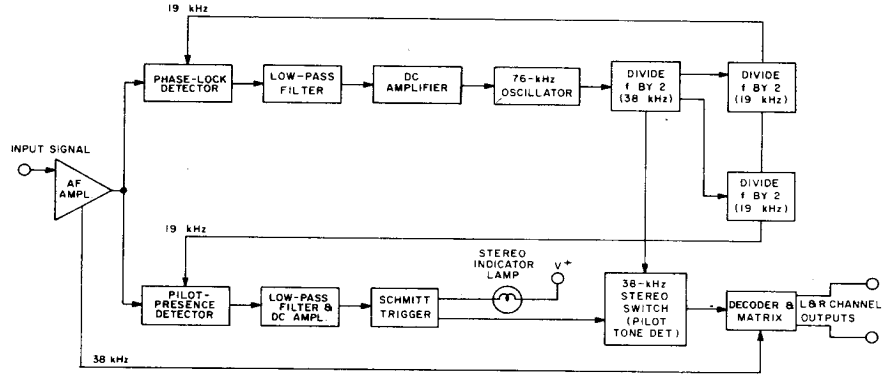

Fig. 2— Functional block diagram of the CA1310A system.

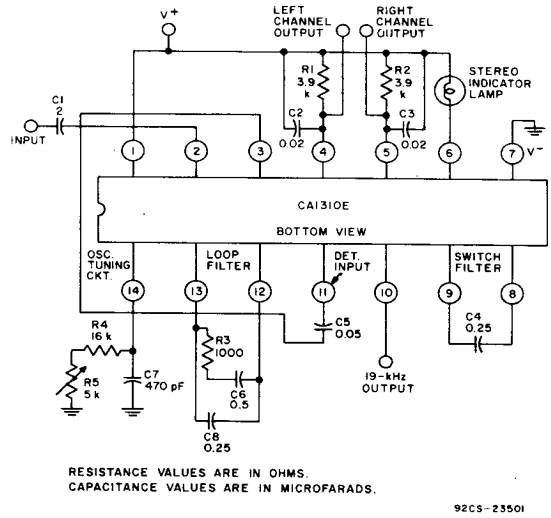

Fig. 3—Test circuit for measurement of dynamic characteristics.

NOTES *for test circuit of Fig. 3.*

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower-value input coupling capacitor may be used in place of the 2-μF value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo-switch level-detector circuit is calculated by C4 × 53,000 ohms ±30% with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot-level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05-μF capacitor provides a 1.75° phase lead at 19 kHz.

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25 μF, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than ±3% typ. is required, reduce value of C7 and increase values of R4 and R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. The tolerances of R4 and C7 are ±1% in the test circuit and ±5% in typical application circuits.

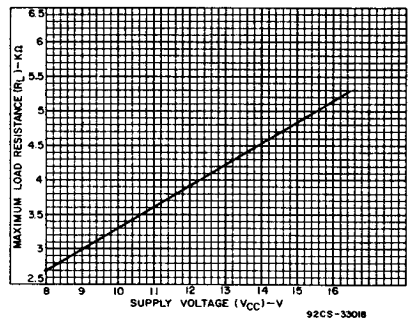

Fig. 4—Maximum load resistance vs. supply voltage.