RCA Solid State

RCA Solid State

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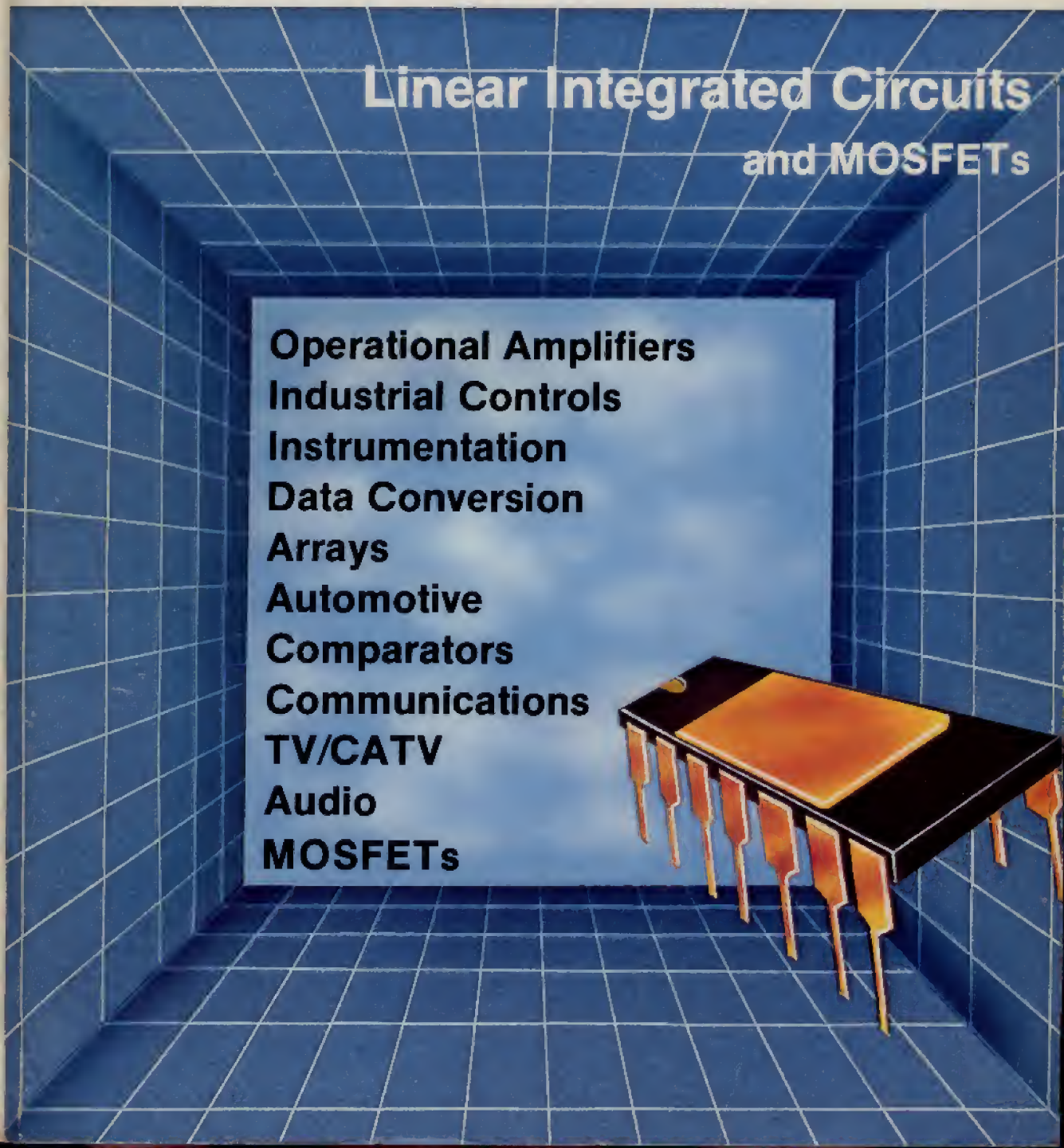
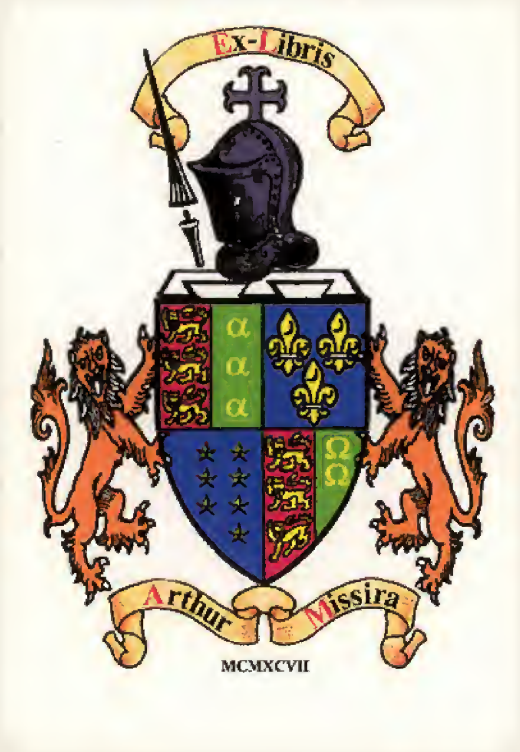
APPLICATIONS



Linear Integrated Circuits and MOSFETs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Linear Integrated Circuits and MOSFETs—Applications

RCA offers a broad line of linear integrated circuits and discrete small-signal MOS field-effect transistors (MOSFETs) for a broad variety of diverse applications in industrial, military, and consumer applications. This book contains a selection of application notes that provide helpful user information on many popular types currently available from RCA Solid State Division as standard products. The products covered include operational amplifiers, power-control circuits, arrays, differential amplifiers, circuits for television, AM and FM radio, and audio system, data-conversion and special-function circuits, and MOSFETs.

The application notes are included in this book in the alpha-numeric sequence of the RCA identification number. A classification chart provides a complete listing of these notes in two ways for easy reference. The first listing groups the notes into specific categories according to product and circuit function. The second listing is by device type and, in essence, is a cross reference of specific devices to relevant application notes.

Detailed ratings and characteristics data on the devices covered in the application notes are provided in the **RCA Linear Integrated Circuits and MOSFETs** DATABOOK, SSD-240B, and in the technical data bulletin on each specific device. Other technical publications on these devices, such as product selection guides and special-emphasis catalogs and brochures, are listed at the end of this book.

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When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

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Table of Contents

Application Note Classification Chart

Application Notes

Application Notes (Cont'd)

Application Note Classification Chart
By Category

Operational Amplifiers

ICAN-6048	Some Applications of a Programmable Power Switch/Amplifier IC
ICAN-6077	An IC Operational-Transconductance Amplifier (OTA) with Power Capability
ICAN-6386	Understanding and Using the CA3130, CA3130A, and CA3130B BiMOS Operational Amplifiers
ICAN-6459	Why Use the CMOS Operational Amplifier—And How To Use It
ICAN-6668	Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers
ICAN-6669	FET-Bipolar Monolithic Op Amps Mate Directly to Sensitive Sources (CA3140, CA3240)
ICAN-6732	Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits
ICAN-6818	Dual Variable Op-Amp IC, the CA3280, Simplifies Complex Analog Designs
ICAN-6933	Application of the CA080 BiMOS Op-Amp Series in Low-Cost Instruments and Audio Circuits

Power Control Circuits

ICAN-6048	Some Applications of a Programmable Power Switch/Amplifier IC
ICAN-6157	Applications of the CA3085 Series Monolithic IC Voltage Regulators
ICAN-6182	Features and Applications of RCA IC Zero-Voltage Switches (CA3058, CA3059, CA3079)
ICAN-6915	Application of the CA1524-Series Pulse Width Modulator IC's
ICAN-7174	The RCA CA1524E Pulse-Width Modulator-Driver for an Electronic Scale

Integrated-Circuit Arrays

AN-4590	Using MOSFET IC's in Linear Circuit Applications
ICAN-4072	Application of the RCA CA3048 Integrated-Circuit Amplifier Array
ICAN-5296	Application of the RCA CA3018 Integrated-Circuit Transistor Array
ICAN-5299	Application of the RCA CA3019 Integrated-Circuit Diode Array

Broadband Video Amplifiers and Differential Amplifiers

ICAN-5337	Application of the RCA CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges
ICAN-5766	Application of the RCA CA3020 and CA3020A Integrated-Circuit Multi-Purpose Wideband Power Amplifiers

TV, FM, AM, and Audio Circuits

ICAN-5269	IC's for FM Broadcast Receivers
ICAN-5380	IC FM Intermediate-Frequency Amplifiers
ICAN-6077	An IC Operational-Transconductance Amplifier (OTA) with Power Capability
ICAN-6247	Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques
ICAN-6257	Application of the CA3089E FM-IF Subsystem
ICAN-6259	Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Decoder
ICAN-6302	Description and Application of the RCA CA3120E Integrated-Circuit TV-Signal Processor
ICAN-6303	A Single IC for the Complete PIX-IF Subsystem in TV Receivers
ICAN-6472	A Chrominance Demodulator IC with Dynamic Flesh Correction (CA3126, CA3137)
ICAN-6718	Application of the CA3143 and CA3144 TV Luminance Processors
ICAN-6728	Application of the CA3134 Sound IF and Output Sybsystem in TV Receivers
ICAN-6802	A High-Stability Sync-AGC and Horizontal-Vertical Countdown System for 525-Line Color-TV Receiver Applications using RCA CA3154 and CA3157 IC's
ICAN-7164	RCA CA3210 Horizontal, Vertical and Regulator Control Integrated Circuit
ICAN-7169	VideoDisc's Video and Audio Demodulation, Defect Detection and Squelch Control (CA3215)
ICAN-7173	A New Low Level Luminance Processing System (CA3143, CA3144)
ICAN-7175	Integrated NTSC Chrominance/Luminance Processor (CA3217)

Data Conversion Circuits

ICAN-6956	CMOS/SOS Flash A/D Converter, the CA3300, Operates at Video Speed on Low Power

Special-Function Circuits

ICAN-6823	CA3164E BiMOS Control Chip Extends Battery Life in Camera's Photoflash Circuit

MOSFETs

AN-3193	Application Considerations for the RCA 3N128 VHF MOS Field-Effect Transistor
AN-3452	Chopper Circuits Using RCA MOS Field-Effect Transistors
AN-3535	An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer
AN-4018	Design of Gate-protected MOS Field-Effect Transistors
AN-4125	MOSFET Biasing Techniques
AN-4431	RF Applications of the Dual-Gate MOSFET up to 500 MHz
AN-4590	Using MOSFET IC's in Linear Circuit Applications

Application Note Classification Chart

By Device Type

Linear IC's

Type	Application Note
CA080-83	ICAN-6933
CA1524	ICAN-7174, ICAN-6915
CA3012	ICAN-5269, ICAN-5380
CA3014	ICAN-5269
CA3018	ICAN-5296
CA3019	ICAN-5299
CA3020	ICAN-5766
CA3028	ICAN-5337, ICAN-5380
CA3048	ICAN-4072
CA3058	ICAN-6182
CA3059	ICAN-6182
CA3068	ICAN-6303
CA3079	ICAN-6182
CA3080	ICAN-6077, ICAN-6668
CA3085	ICAN-6157
CA3089	ICAN-6257
CA3090	ICAN-6259
CA3094	ICAN-6048, ICAN-6077
CA3120	ICAN-6302
CA3126	ICAN-6247, ICAN-6472
CA3130	ICAN-6386, ICAN-6459
CA3134	ICAN-6728
CA3137	ICAN-6472
CA3140	ICAN-6669
CA3143	ICAN-6718, ICAN-7173
CA3144	ICAN-6718, ICAN-7173
CA3154	ICAN-6802
CA3157	ICAN-6802
CA3164	ICAN-6823
CA3210	ICAN-7164
CA3215	ICAN-7169
CA3217	ICAN-7175
CA3240	ICAN-6669
CA3280	ICAN-6818
CA3300	ICAN-6956
CA6741	ICAN-6732

MOSFETs

Type	Application Note
3N128	AN-3193
3N138	AN-3452
3N187	AN-4018
3N200	AN-4431
40468	AN-3535
40559	AN-3535
40819	AN-4018
40673	AN-4018
40820	AN-4018
40821	AN-4018
40822	AN-4018
40823	AN-4018

Application Notes

1CE-402

Operating Considerations for RCA Solid State Devices

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

> Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Similarly, the TO-5 style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operatings to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors: see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operating could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT and VERSATAB in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or

bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. When the use of a properly designed fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT and TO-202 VERSATAB in-line packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 235 °C and must be applied for not more than 10 seconds at a distance not less than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardware for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp.

Socket No. PTD-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-suppied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

Cleaning After Mounting

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specific time. From a reliability standpoint, however, it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term transistor life of all cleaning solvents, which are marketed under a variety of brand names with numerous additives. These solvents can, however, be classified with respect to their component parts, as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the package. Alcohols are acceptable solvents and are recommended for flux removal whenever possible. Examples of suitable alcohols are methanol, isopropanol, and special denatured ethyl alcohols, such as SDA1, SDA30, SDA34, and SDA44.

When considerations such as solvent flammability are of concern, selected freon-alcohol blends are usable when exposure is limited. Solvent such as the following should be safe for normal flux-removal operations, but care should be taken to assure their suitability in the cleaning procedure:

Freon TE
Freon TE-35
Freon TP-35 (Freon PC)

The solvents may be used for a maximum of 4 hours at 25 °C or for a maximum of 1 hour at 50 °C.

Care must also be used in the selection of fluxes in the soldering of leads. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

Alpha Reliaros No. 320-33
Alpha Reliaros No. 346
Alpha Reliaros No. 711
Alpha Reliafoam No. 807
Alpha Reliafoam No. 809
Alpha Reliafoam No. 811-13
Alpha Reliafoam No. 815-35
Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and physical standpoint.

Note:
Silicon-oil fluids that come into direct physical contact with the molded-plastic packages may react chemically with and cause damage to the packages. Such fluids, therefore, are unacceptable as baths for degreasing and flux removal. Silicone oils contained in thermal compounds or other materials used in mounting the molded-plastic packages, however, do not cause damage to the packages provided the bleed rate of such materials is not excessive. For example, in mounting arrangements that employ an insulating washer, a thermal-grease heat-sink compound, such as Dow Corning No. 340 or equivalent, for which the bleed rate does not exceed 0.5 per cent after 24 hours or 200°C is recommended for use on both sides of the insulating washer.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

*Trade Name: Emerson and Cumming, Inc.

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS/FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS/FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS/FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent. (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

RF POWER TRANSISTORS

Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled

away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

Operating

Forward-Biased Operation. For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropiate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

Load VSWR. Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transistor Manual, Technical Series RFM-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

INTEGRATED CIRCUITS

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar■ leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

COS/MOS INTEGRATED CIRCUITS

Handling

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current

■Trade Name: Westinghouse Corp.

*Mil-M-38510A, paragraph 3.5.6.1(a), lead material

type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handing considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated circuits".

LINEAR INTEGRATED CIRCUITS

In linear integrated circuits that employ diode isolation techniques, there are numerous parasitic devices associated with the primary circuit components. These devices may be activated or turned on by driving inputs and/or outputs beyond the supply-voltage range of the integrated circuit. For example, externally driving the collector terminal of a transistor array below the isolation potential or substrate will forward bias the parasitic isolation diode shown in Fig. 1. Since the

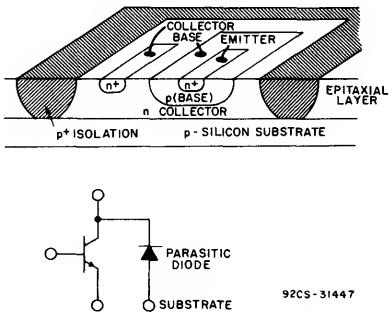


Fig. 1—Sectional view of conventional "vertical" n-p-n transistor commonly used on IC chip. Also shown is the equivalent circuit and associated parasitic diode.

collector region and substrate form a comparatively large-area diode, high currents will be sustained, often at levels sufficiently high to melt the metalization to these devices.

Operational amplifiers like the 741 and other similar structures can be damaged by driving a positive-going signal into the input device with power off. The signal will forward bias the collector-to-base junction of the input transistor and, if the positive supply impedance is low enough, drive curent back into the supply. Current above the maximum rating may result in damage to the amplifier.

Supply transients are another possible source of damage. They can activate or trigger parasitic SCR devices which can cause an integrated circuit to draw extremely high current. If the supply impedance is sufficiently high, the SCR gate drive in the latched condition is removed by the limiting action of the supply. If the supply impedance is too low, the device will continue to demand high currents until the metalization of either the device or the pc board fuses open.

Although device manufactuers take precautions to keep the number of these parasitic devices at a minimum, normal device process variations occasionally make the formation of parasitic devices inevitable. It is essential, therefore, that the user take precautions to insure that an integrated circuit is never operated beyond its maximum ratings, even under momentary transient conditions.

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40 °C
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the realtively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

AN-3193

Application Considerations for the RCA 3N128 VHF MOS Field-Effect Transistor

by

F. M. Carlson

Early MOS field-effect transistors were intended primarily for low-frequency applications in which their extremely high input impedance is advantageous,* and were not designed to be useful in the vhf range (30 to 300 MHz). Recently, however, RCA has developed high-frequency MOS transistors that exhibit high gain and low noise at vhf, together with very low feedback capacitance and cross-modulation distortion that approaches the low levels of electron tubes. The low level of cross-modulation distortion is a particularly important characteristic in view of the increasing congestion of the communications frequency bands.

This note describes applications and vhf circuit considerations for a new high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

Biasing Requirements and Circuit Configurations

The biasing requirements and operating characteristics of an n-channel MOS transistor such as the 3N128 are similar to those of an electron tube. For example, the 3N128 uses positive drain voltages and usually negative gate voltages which are analogous to the plate and grid voltages, respectively, of electron tubes. In addition, the current-voltage characteristics of the 3N128, shown in Fig. 1, are similar to those of a pentode tube. An electron-tube analogy, therefore, can be useful in the analysis of the n-channel 3N128 MOS transistor.†

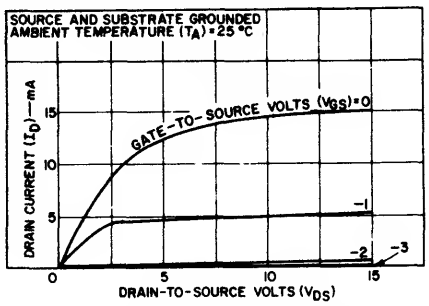


Fig. 1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.

Although their characteristics are similar, MOS transistors have several important advantages over electron tubes. They can be operated at the low voltages typical of bipolar transistors. The dc gate current of MOS transistors is substantially less than the

* The basic theory of MOS transistors and equivalent circuits for these devices are discussed in RCA Application Note AN-201, "Application Considerations for RCA 3N98 and 3N99 Silicon MOS Transistors," by D. M. Griswold.

† The electron-tube analogy does not apply to p-channel MOS transistors or to enhancement types.

grid current of most electron tubes. In addition, the MOS transistor requires no heat-generating filament.

MOS transistors are most often used in the common-source type of circuit configuration. Fig.2 shows three basic methods of dc-biasing an MOS transistor in a common-source circuit. MOS transistors may also be used in common-gate or common-drain (source-follower) configurations.[2] These circuits are not widely used in vhf applications, however, because their gain is low at high frequencies.

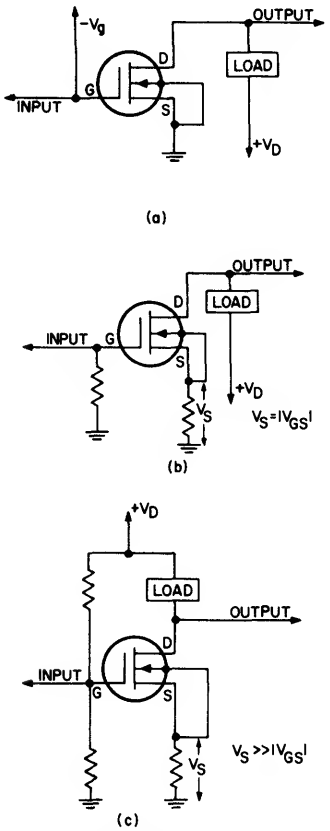
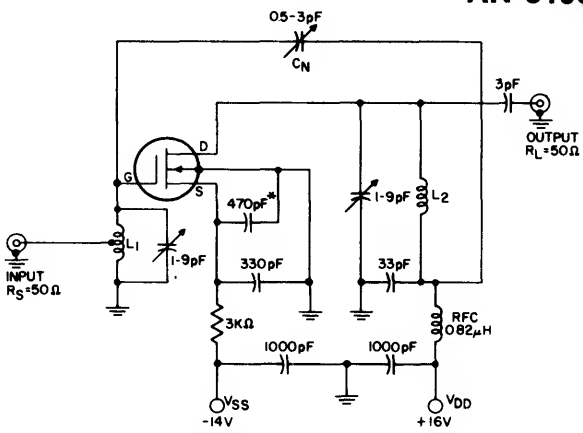


Fig.2 - Bias methods for common-source MOS transistor stages: (a) fixed bias; (b) source-resistor bias; (c) constant-current bias.

Fig.3 shows a 200-MHz common-source amplifier used to measure the rf power gain of the MOS transistor. This amplifier uses a modified form of the constant-current biasing arrangement shown in Fig.2(c). With this modified biasing arrangement, both the insulated gate and the case of the MOS transistor are operated at dc ground potential. The insulated gate should always have a dc path to ground even if the path is through a multimegohm resistor. If the gate is allowed to float, the resultant dc bias conditions may be unpredictable and possibly harmful.



L_1 = 4-1/2 turns of No.20 wire, 3/16 inch in dia., 1/2 inch long, tapped at 1 turn

L_2 = 3-1/2 turns of No.20 wire, 3/8 inch in dia., 1/2 inch long

* Leadless disc capacitor

Fig.3 - 200-MHz common-source amplifier.

Fig.4 illustrates the effect of the leakage resistances R_{L1} and R_{L2} when the insulated gate is floating. When these resistances ($\approx 10^{14}$ ohms) are approximately equal, they form a voltage divider which biases the insulated gate at $+V_{DD}/2$. This value of bias voltage may exceed the maximum rating for positive gate voltage and, in addition, may cause an excessive flow of drain current.

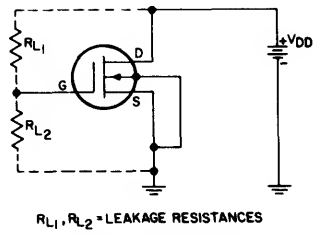


Fig.4 - Bias conditions for an MOS transistor when the insulated gate is floating.

The cascode configuration represents a useful variation of common-source circuit. In this configuration, a common-source-connected MOS transistor is used in the lower section of the cascode, and a common-gate-connected MOS transistor is used in the upper section. Fig.5 shows the use of MOS transistors in a 200-MHz cascode amplifier. This circuit normally requires a negative voltage on the gate of Q_1, a positive voltage on the gate of Q_2, and approximately equal drain-to-source voltages for each transistor. Although the gate of Q_2 may require a positive voltage of 5 to 10 volts, the net gate-to-source voltage for this transistor should be approximately 0 to -1 volt.

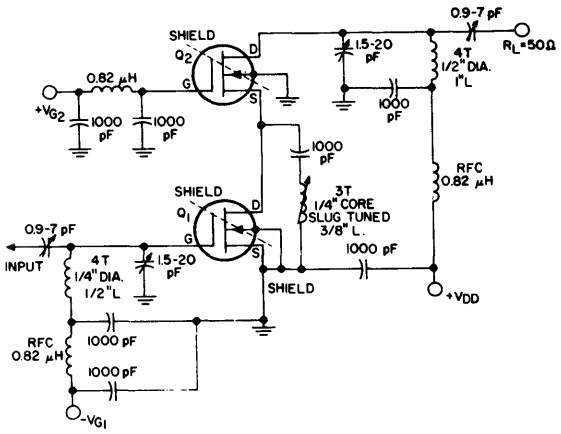


Fig.5 - 200-MHz cascode amplifier.

Selection of Operating Point

The operating point selected determines the power gain, noise figure, power dissipation, and, where applicable, battery life. In many applications, a compromise between gain and available supply voltages or battery lifetime is necessary. Knowledge of the variation in gain and noise figure as functions of voltage and current is essential, therefore, before an operating point can be selected.

The 3N128 provides maximum rf power gain at a drain-to-source voltage V_{DS} of approximately 20 volts and a drain current I_D of about 5 milliamperes. The transistor also exhibits a minimum noise figure at a V_{DS} of 20 volts for a drain current of about 2 milliamperes. The difference in the noise figures obtained at 2 milliamperes and at 5 milliamperes, however, is very small (usually between 0 and 0.2 dB) and generally is not a significant factor in the selection of the operating point. Although a V_{DS} of 20 volts represents the optimum value for the 3N128 in terms of both rf power gain and noise figure, this value is also the maximum V_{DS} rating for the transistor. Greater long-term reliability is achieved, therefore, by operation of the 3N128 at a V_{DS} of 12 to 15 volts rather than at 20 volts.

For a V_{DS} of 15 volts and an I_D of 5 milliamperes, the 3N128 typically provides a power gain of 18 dB and a noise figure of 4 dB at 200 MHz. Operation of the 3N128 at considerably lower drain currents, such as those normally employed in battery-powered equipment, does not seriously affect system performance. For example, when the transistor is operated at a V_{DS} of 15 volts and an I_D of only 1 milliampere, the power gain and noise figure at 200 MHz are typically 15.5 dB and 4.5 dB, respectively. Because the MOS transistor is a voltage-controlled device, its performance for a given power dissipation can often be improved by operation at high voltage and low current levels. At a power dissipation of 30 milliwatts, for example, the 3N128 typically provides a power gain of 17.3 dB and a noise figure of 3.9 dB when operated at 15 volts and 2 milliamperes. At the same dissipation level, however, the power gain is reduced to 14.6 dB and the noise figure is increased to 4.7 dB when the 3N128 is operated at 6 volts and 5 milliamperes. Fig.6 shows the variations in power gain and noise figure of the 3N128 as functions of the drain current and voltage.

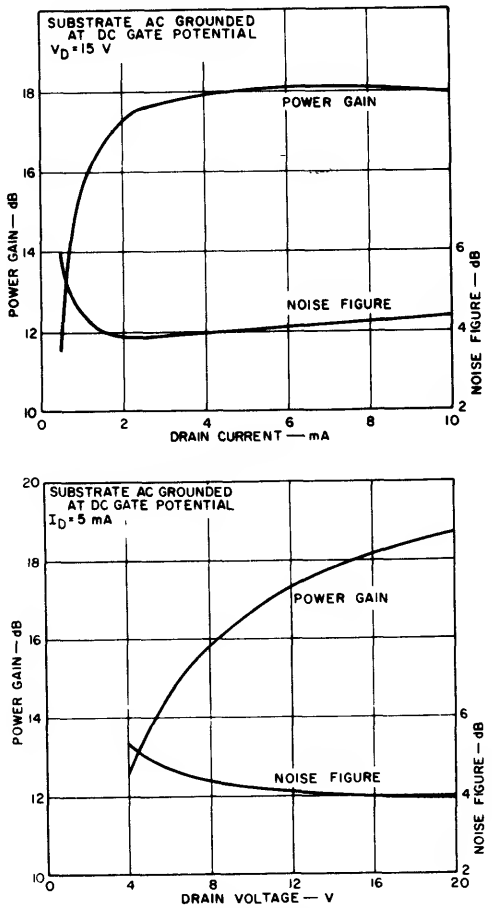


Fig.6 - Power gain and noise figure of the RCA 3N128 at 200 MHz as functions of drain current and voltage.

A gate voltage V_G of between -0.5 and -2 volts is normally required to bias a 3N128 for operation at a drain voltage V_D of 15 volts and a drain current I_D of 5 milliamperes. If a fixed-bias circuit, as shown in Fig.2(a), is used, the value of the gate voltage must be adjustable to compensate for variations among individual transistors. For the source-resistance bias circuit shown in Fig.2(b) the value of the biasing resistor should be 200 ohms (5 mA x 200 ohms = 1 volt). The source-resistance circuit will limit the variations in current among the different transistors to approximately

50 per cent. With the constant-current bias circuit shown in Fig.2(c), variations in current from one transistor to another can easily be limited to less than 10 per cent. Regardless of the bias circuit or the bias point selected, there is no danger of thermal runaway with the 3N128 because this transistor has a negative temperature coefficient at the zero-gate-bias point. In the selection of the bias circuit for an MOS transistor stage in which automatic gain control is employed, consideration should be given to the following principle: The more restrictive the tolerance imposed on quiescent operating-point current, the more difficult automatic gain control of the stage becomes because the self-compensating action of the constant-current bias circuit also resists current changes that result from the agc action.

AGC Methods

When it is necessary to employ agc in an MOS transistor stage, either of two methods may be used to reduce transistor gain. In one method, referred to as reverse agc, the reduction in gain is accomplished by an increase in negative gate bias. In the other method, the gain is decreased by reduction of the drain-to-source voltage.

In the reverse agc method, the application of higher negative voltage to the gate reduces the drain current and the transconductance of the transistor. The low feedthrough capacitance of the 3N128 (typically about 0.13 picofarad) usually permits more than 30 dB of gain reduction at frequencies up to 200 MHz. Substantially greater gain reduction can be achieved at lower frequencies or in neutralized amplifier circuits.

Gain reduction achieved by the decrease of drain-to-source voltage is usually controlled by a variable impedance in series, or in shunt, with the MOS transistor. The variable impedance may be another MOS transistor or a bipolar transistor. A major disadvantage of this method is that the MOS feedback capacitance rises by a factor of 4 or 6 times as V_D approaches zero. This increase in capacitance reduces the agc range obtainable and decreases the effectiveness of a fixed neutralization network. In addition, the output impedance of the 3N128 decreases with a reduction in the drain voltage.

In the cascode circuit, agc is accomplished most effectively by application of a negative voltage to the gate of the upper (common-gate) section. A wide agc range can be obtained in this circuit. Gain reductions greater than 45 dB at 200 MHz or 65 dB at 60 MHz are realizable in an unneutralized cascode circuit.

RF Considerations

One of the prime advantages of the 3N128 MOS transistor over bipolar transistors is its superior cross-modulation, intermodulation, and modulation distortion performance. The 3N128 has considerably lower feedback capacitance than junction-gate field-effect transistors. In addition, the 3N128 maintains a high input resistance at frequencies well into the vhf range (the real part of the input admittance, $Re(y_{11}) = 0.15$ mmho at 100 MHz).

At maximum gain, the cross-modulation distortion of the 3N128 is approximately one-tenth that of most bipolar transistors, or roughly comparable to the cross-modulation performance of vacuum tubes (at 200 MHz, an interfering signal of approximately 80 millivolts is required to produce cross-modulation distortion of 1 per cent). However, cross-modulation susceptibility changes as the gain of the stage is changed. For a single 3N128, the cross-modulation distortion increases when reverse agc is applied; the distortion is also increased, but to a lesser extent, if agc action is achieved by reduction of the drain-to-source voltage. A deterioration in cross-modulation performance at high attenuation results from the fact that the MOS triode is a sharp-cutoff device; as a result, large non-linearities occur near "pinch-off." Beyond "pinch-off," the transadmittance depends primarily upon the capacitive feedthrough, which does not have large third-order non-linearities. Cross-modulation performance at the extreme limits of attenuation, therefore, is very good.[1] In cascode stages, the effect of reverse agc on cross-modulation distortion is reduced when the agc is applied to the gate of the common-gate stage; application of reverse bias to the gate of the common-source stage results in cross-modulation performance similar to that of a single triode-connected stage. Figs.7 and 8 show the variation in cross-modulation susceptibility as a function of agc. The test circuits used to measure cross-modulation distortion of MOS transistors are shown in Fig.9.

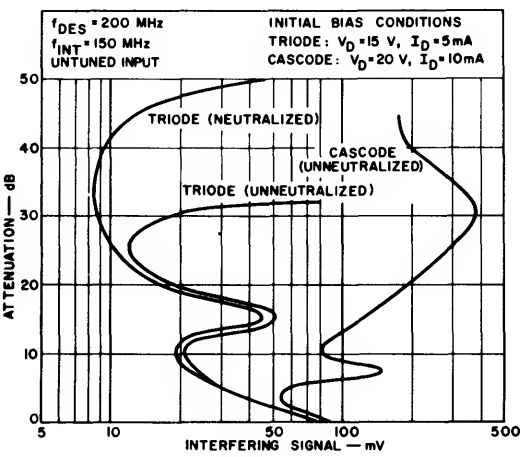


Fig.7 - Cross-modulation distortion as a function of the attenuation produced by reverse agc.

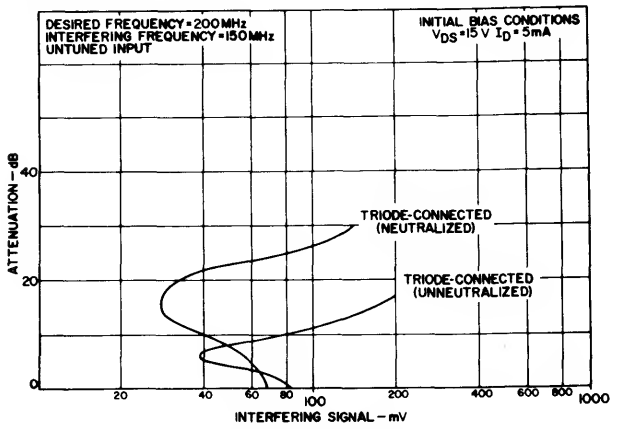


Fig.8 - Cross-modulatian distartian as a function af the attenuatian praduced when agc is accomplished by a reductian af drain-to-source voltage.

The test circuit shown in Fig. 10 is used to measure the intermodulation distortion of MOS transistors. In such measurements, the receiver is tuned to 150 MHz. The MOS is then inserted, and bias voltages are applied. When no signals are applied (i.e., the amplitudes of the signals f_1 and f_2 are both 0 volts), the rf indicator of the receiver indicates an equivalent input noise level of approximately 2.4 microvolts. The signals f_1 and f_2 are gradually increased in amplitude until the reading on the rf indicator is 1 microvolt above the noise level (3.4 microvolts total). This reading indicates that 2.4 microvolts of 150-MHz signal is being produced by the interaction of f_1 and f_2 (i.e., $2f_1 - f_2 = 150$ MHz). Table I lists the dc bias levels used for the 3N128 MOS transistor and the amplitude of the f_1 and f_2 signals required to produce an output, at 150 MHz, of 2.4 microvolts, which corresponds to 1 microvolt above the input noise level. The amplitudes of f_1 and f_2 were measured by an rf vacuum-tube voltmeter; the f_1 generator was turned down for measurement of f_2, and vice versa.

Table I

INTERMODULATION DISTORTION DATA FOR THE 3N128 MOS TRANSISTOR

V_D volts	I_D mA	Interfering Voltages Required to Produce 2.4 microvolts at 150 MHz: f_1 (175 MHz) mV	f_2 (200 MHz) mV
16.5	10	18	18
16.5	10	7	150
16.5	5	15	15
16.5	5	3.5	150
16.5	5	30	3.5
16.5	2.5	19	21

When the same test methods were used to measure the intermodulation distortion of bipolar transistors, distortion levels were found to be two to five times greater than those of the 3N128 MOS transistor.

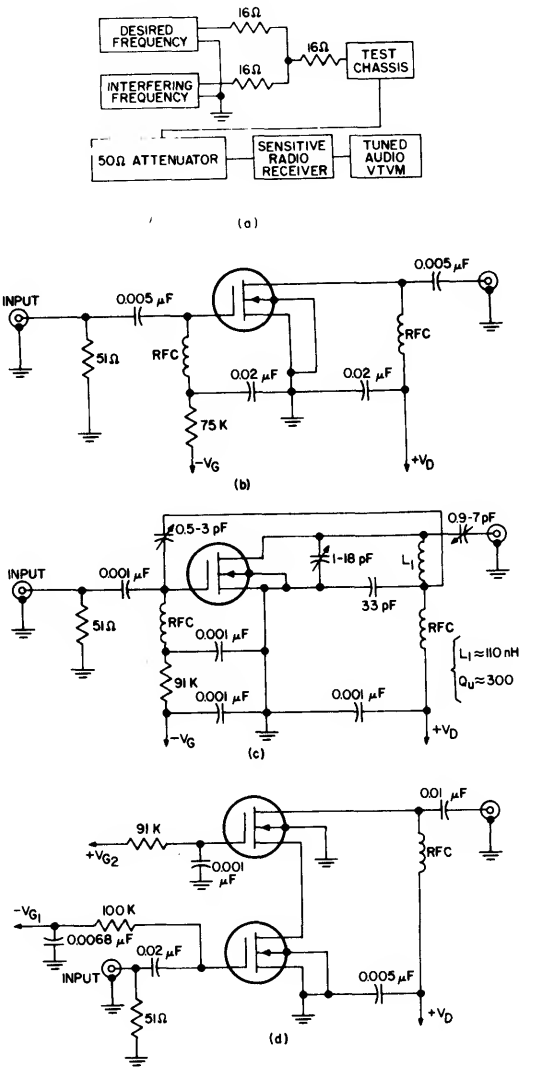


Fig.9 - Test circuits used to measure cross-modulation distortion in MOS transistors: (a) block diagram; (b) unneutralized-stage test circuit; (c) neutralized-stage test circuit; (d) cascode-stage test circuit.

Designing VHF MOS Amplifier Circuits

A complete set of graphs of typical y parameters, both as a function of frequency at constant bias and as as a function of bias at constant frequency, are given in the published data for the 3N128 MOS transistor. The application of these y parameters in the design of the 200-MHz amplifier shown in Fig. 3 is discussed in following paragraphs.

For operation at a frequency of 200 MHz, an I_D of

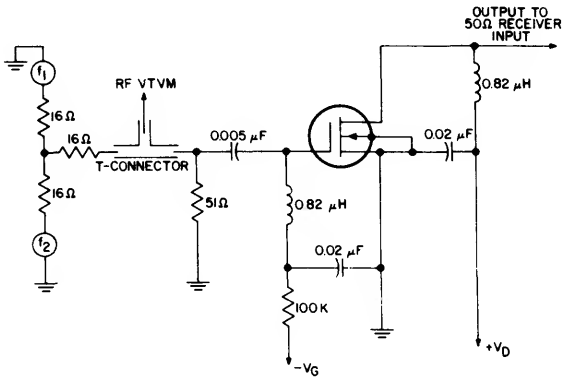


Fig.10 - Test circuit used to measure intermodulation distortion in MOS transistors.

5 milliamperes, and a V_D of 15 volts, the y parameters of the 3N128 are typically as follows:

y_{11} (input admittance with output short-circuited) = 0.45 + j7.2 mmhos

y_{22} (output admittance with input short-circuited) = 0.28 + j1.75 mmhos

y_{21} (forward transfer admittance with output short-circuited) = 7.0 - j1.9 mmhos

y_{12} (reverse transfer admittance with input short-circuited) = 0 - j0.16 mmhos

If y_{12} is assumed to be zero, the maximum available power gain (MAG) under conjugately matched conditions,* may be computed. MAG serves as a useful figure of merit for comparison of the vhf power gain of various MOS transistors. The MAG for the 3N128 is determined as follows:

$$MAG = \frac{|y_{21}|^2}{4Re(y_{11})Re(y_{22})} = \frac{|7.0-j1.9|^2}{4(0.45)(0.28)} = 104 = 20.2\,dB \quad (1)$$

where Re means "the real part of."

All MOS transistors have a small, but measurable, feedback component (y_{12}); it is possible, therefore, that some of them will oscillate under certain circuit conditions. This possibility may be checked by use of methods given by Linvill[2,4] and by Stern.[3,4] If the transistor is unconditionally stable for any combination of passive source and load admittances, then Linvill's critical stability factor C, as determined from the following equation, is less than |1|:

$$C = \frac{|y_{21}y_{12}|}{2Re(y_{11})Re(y_{22}) - Re(y_{21}y_{12})} \quad (2)$$

The critical stability factor for the 3N128 is calculated as follows:

$$C = \frac{|(7.0-j1.9)(0-j0.16)|}{2(0.45)(0.28) - Re(7.0-j1.9)(-j0.16)} = 2.08$$

Stern has derived a similar expression for stability C_S that includes the effect of the generator and load conductances, y_g and y_L, respectively, as follows:

$$C_S = \frac{|y_{21}y_{12}|}{2\,Re(y_{11}+y_g)Re(y_{22}+y_L) - Re(y_{21}y_{12})} < |1| \quad (3)$$

If a conjugate match is assumed at both the input and the output, then $Re(y_g) = Re(y_{11})$, and $Re(y_L) = Re(y_{22})$. For this condition, the stability factor is calculated as follows:

$$C_S = \frac{|(7.0-j1.9)(-j0.16)|}{2(0.45+0.45)(0.28+0.28) - Re(7.0-j1.9)(-j0.16)} = \frac{1.16}{1.31} = 0.885$$

These calculations show that the transistor itself is not unconditionally stable, but that it is stable when placed in a conjugately matched circuit. Therefore, neutralization is not required, although it may be used if a more symmetrical pass-band characteristic is desired. All unneutralized amplifiers have a certain amount of skew in the selectivity characteristic; if this skewness becomes objectionable for the required application, then neutralization (or mis-matching) is necessary.

When neutralization is desired, there are two common methods of obtaining the required feedback. The first, and more common method, is the capacitance-bridge technique shown in Fig.11(a). The capacitance bridge becomes more apparent when the circuit is redrawn as shown in Fig.11(b). The condition for neutral-

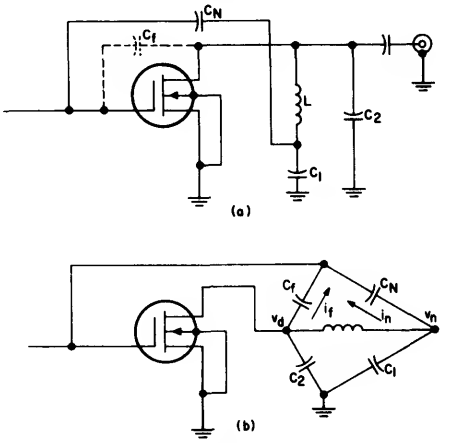


Fig.11 - Capacitance-bridge neutralization circuit: (a) actual circuit configuration; (b) circuit redrawn to emphasize capacitance-bridge network.

* Conjugate match means that the transistor input and the generator and the transistor output and load are matched resistively and that all reactance is tuned out.

ization is that $i_f = i_n$. This condition implies the following relationship:

$$\frac{v_d}{jX_f} = \frac{-v_n}{jX_n}, \text{ or } C_f v_d = -C_n v_n \quad (4)$$

The voltage v_n is defined by the following equation:

$$v_n = \left(\frac{v_d}{jX_L + jX_1}\right) jX_1 = \left(\frac{v_d}{\frac{-\omega^2 LC_1 + 1}{j\omega C_1}}\right) \frac{1}{j\omega C_1} = \frac{v_d}{-\omega^2 LC_1 + 1} \quad (5)$$

If this relationship for v_n is substituted in Eq.(4), the following result is obtained:

$$C_f v_d = -C_n \left(\frac{v_d}{-\omega^2 LC_1 + 1}\right), \text{ or } C_n = -C_f(-\omega^2 LC_1 + 1) \quad (6)$$

At resonance, the equation for the neutralization capacitance C_n may be rewritten as follows:

$$C_n = -C_f\left[\left(\frac{-1}{\omega C_2}\right)\omega C_1 + 1\right] = C_f\left(\frac{C_1}{C_2} - 1\right) \quad (7)$$

If $C_1 >> C_2$, Eq.(7) may be rewritten as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) \quad (8)$$

The other common method of neutralization is the transformer-coupled method shown in Fig.12. Again, the condition for neutralization is that $i_f = i_n$. The requirements for this condition are expressed by the following equation:

$$\frac{v_d}{X_f} = \frac{-v_n}{X_n}, \text{ or } C_f v_d = -C_n v_n \quad (9)$$

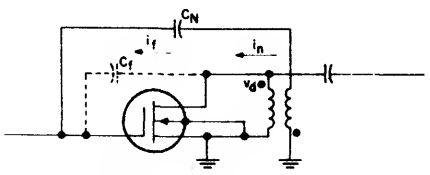


Fig.12 - Transformer-coupled neutralization circuit.

Eq.(9) may be rewritten in the following form:

$$\left|\frac{v_d}{v_n}\right| = \frac{C_n}{C_f} \quad (10)$$

The required turns ratio for the coupling transformer can be determined from Eq.(10).

The generator and load impedances must be matched to the transistor input and output impedances, respectively, to obtain maximum gain. For the 200-MHz amplifier shown in Fig.3, the generator resistance at the input is 50 ohms. For a conjugately matched input, the generator admittance y_g and the real part of the transistor input admittance must appear to be equal. Because the generator admittance y_g is 20 mmhos and the real part of the input admittance $Re(y_{11})$ is 0.45 mmho, the coupling transformer must provide a transformation ratio of 44 to obtain the desired impedance match. The turns ratio required is determined as follows:

$$\frac{N_2}{N_1} = \sqrt{44} = 6.6$$

Experimentally, a turns ratio of 4 was found to be approximately the optimum value. This difference results, in part, from the fact that the parallel resistance of the tank coil was not considered in the calculation. At the output of the 200-MHz amplifier, the load is also 50 ohms. Because the dc drain voltage must be blocked from the load, a series matching capacitor was selected which performs both dc blocking and resistive matching simultaneously.

In the actual load-circuit network shown in Fig.13(a), the value of capacitor C_S must be chosen so that the load admittance, $y_L = 20$ millimhos, is apparently equal to the real part of the transistor output admittance, $Re(y_{22}) = 0.28$ millimhos. Fig.13(b) shows the equivalent circuit of the load-circuit network for this condition.

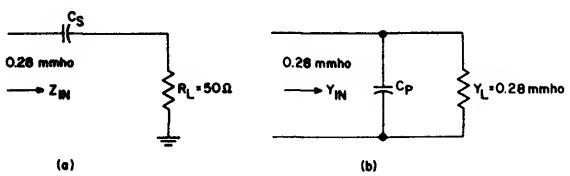


Fig.13 - Output network in which series coupling capacitance is used for dc-voltage blocking and resistive matching: (a) actual network; (b) electrical equivalent.

The following equation gives the input impedance Z_{IN} for the network shown in Fig.13:

$$Z_{IN} = R_S + \frac{1}{j\omega C_S} \quad (11)$$

The input admittance y_{IN}, therefore, may be expressed as follows:

$$y_{IN} = \frac{1}{R_p} + j\omega C_p = \frac{1}{Z_{IN}} = \frac{1}{R_S + \frac{1}{j\omega C_S}} \quad (12)$$

The terms in Eq.(12) are rearranged to obtain the following result:

$$\frac{R_S}{R_p} + j\omega C_p R_S + \frac{1}{j\omega C_S R_p} + \frac{j\omega C_p}{j\omega C_S} = 1 \quad (13)$$

The real and imaginary terms in Eq.(13) are equated to obtain the following relationships:

$$\frac{R_S}{R_p} + \frac{C_p}{C_S} = 1 \qquad (14)$$

$$\omega C_p R_S - \frac{1}{\omega C_S R_p} = 0 \qquad (15)$$

$$C_p = \frac{1}{(\omega C_S R_p)(\omega R_S)} \qquad (16)$$

Eq.(16) is substituted into Eq.(14) to obtain the following equation for the matching capacitance C_S:

$$C_S = \frac{1}{\omega}\sqrt{\frac{1}{(R_p - R_S)R_S}} \qquad (17)$$

Substitution of numerical values for the parameters in Eq.(17) yields the following value for C_S:

$$C_S = \frac{1}{2\pi(2 \times 10^8)}\sqrt{\frac{1}{(3600-50)50}} = 1.9 \text{ pF}$$

Experimentally, a 3-picofarad capacitor was found to perform very satisfactorily in the amplifier. If $R_p >> R_S$, then $C_p \approx C_S$. Therefore, a 3-picofarad capacitance appears in parallel with the 1.4-picofarad capacitance of the MOS transistor. A small 1-to-9-picofarad variable air capacitor was selected for the tank tuning capacitor to compensate for variations among transistors. For a nominal value of 2 picofarads for the air capacitor, the total output capacitance is 6.4 picofarads. The inductance required to resonate with 6.4 picofarads at 200 MHz is 0.1 microhenry. When the total output capacitance is known, the required neutralization capacitor can be calculated. If C_1 is arbitrarily selected as 33 picofarads, the neutralization is determined from Eq.(8), as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) = 0.2\left(\frac{33}{6.4}\right) = 1.0 \text{ pF}$$

The optimum value for the neutralization capacitor was determined experimentally by use of a small (0.5-to-3-picofarad) variable capacitor. This capacitor was adjusted to the optimum value for a typical unit (C_{rss} = 0.13 pF) and then fixed. The required input inductance was found to be 0.06 microhenry. The completed amplifier is shown schematically in Fig.3. The bandwidth of the amplifier is typically 8 MHz and shows negligible skew.

The y parameters may also be used to design a cascode vhf amplifier such as the one shown in Fig.5. This circuit had typical power gain and noise figure of 17 dB and 4.2 dB, respectively. The amplifier has a bandwidth of 10 MHz with negligible skew. The capacitance of the $source_2$-$drain_1$ interconnection must be tuned out to achieve a good vhf noise figure. The noise figure of the cascode amplifier is 2 to 3 dB higher if this capacitance is not tuned out.

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Chopper Circuits Using RCA MOS Field-Effect Transistors

by

F. M. Carlson

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but eliminate their inherent offset-voltage and leakage-current problems.

Basic Chopper Circuits

Chopper circuits are basically of either the shunt type or the series type, as shown in Fig. 1, or a combination of the two.

The shunt chopper circuit, shown in Fig. 1(a), operates as follows: When the switch S is opened, a voltage that is directly proportional to the input signal appears across the load. When the switch is closed, all of the input signal is shorted to ground. Therefore, if the switch is opened and closed periodically, the voltage across the load appears as a square wave that has an amplitude directly porportional to the input signal. This square wave may be highly amplified by a relatively drift-free, stable-gain ac amplifier. This procedure is generally used in low-level dc amplifiers, i.e., a small dc input is chopped, the resulting ac signal is amplified, and the output of the ac amplifier is rectified to produce a dc output directly proportional to the input.

The series chopper circuit, shown in Fig. 1(b), can also be used to chop dc signals. This type of circuit is particularly useful in telemetry or other systems in which a signal source such as a transducer is to be connected periodically to a load such as a transmitter.

An ideal chopper is simply an on-off switch that has certain desirable characteristics. Table I lists

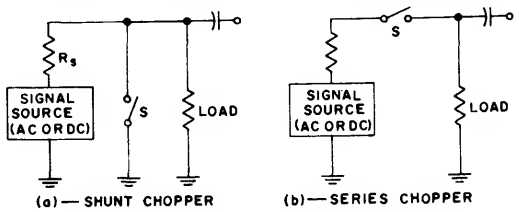


Fig. 1 - Basic chopper circuits.

Ideal Chopper Characteristics	Available Chopper Devices Compared to Ideal		
	MOS	Bipolar	Electromechanical Relay
Infinite Life	Good	Good	Poor
Infinite Frequency Response	Good	Good	Poor
Infinite OFF Resistance	Good	Fair	Good
Zero ON Resistance	Poor	Fair	Good
Zero Driving-Power Consumption	Good	Fair	Fair
Zero Offset Voltage	Good	Poor	Good
Zero Feedthrough between the driving signal and signal being chopped	Fair	Fair	Good
Small Size	Good	Good	Poor

Table I - Comparison of available chopper devices with an ideal.

some of these characteristics, and shows the relative merits of relays, bipolar transistors, and MOS transistors in each area.

Use of MOS Transistors as Choppers

Fig.2 shows voltage-current characteristics of an n-channel depletion-type MOS field-effect transistor such as the RCA-40460. Fig.3 shows an expanded view of the curves in Fig.2(a) in the region about the origin.

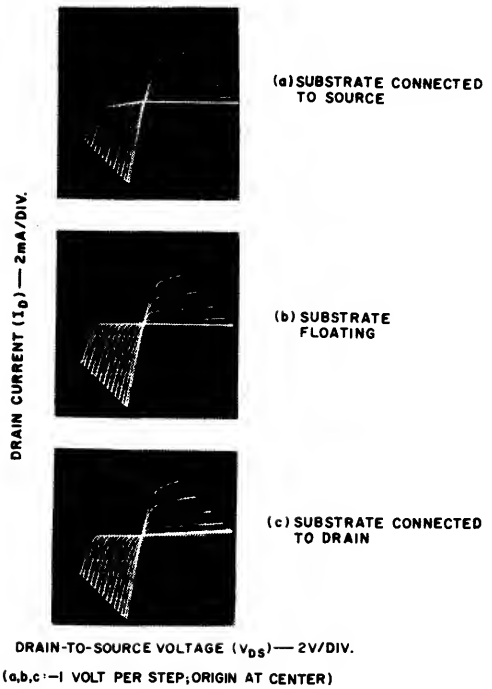


Fig.2 - Voltage-current characteristics of an n-channel depletion-type MOS transistor: (a) with substrate connected to source; (b) with substrate floating; (c) with substrate connected to drain.

Because each curve passes through the origin, the MOS transistor is said to have zero offset voltage. In an MOS shunt chopper circuit, therefore, the output is zero when the input voltage is zero. This result is not obtained with bipolar transistors. Even for zero input voltage, a bipolar transistor has an offset voltage equivalent to the collector-to-emitter saturation voltage $V_{CE}(sat)$ between its collector and emitter terminals. MOS transistors have no parameter comparable to $V_{CE}(sat)$.

When the gate-to-source voltage V_{GS} is zero, an MOS transistor such as the 40460 has an effective resistance of 200 to 300 ohms between its drain and source terminals. If the gate-to-source voltage is made positive, this resistance decreases to about 100 ohms (typically to 90 ohms for the 40460). No significant increase in gate current occurs when V_{GS} is made positive because the gate of an MOS transistor is insulated from the source-to-drain channel by an oxide layer. (In a junction-gate field-effect transistor, the gate and the channel form a p-n junction, and low gate current can be obtained only when this junction is reverse-biased.) When the resistance between the drain and source terminals is low (100 to 300 ohms), an MOS transistor is said to be ON; the drain-to-source channel resistance is then designated as $r_{ds}(ON)$. This ON condition corresponds to the closed-switch condition in the circuits of Fig.1.

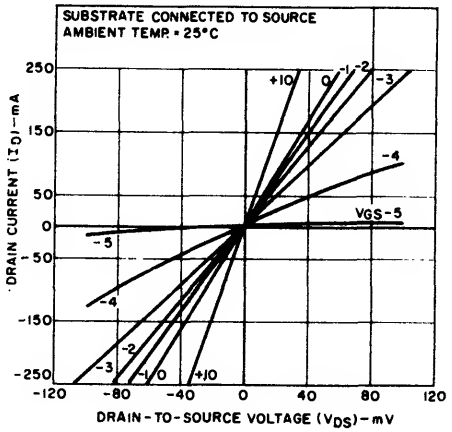


Fig.3 - Low-level drain current as a function of drain-to-source voltage in an n-channel depletion-type MOS transistor with substrate connected to source.

When a negative voltage of about -6 volts or more is applied between the gate and the source of the MOS transistor, the channel resistance between drain and source becomes extremely high (typically thousands of megohms). In this condition, which is known as "cutoff" or "pinchoff", it is impractical to measure the channel resistance directly; instead, the leakage current that flows from drain to source at cutoff is normally specified. This current $I_D(OFF)$, is typically 0.1 nanoampere for the 40460. Because $I_D(OFF)$ is measured at a drain-to-source voltage of 1 volt, the equivalent channel resistance is 10,000 megohms. This OFF condition corresponds to the open-switch condition in the circuits of Fig.1.

Fig.4 shows three basic chopper circuits using the MOS field-effect transistor. The gating signal for the 40460 should swing from zero to at least -6 volts, and may cover a range as large as ±10 volts. The substrate (and thus the case) of the 40460 transistor is usually connected to the source. However, if the incoming

signal to be chopped exceeds -0.3 volt, the substrate must be "floated", connected to the drain, or biased negatively so that the source-to-substrate and drain-to-substrate voltages never exceed -0.3 volt. If this value is exceeded, the substrate, which forms two p-n junctions with the drain and the source, becomes forward-biased and the resulting flow of diode current shunts the incoming signal to ground.

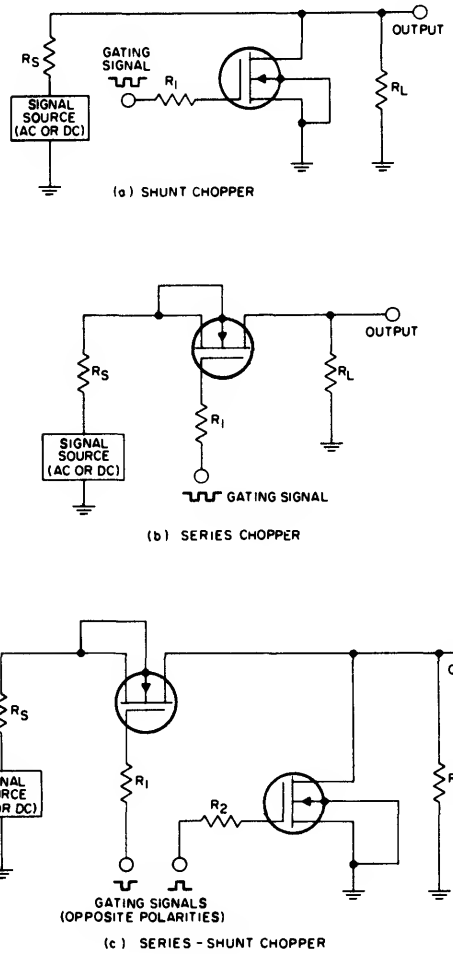


Fig.4 - Basic MOS chopper circuits.

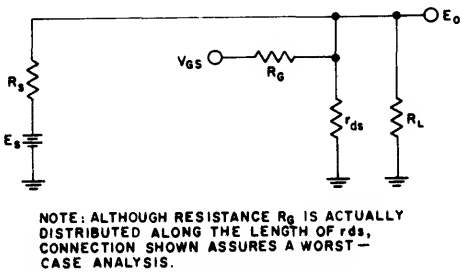
Steady-State Conditions

Ideally, when an MOS transistor in a shunt chopper circuit is ON, the output voltage of the circuit should be zero. Because the drain-to-source resistance rds is some finite value, however, the output cannot reach true zero. Fig.5 shows an equivalent circuit for steady-state conditions in an MOS shunt chopper. For the ON condition, the output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (1)$$

In Eq.(1), it is assumed that the gate leakage resistance R_G is much larger than the drain-to-source resistance r_{ds}. If the load resistance R_L is also much larger than r_{ds}; Eq.(1) can be simplified as follows:

$$E_O = E_S \left[\frac{r_{ds}}{R_S + r_{ds}} \right] \quad (2)$$



NOTE: ALTHOUGH RESISTANCE R_G IS ACTUALLY DISTRIBUTED ALONG THE LENGTH OF rds, CONNECTION SHOWN ASSURES A WORST-CASE ANALYSIS.

Fig.5 - Steady-state equivalent circuit of MOS shunt chopper.

For E_O to approach zero, it is necessary that the source resistance R_S be much greater than r_{ds}. The value of E_O is then given by

$$E_O = E_S (r_{ds}/R_S) \quad (3)$$

A typical value for R_S and R_L in an MOS shunt chopper is 0.1 megohm. A typical value of r_{ds}(ON) for the 40460 transistor is 90 ohms. If these values are substituted in Eq.(3) and the signal voltage E_S is assumed to be 1 millivolt, E_O is calculated as follows:

$$E_O = 10^{-3} (90/10^5) = 0.9 \text{ microvolt}$$

In the ON condition, therefore, the dc error voltage is less than 0.1 per cent for the values used, and is directly proportional to the input signal.

For the OFF condition, the steady-state output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] + V_{GS} \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_G + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (4)$$

In most MOS transistors, both $r_{ds}(OFF)$ and R_G are much greater than R_L. Therefore, Eq.(4) may be simplified as follows:

$$E_O = E_S \frac{R_L}{R_S + R_L} + V_{GS} \frac{R_L}{R_G} \qquad (5)$$

If R_S, R_L, and E_S are assumed to have the values used previously, the gate-to-source voltage V_{GS} is assumed to be -10 volts, and the gate resistance R_G is assumed to be 10^{12} ohms (minimum permissible gate resistance for the 40460), the value of E_O is calculated as follows:

$$E_O = 10^{-3}\left[\frac{10^5}{2 \times 10^5}\right] - 10\left[\frac{10^5}{10^{12}}\right]$$

$$= \frac{10^{-3}}{2} - 10^{-6} \approx 0.5 \text{ millivolt}$$

The second term in Eq.(5) is the error term for the OFF condition; it is not proportional to the input signal E_S. For the numbers used, the output error in the OFF condition is only 0.2 per cent. If a typical value of 10^{14} ohms is used for the 40460 gate resistance instead of the minimum value of 10^{12} ohms, the error voltage is reduced to only 0.002 per cent. The output error remains small for any value of signal voltage E_S that does not approach the error voltage in magnitude.

Because the error voltage is inversely proportional to the gate leakage resistance R_G, most junction gate field-effect transistors produce larger error voltages than MOS transistors (the minimum R_G of most junction-gate devices is only 1 to 10 per cent that of MOS transistors).

A similar procedure may be used for analysis of series chopper and series-shunt chopper circuits.

The operation of all MOS chopper circuits is greatly affected by the magnitude of the source and load resistances. Table II lists the output voltages of the three basic chopper circuits for various combinations of source and load resistances. It is assumed that the input voltage E_S is 1 millivolt, and that the drain-to-source resistance r_{ds} is 100 ohms in the ON condition and 1000 megohms in the OFF position. The gate leakage resistance R_G (10^{12} ohms or more) is neglected. The following conclusions can be drawn from the data shown:

1. Only the series or the series-shunt circuit should be used when $R_S < r_{ds}(ON)$.
2. In general, R_L should be high. ($R_L >> r_{ds}(ON)$)
3. The load resistance should be higher than the source resistance. ($R_L \geq R_S$)
4. The performance of the series-shunt circuit is equal to or better than that of either the series or the shunt chopper alone for any combination of R_S and R_L.

Source Resistance R_S (ohms)	Load Resistance R_L (ohms)	Approximate Output Voltage E_o - μV (Max. Output = 1 mV) Shunt Chopper (ON)	Shunt Chopper (OFF)	Series Chopper (ON)	Series Chopper (OFF)	Series-Shunt Chopper (ON)	Series-Shunt Chopper (OFF)
1 M	1 M	0.1	500	500	1	500	0.0001
100 K	1 M	1	900	900	1	900	0.0001
100	1 M	500	1000	1000	1	1000	0.0001
0	1 M	1000	1000	1000	1	1000	0.0001
1 M	100 K	0.1	90	90	0.1	90	0.0001
1 M	100	0.05	0.1	0.1	0.0001	0.1	0.00005
100 K	100 K	1	500	500	0.1	500	0.0001
100	100	333	500	333	0.0001	333	0.00005

Table II - Steady-state chopper output voltage for various source and load resistances.

Transient Conditions

Fig.6 shows the ac equivalent circuit of an MOS shunt chopper. The interelectrode capacitances of the MOS transistor affect operation of the circuit at high frequencies. The input capacitance C_{gs} increases the rise time of the gate driving signal and thus increases the switching time of the chopper. This effect is not usually a serious limitation, however, because the switching time of the MOS transistor depends primarily on the input and output time constants. Switching times as short as 10 nanoseconds can be achieved when an MOS transistor is driven from a low-impedance generator and the load resistance is less than about 2000 ohms.

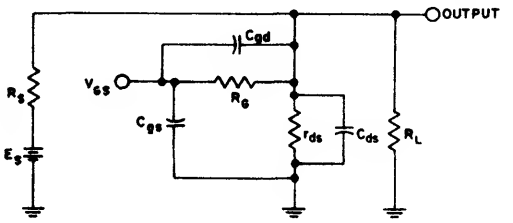


Fig.6 - AC equivalent circuit of MOS shunt chopper.

The output capacitance C_{ds} also tends to limit the maximum frequency that can be chopped. When the reactance of this capacitance becomes much lower than the load resistance R_L, the chopper becomes ineffective because $X_{C_{ds}}$ is essentially in parallel with R_L and $r_{ds}(OFF)$.

The feedthrough capacitance C_{gd} is the most important of the three interelectrode capacitances because it couples a portion of the gate drive signal into the load circuit and causes a voltage spike to appear across R_L each time the gate drive signal changes state. C_{gd} and R_L form a differentiating network which allows the leading edge of the gate drive signal to pass through. The output capacitance C_{ds} is beneficial to the extent that it helps reduce the amplitude of the feedthrough spike.

The effect of the feedthrough spikes can be reduced by several methods. Typical approaches include the following:

(a) use of a clipping network on the output when the input signal to be chopped is fixed in amplitude,

(b) use of a low chopping frequency,

(c) use of an MOS transistor that has a low feedthrough capacitance C_{gd} (some RCA MOS transistors have typical C_{gd} values as low as 0.13 picofarad),

(d) use of a gate drive signal that has poor rise and fall times,

(e) use of a source and load resistance as low as feasible,

(f) use of a shield between the gate and drain leads,

(g) use of a series-shunt chopper circuit.

Temperature Variations

The variation of MOS transistor parameters with temperature can affect the operation of a chopper circuit unless allowance is made for such variations in the circuit design. It is important, therefore, to determine the approximate degree to which each parameter can be expected to change with temperature. Fig.7 shows curves of channel resistance r_{ds}, gate leakage current

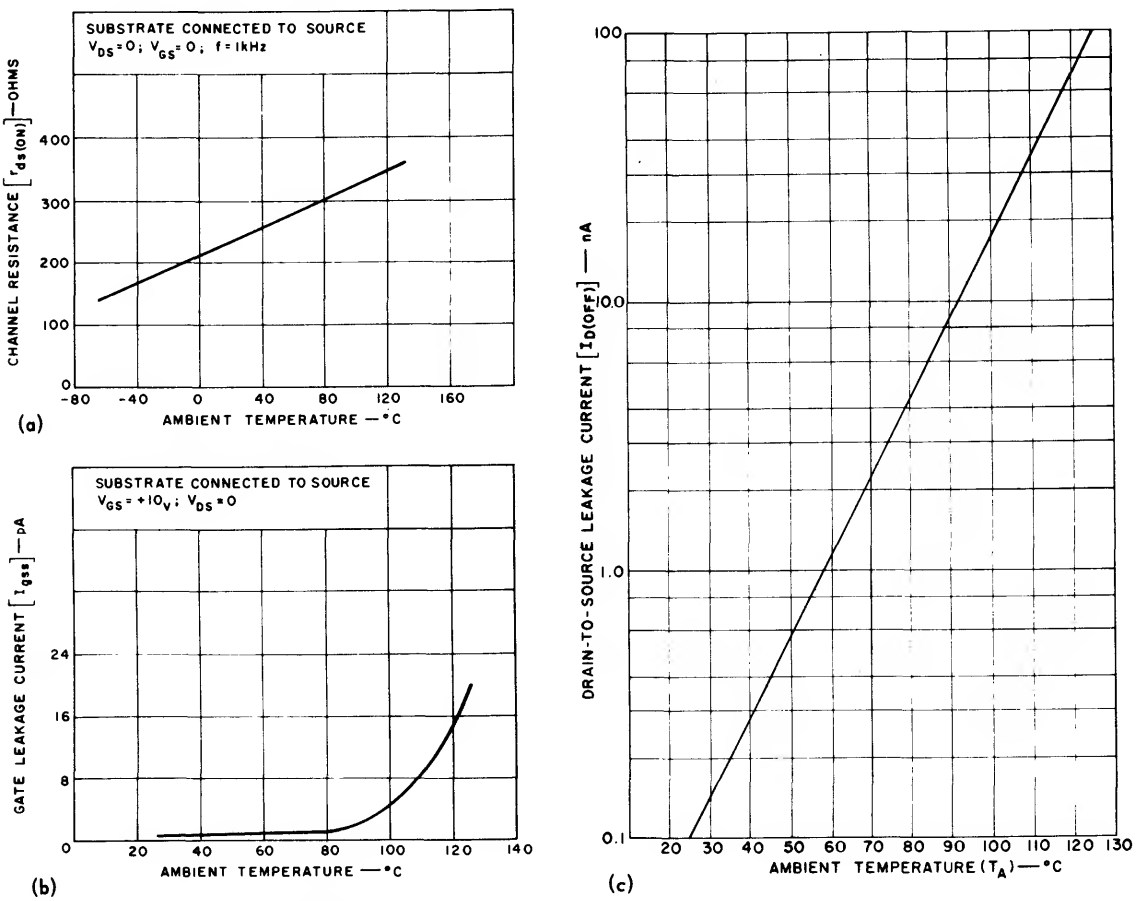


Fig.7 - Variation of 40460 parameters with ambient temperature: (a) channel resistance r_{ds}; (b) gate leakage current I_{gss}; (c) drain-to-source leakage current $I_{D(OFF)}$.

I_{GSS}, and drain-to-source leakage current $I_{D(OFF)}$ as a function of temperature for the 40460. I_{GSS} and $I_{D(OFF)}$ were not measured at temperatures below 25° C because condensation and frost that form on the test chassis result in erroneous and/or erratic readings of pico-ampere currents. Test circuits used to measure these parameters are shown in the Appendix.

Typical Circuits

Fig.8 shows three chopper circuits that were constructed for demonstration purposes: (a) a shunt chopper, (b) a series chopper, and (c) an ac chopper. The 0.005-microfarad capacitor across the gate drive generator in

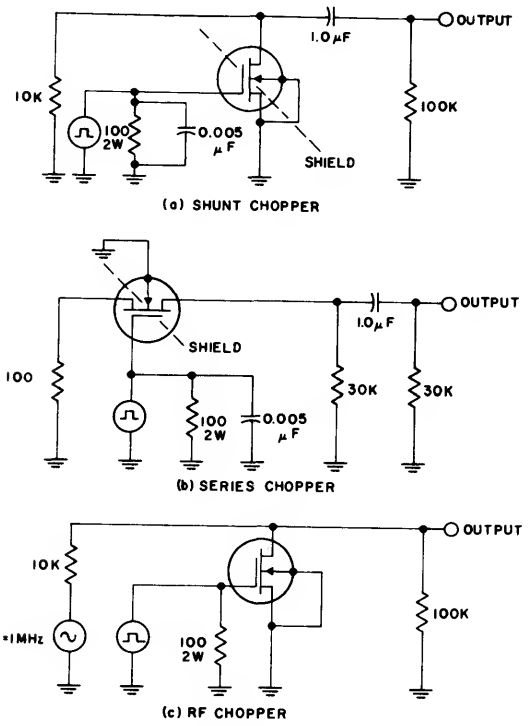


Fig.8 - Typical MOS chopper circuits: (a) shunt chopper; (b) series chopper; (c) rf chopper.

circuits (a) and (b) increases the rise time of the gate drive signal. A resistor is used in each circuit to simulate the impedance of the signal source. The actual input voltage was set at zero so that spike feedthrough and offset voltages could be measured. The dc offset voltage, which is caused primarily by the average value of the spikes over the whole cycle, was too small to be measured on the equipment available. Fig.9 shows the actual spike feedthrough for the 40460 and 3N128 MOS transistors in the shunt and series circuits of Figs.8(a) and 8(b); the rise time of the gate drive signal was 1 microsecond.

It is recommended that MOS choppers be driven from a square-wave source. Fig.10 shows the feedthrough that results when the circuits of Figs.8(a) and 8(b) are driven from a sine-wave generator instead of a square wave.

Fig.11 shows how the circuit of Fig.8(c) can be used to chop an rf signal at either a slow or a fast chopping frequency. The 40460 transistor can be used to chop rf signals extending up to the low vhf region. The frequency of the gate drive signal can be as high as several hundred kilohertz before excessive degradation of the square wave occurs. The rise time of the

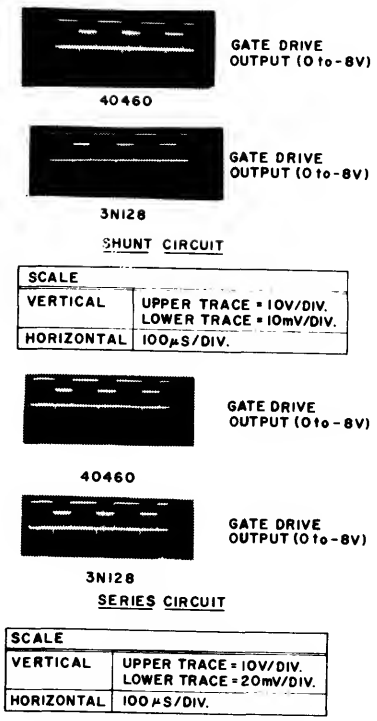


Fig.9 - Actual spike feedthrough in shunt and series chopper circuits employing the 40460 and 3N128 MOS transistors.

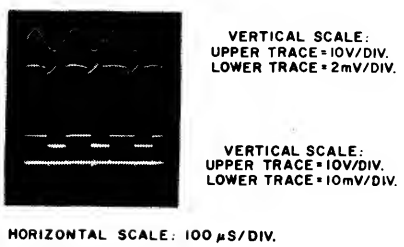


Fig.10 - Comparison of sine- and square-wave gate drive for an MOS shunt chopper employing the 40460.

gate drive signal for the circuit of Fig. 8(c) was 15 nanoseconds.

In field-effect-transistor choppers using a version of the series-shunt circuit shown in Fig.8(c), noise and offset voltages as low as 10 microvolts or less have been obtained.[1] Balanced MOS chopper circuits using special compensating networks have also been developed to chop 0.1-microvolt signals at impedance levels up to 40,000 ohms and chopping frequencies up to 250 Hz.[2]

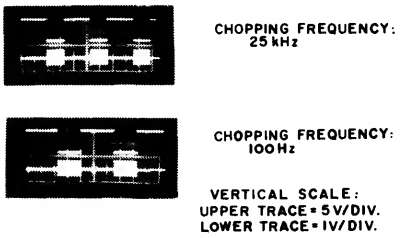


Fig.11 - Results of using MOS rf chopper at a fast and a slow chopping frequency.

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APPENDIX

Test Circuits

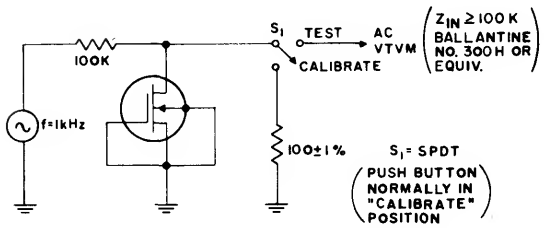


Fig.A-1 - Channel resistance ($r_{ds}(ON)$) measurement circuit.

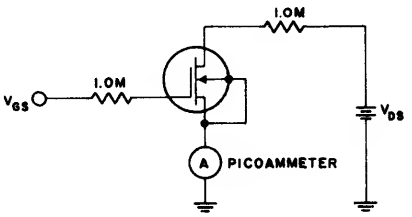


Fig.A-2 - Cutoff current ($I_D(OFF)$) measurement circuit.

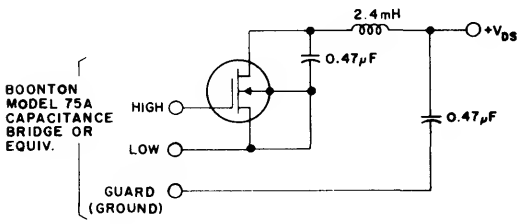


Fig.A-3 - Input capacitance (C_{iss}) measurement circuit.

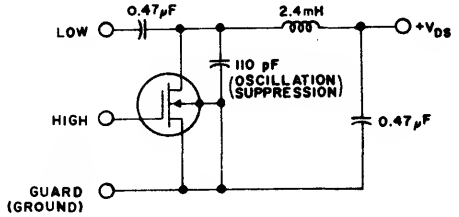


Fig.A-4 - Reverse transfer (Feedback) capacitance (C_{rss}) measurement circuit.

An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

by

C.H. Lee and S. Reich

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response[1], dynamic range, noise immunity, gain, and feedthrough capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer. A conversion gain of 17.5 dB was obtained, to provide an over-all tuner gain of approximately 30 dB. RF and mixer circuit considerations pertinent to the design are discussed.

Performance Features of MOS Transistors

Spurious response in an FM tuner is caused by the mixture of unwanted signals with the desired carrier in either the rf stage or the mixer. This effect can be expressed mathematically by use of the Taylor series expansion of the simple transfer function of output current as a function of input voltage at the operating point, as follows:

$$i_o = I_o + \alpha e_s + \beta e_s^2 + \theta e_s^3 + \ldots \qquad (1)$$

where i_o is the instantaneous value of output current of the device; I_o is the dc component of output current; e_s is the rf signal voltage present at the input terminal of the transistor; and α, β, and θ are the coefficients of a Taylor series expansion. These coefficients are related to the first-, second-, and third-order derivatives of the transfer characteristic as determined by the bias point. It can be shown[2,3] that mixing action within the device is attributable to the second-order term (βe_s^2), and that cross-modulation and intermodulation result from third- and higher-order terms. Therefore, when a device has an inherent square-law transfer characteristic, i.e., the drain current varies as the square of the applied gate-to source voltage, third- and higher-order terms are zero and spurious response is eliminated. The transfer characteristic of MOS field-effect transistors more nearly approaches this ideal square-law relationship than the very steep exponential transfer characteristic of bipolar transistors.

The dynamic-range capability of MOS field-effect transistors is about 25 times greater than that of bipolar transistors. In an actual tuner circuit, this large intrinsic dynamic range is reduced by a factor proportional to the square of the circuit source impedances.[4] The net result is a practical dynamic range for MOS tuner circuits about five times that for bipolar types.

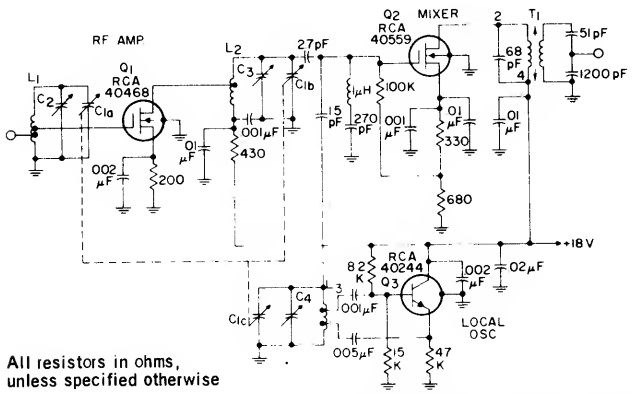
With MOS field-effect transistors, as contrasted with either bipolar transistors or junction-gate field-effect transistors, there is no loading of the input signal, nor drastic change of input capacitance even under extreme overdrive conditions.

In junction-gate field-effect transistors, a large incoming signal can have sufficiently high positive swing to drive the gate into conduction by a momentary forward bias; power is then drawn from the input signal in the same way as if a resistance were placed across the input circuit. In bipolar transistors, there is a gradual change of both input impedance and input capacitance as a function of large signal excursions. These changes are undesirable because they can result in detuning of tuned circuits and widening of the input selectivity curve.

FM Tuner Design

The FM tuner shown in Fig.1 uses single-gate MOS field-effect transistors in the rf-amplifier and mixer stages and a bipolar transistor as the local oscillator. The rf-amplifier transistor RCA-40468 operates in the common-source configuration with a stage gain of 12.7 dB. The mixer transistor RCA-40559 also operates in the common-source configuration, with both the rf and local-oscillator signals applied to the gate terminal. The bipolar oscillator transistor RCA-40244 operates in the common-collector mode. The conversion power gain from the mixer stage is 17.5 dB; the total gain of the tuner is 30.2 dB.

Performance of the FM tuner was evaluated by use of the bipolar-transistor if amplifier shown in Fig.2. The 10.7-MHz if output from the tuner is coupled to the first if-amplifier stage by means of a double-tuned transformer T_1. The if amplifier employs two 40245 and one 40246 bipolar transistors, each operating in a neutralized common-emitter configuration at a collector current of 3.5 milliamperes. The over-all gain of the if amplifier is 88 dB. A detailed analysis of a similar if amplifier is covered in an earlier publication.[5]



C_{1a}, C_{1b}, C_{1c} - 3-gang tuning capacitor, TRW 5-plate Model V2133 with trimmers stripped off.

C_2, C_3, C_4 - Arco 402 trimmer, maximum value 10 pF

L_1 - No.18 bare copper wire, 5 turns on 19/64" form, coil length 1/2", with IRN .250" x .250" Arnold slug. Q_0 = 164. Antenna tap at 0.8 of a turn, output tap at 1.4 turns.

L_2 - No.18 bare copper wire, 5 turns on 15/64" form, coil length 3/8", with 0.181" x 0.375" Arnold slug. Q_0 = 104.

L_3 - No.18 bare copper wire, 5 turns, air core with 3/8" O.D., coil length 1/2". Emitter tap on 1-1/2 turns. Feedback tap on 2 turns. Q = 164.

T_1 - Double tuned, 90 per cent of critical coupling. Primary unloaded uncoupled Q = 137 with 68-pF tuning capacitance, secondary unloaded uncoupled Q = 76 with 47-pF tuning capacitance. Secondary has a turns ratio of 26.2 to 1.0. Primary, No.32 enamel wire, 15 turns, space wound at 60 TPI, 0.250" x 0.500" TH slug. Secondary, No.36 enamel wire, 18 turns, close wound, 0.250" x 0.250" TH slug. Both coils on 9/32" form without shield.

Fig.1 - Circuit diagram of FM tuner using MOS transistors for the rf amplifier and mixer stages.

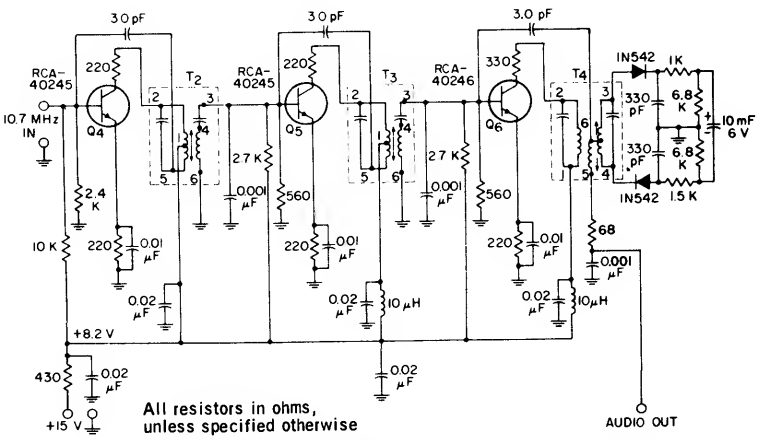


Fig.2 - Three-stage if amplifier using bipolar transistors.

Table I summarizes the performance of the MOS tuner. Spurious response was evaluated with a generator output of 350 millivolts.

OVER-ALL TUNER PERFORMANCE

Carrier Frequency	100	MHz
Modulation Frequency	400	Hz
Deviation (except IHFM)	22.5	kHz
Sensitivity:		
IHFM	1.75	μV
20-dB Quieting	1.5	μV
30-dB Quieting	1.75	μV
3-dB Limiting	2.5	μV
Image Rejection	62	dB
IF Rejection	96	dB
Half-IF Rejection	92	dB
Spurious Response across VHF band with $e_{gen.}$ = 0.35 volt	NONE	

Table I - Over-all performance characteristics of FM tuner.

RF-Circuit Considerations

The RCA-40468 MOS transistor used in the rf amplifier stage has a maximum available gain of 24 dB. Because the design criteria required a total mismatch plus insertion loss of 11.3 dB, the net gain for the stage is 12.7 dB. Although the design procedure used for these calculations has been discussed previously,[1,6] some of the considerations for optimizing performance warrant additional comment.

In the design of an rf stage for FM performance, the stage gain should be a compromise between optimum receiver sensitivity and spurious response rejection. In other words, the rf gain capability should be large to minimize the effects of noise from the mixer, and yet be limited to prevent a very large undesired incoming signal located on the skirt of the selectivity curve from driving the mixer beyond its dynamic range. Good FM tuner performance is achieved by selection of the proper rf-stage gain and step-down to the mixer input.

The rf input coil L_1 is tapped down to provide the smallest practical input swing to the gate of the rf-amplifier transistor for increased dynamic range. This tap-down is a compromise between optimizing for dynamic range and noise. When the degree of mismatch has been established, the drain-circuit load L_2 is determined from stage-gain and bandwidth requirements. Table II shows the device parameters used for the design of the rf stage.

The 40468 MOS transistor has a typical feedback capacitance of 0.12 picofarad, with a maximum value of 0.2 picofarad. This small value of C_{rss} minimizes oscillator radiation feedback through the device, and also makes it unnecessary to add neutralization components to the rf stage to achieve adequate gain.

Mixer-Circuit Considerations

The mixer circuit shown in Fig.1 is designed for operation into an 8000-ohm load. A load up to 12,000 ohms is permissible and provides a gain increase of about 1 dB from the mixer. The input circuit is tapped down by a 2.7-picofarad capacitor in series with the device input capacitance to improve dynamic range. These mismatch losses result in a stage gain of 17.5 dB, as compared to the maximum available gain of 21.5 dB shown in the published data for the 40559 transistor.

The trap consisting of a 1-microhenry inductor and 270-picofarad capacitor is designed to bypass any 10.7-MHz component that may appear at the input to the mixer. A 1.5-picofarad capacitor couples the oscillator signal to the mixer gate. Because the capacitor is small, interaction with the oscillator tuned circuit is minimized and good oscillator stability is maintained. The injection level at the gate of the mixer is 700 millivolts rms.

The biasing arrangement for the mixer stage is particularly important: substrate bias is used to provide the optimum combination of mixing and spurious-response rejection. Fig.3 shows the shift of the transfer characteristic as a function of negative substrate bias E_{bs} for the RCA-40559 mixer transistor.

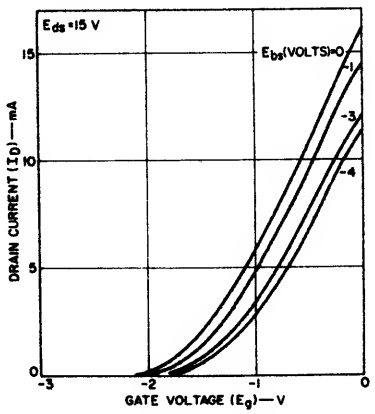


Fig.3 - Transfer characteristics of the RCA-40559 MOS field-effect transistor for several values of substrate bias.

The transconductance, which is the first derivative of the transfer characteristic, also varies as a function of substrate bias, as shown in Fig.4. As stated previously, mixing is accomplished by means of the quadratic term of Eq.(1); higher-order terms contribute only to undesired responses. For ideal mixing, therefore, the

transconductance curve should approach a straight line. As the transconductance curve becomes linear, higher-order derivatives (i.e., above the second) reduce to zero and the conversion transconductance increases. Fig.4 shows that the transconductance curve is most linear at

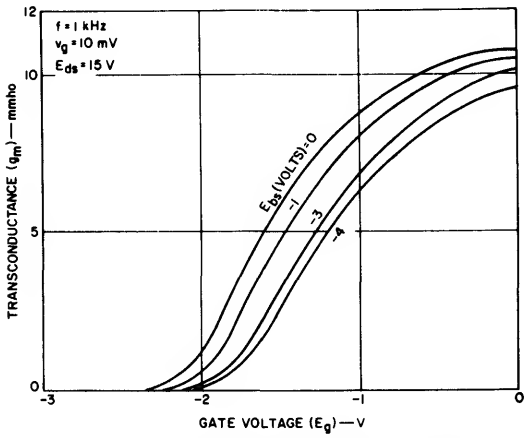


Fig.4 - Transconductance of the RCA-40559 as a function of gate bias with the substrate voltage as the parameter.

a substrate bias of -3 volts. Fig.5 shows the relative conversion gain of the RCA-40559 mixer stage as a function of the oscillator injection level at substrate bias of zero and -3 volts. It can be seen that the conversion transconductance also increases with the oscillator injection level.

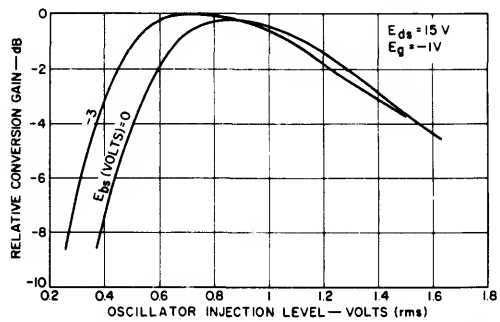


Fig.5 - Conversion transconductance as a function of oscillator injection level.

Table II shows the MOS device characteristics measured under circuit conditions. Reasonable verification of the measured conversion transconductance was obtained by calculation of the conversion transconductance for gate voltages ranging from zero to -2.1 volts. Details of these measurements are given in the Appendix.

Parameter	Units	RF Amplifier RCA-40468	Mixer RCA-40559
C_{rss}	pF	0.12	0.12
R_{in}	KΩ	4.5	6 (100 MHz)
C_{in}	pF	5.5	5.0
R_o	KΩ	4.2	12 (10.7 MHz)
C_o	pF	1.4	1.5
y_{21}	mmho	7.5	2.8
MAG	dB	24.2	21.5
MUG (unneutralized)	dB	14	-
G_p (in tuner)	dB	12.7	17.5

Table II - Device parameters for RCA-40468 and 40559 MOS field-effect transistors.

On the basis of these results, the optimum operating conditions for the mixer circuit were empirically established at an effective gate bias of -1 volt and an effective substrate bias of -3 volts to provide a typical drain current of 3 milliamperes.

Oscillator-Circuit Considerations

The common-collector oscillator circuit shown in Fig.1 generates an extremely clean output waveform. The absence of harmonics in the oscillator signal is an important factor in good tuner design. The oscillator signal is coupled to the mixer gate by means of a 1.5-picofarad capacitor which isolates the tuned circuit of the oscillator from the input circuit of the mixer and thus minimizes the possibility of oscillator instabilities as a result of "pulling".

Over-all Tuner Performance

The performance of the single-gate MOS tuner with respect to sensitivity, limiting, and particularly spurious response exceeds that obtained with the best bipolar transistors. In general, spurious-response performance can be degraded by inadequate circuit layout and wiring practices. For this reason, care should be exercised in arranging the physical layout of the tuner, and power-supply decoupling should be used.

Figs.6 and 7 show the measured sensitivity of the tuner of Fig.1. The quieting sensitivity, shown in Fig.6, is practically flat across the entire FM band. IHFM sensitivity and 3-dB limiting, shown in Fig.7, show the same excellent performance. The IHFM sensitivity test input voltage, as defined by the Institute of High Fidelity Manufacturers, is the minimum 100-per-cent-modulated signal input which, when applied to a receiver through the standard 300-ohm dummy antenna and an audio voltmeter connected through a 400-Hz filter, re-

duces a total internal receiver noise and distortion to the point where the output rises 30 dB when the 400-Hz null filter is removed from the audio voltmeter circuit. This value is expressed in microvolts.

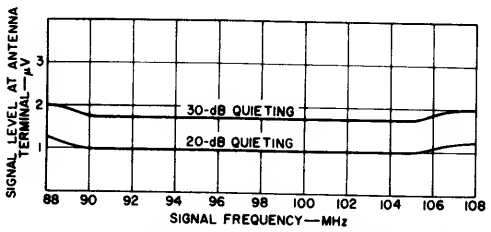


Fig.6 - Signal level for 20- and 30-dB quieting as a function of signal frequency.

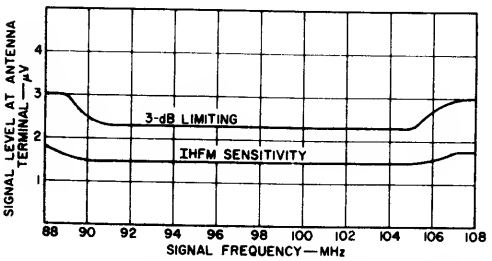


Fig.7 - Signal level for 3-dB limiting and IHFM sensitivity as a function of signal frequency.

Figs.8 and 9 provide additional performance characteristics. Fig.8 shows the gain and noise characteristics; Fig.9 shows the image and half-if rejection of the tuner. The spurious responses shown in Fig.9 were measured with a generator drive capability of 350-millivolts from 10.7 to 216 MHz.

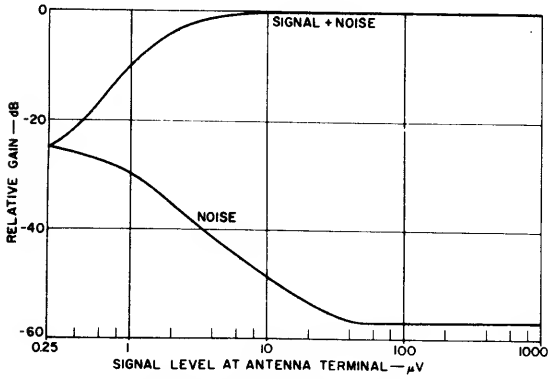


Fig.8 - Relative gain of signal and noise as a function of the signal voltage level.

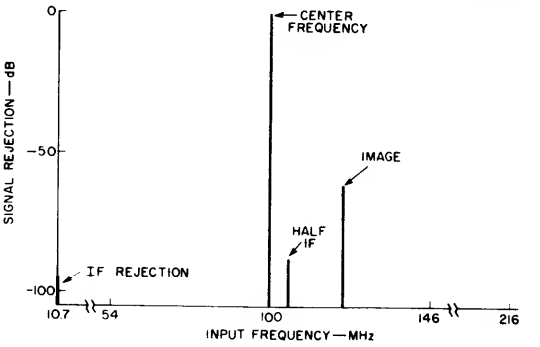


Fig.9 - Signal rejection as a function of input frequency, measured with a generator voltage of 350 millivolts.

MOS transistors covering a wide range of drain current were tested in the rf-amplifier and mixer sockets. Performance variations for image rejection and half-if rejection were within ± 1 dB of the values shown in Table I. Variations in sensitivity were less than 0.25 microvolt.

Conclusions

The RCA-40468 and 40559 MOS field-effect transistors were designed into an FM tuner. Evaluation of this tuner was made in conjunction with an FM-if amplifier that used 40245 and 40246 bipolar transistors. Over-all performance of the combination showed that the capability of MOS devices for dynamic range, sensitivity, and spurious response rejection exceeds that obtained with similar FM tuners that used bipolar transistors. Experimental work indicated that performance variations as a function of product distribution were insignificant.

APPENDIX

Calculation of Conversion Transconductance from the Operating Characteristic

The following procedure is used to calculate the conversion transconductance of the mixer stage based on the degree of linearity of the transconductance curves of Fig.4 and the magnitude of the oscillator injection voltage. The results show that the conversion transconductance is greatest for the curve that is most linear. For the mixer circuit described in this Note, this condition occurs at a substrate bias of -3 volts.

For the curves of Fig.4, the transconductance g_m is given by the following general relation:

$$g_m = f(E_g) \qquad (2)$$

where E_g is the gate bias. For a substrate bias of -3 volts, and a gate bias between zero and -2.1 volts,

the corresponding curve of transconductance is expressed as follows:

$$g_m = 12.5 - 2.14\epsilon^{-0.937E_g} \quad (3)$$

For optimum mixer performance with a minimum of spurious responses, a gate voltage of -1 volt was selected as the quiescent operating point. The Taylor series expansion for Eq.(3) for a center-point operating bias E_g of -1 volt is given by

$$g_m = 10.3 + 2.584\ e_g - 0.148\ e_g^2 + 0.75\ e_g^3 + \ldots \quad (4)$$

where e_g is the instantaneous voltage on the gate. This instantaneous gate voltage e_g can be expressed in terms of the peak oscillator signal voltage e_o, as follows:

$$e_g = -1 + e_o \sin \omega_o t \quad (5)$$

Substitution of Eq.(5) into Eq.(4) yields the following expression for transconductance:

$$g_m = 6.82 + 5.13\ e_o \sin \omega_o t - 2.39\ e_o^2 \sin^2 \omega_o t + 0.75\ e_o^3 \sin^3 \omega_o t \quad (6)$$

An expression for instantaneous drain current i_d in terms of Eq.(6) and the incoming signal e_s can then be written, as follows:

$$i_d = g_m\ e_s \sin \omega_s t \quad (7)$$

Expansion of Eq.(7) in terms of $e_o \sin \omega_o t$ and $e_s \sin \omega_s t$ and selection of those components which are effective at 10.7 MHz [i.e., sin $(\omega_o - \omega_s)t$ components] provides the following expression for drain current at the intermediate frequency:

$$i_{IF} = (2.57\ e_o + 0.28\ e_o)e_s \quad (8)$$

By definition, the conversion transconductance g_c is equal to the if current divided by the signal voltage, as follows:

$$g_c = i_{IF}/e_s \quad (9)$$

Therefore, g_c can be expressed in terms of the oscillator injection voltage e_o as follows:

$$g_c = (2.57 + 0.28)e_o \quad (10)$$

Because the magnitude of oscillator injection voltage e_o for the MOS FM tuner was selected to be 1 volt peak, the conversion transconductance is calculated to be

$$g_c = (2.57) + (0.28) = 2.85 \text{ mmhos}$$

By use of the same procedure, the conversion transconductance at a substrate bias of zero volts is calculated to be 2.29 millimhos. It is apparent that the application of a substrate bias provides an increase in conversion transconductance of more than 25 per cent.

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Design of Gate-Protected MOS Field-Effect Transistors

by L. A. Jacobus and S. Reich

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. [1,2] Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential build-up across the gate insulation.

Breakdown Mechanism

Before the techniques of gate protection can be applied, the breakdown mechanism associated with gate destruction must be understood. For the sake of simplicity in exploring the breakdown mechanism, a single-gate structure is used. Fig. 1 shows this single-gate structure (a), its electrical symbol (b), and a much simplified equivalent circuit (c) that explains the possible static discharge paths within the device. The substrate diode is formed by the p-n junction integrated over the entire junction area, i.e., the source and drain diffusions connected by the inversion layer or n-type channel. Fig. 1 (c) lumps the diffuse diode into one equivalent diode terminating at the center of the channel.

C_{IN} in Fig. 1(c) represents the gate-to-channel capacitance, and R_1 and R_2 represent the channel resistance. R_3 is the leakage resistance associated with the substrate-to-channel equivalent diode D_1. Leakage resistance across C_{IN} was intentionally deleted because it is more than a thousand orders of magnitude higher than R_3. In a typical RCA MOS field-effect transistor (e.g., 3N128), C_{IN} is less than 5 picofarads. The channel resistance $R_1 + R_2$, which is a function of the applied bias, can range from 10^2 to 10^{10} ohms. R_3 is also subject to variations determined by operating conditions, but can be assumed to be in the order of 10^9 ohms. Thus, the application of a dc potential between the gate and any other element results in practically all of this potential being applied across C_{IN}.

In a dual-gate MOS field-effect transistor, the oxide thickness of the C_{IN} dielectric is about 600 angstroms. The dielectric material is SiO_2, which has a breakdown constant of 5×10^6 volts per centimeter. The gate voltage-handling capability is therefore 30 volts. A cross-section of a typical RCA dual-gate device is shown in Fig. 2 (a), and its schematic symbol in Fig. 2(b). The substrate in this structure is internally tied to the source; this connection is also shown schematically by the dotted line in Fig. 1(c).

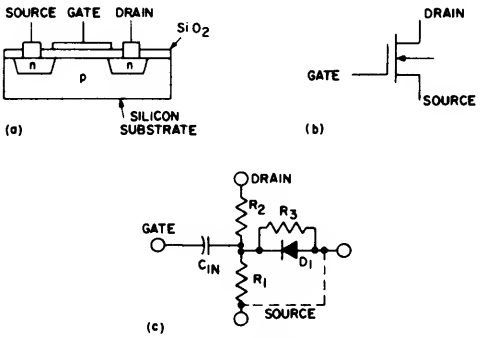


Fig. 1 - Single-gate MOS field-effect transistor: (a) structure; (b) electrical symbol; (c) simplified equivalent circuit.

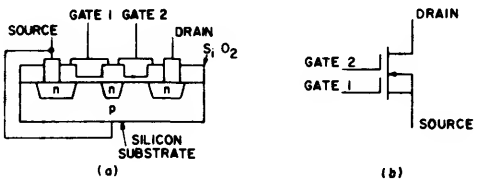


Fig. 2 - Dual-gate MOS field-effect transistor: (a) structure; (b) electrical symbol.

Static Discharge

If the potential applied to an MOS transistor were entirely within the control of the circuit designer, there would be no need for gate protection. Unfortunately, designers do not have complete control of the MOS field-effect transistor environment and static potentials do accumulate. These high potentials can inadvertently be discharged through the device when it is handled

during the equipment manufacturing cycle or by a receiving antenna associated with the end product in which the transistor is used. The more severe of these conditions, in terms of percentage of units that suffer damage, is probably the initial handling phase.

Fig. 3 shows a simple equivalent circuit of a static discharge generator as it appears at the input of an MOS transistor. E_S represents the static potential stored in the static generator capacitor C_D. This voltage must be discharged through internal generator resistance R_S. Laboratory experiments have determined that a human body acts as a static (storage) generator with a capacitance C_D ranging from 100 to 200 picofarads and a resistance R_S greater than 1000 ohms. Although there is

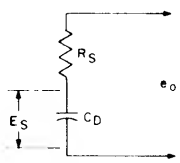


Fig. 3 - Equivalent circuit of a static discharge generator.

virtually no upper limit to the amount of static voltage that can be accumulated, repeated measurements suggest that the amount of potential stored is usually less than 1000 volts. Experience has also indicated that the potential from a static discharge is more severe during transistor handling than when the device is installed in a typical application. In an rf application, for example, a static potential picked up by the antenna would traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the input of the rf amplifier. For this reason, the development of gate-protected MOS transistors concentrated on the requirement that the devices be capable of withstanding the static discharges likely to occur during handling operations.

Gate-Protection Methods

It has been established above that in terms of a static discharge potential it is reasonable to represent the MOS transistor as a capacitor, such as C_{IN} in Fig. 4. The ideal situation in gate protection is to provide a signal-limiting configuration that allows for a signal such as that shown in Fig. 4(a) to be handled without clipping or distortion. The signal-limiting devices should limit all transient responses that exceed the gate breakdown voltage, as shown in Fig. 4(b). One possible means of securing proper limiting is to place a diode in parallel with C_{IN}, as shown in Fig. 4(c). Unfortunately, this arrangement causes several undesirable consequences. In terms of signal handling, the single diode clips the positive peaks of a sine wave such as that in Fig. 3(a) when the transistor is operated in the vicinity of zero bias. The 3N140 dual-gate MOS transistor, for example, is frequently operated with the rf signal superimposed on a slightly positive "bias" potential on gate No. 1. Furthermore, gate No. 2 of the 3N140 is designed to handle large positive and negative dc voltage swings from the agc loop. A single-diode arrangement would render this device useless for this type of circuit. It is important, therefore, that the limiting device be an effective open circuit to any incoming signals through the amplitude range of such signals. The best available method for accomplishing this effective open circuit is the back-to-back diode arrangement pioneered by RCA and shown in Fig. 3(d).

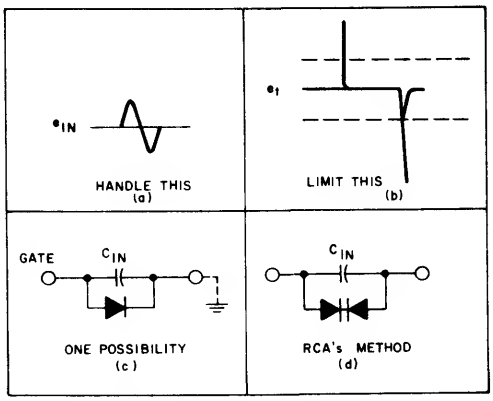


Fig. 4 - Gate-protection requirements and two solutions.

Ideally, the transfer characteristic of the protective signal-limiting diodes has an infinite slope at limiting, as shown in Fig. 5(a). Under these conditions, the static potential generator in Fig. 5(b) discharges through its internal impedance R_S into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, with an infinite transfer slope ($R_S = 0$), would then limit the voltage presented to the gates to its knee value, e_d. The difference voltage $E - e_d = e_S$ (where E is the static potential in the static generator, e_d is the diode voltage drop, and e_S is the voltage drop across the generator internal resistance) appears as an IR drop across R_S, the internal impedance of the generator. The instantaneous value of the diode current is then equal to e_S/R_S. During handling, the practical range of this discharge varies from several milliamperes to several hundred milliamperes.

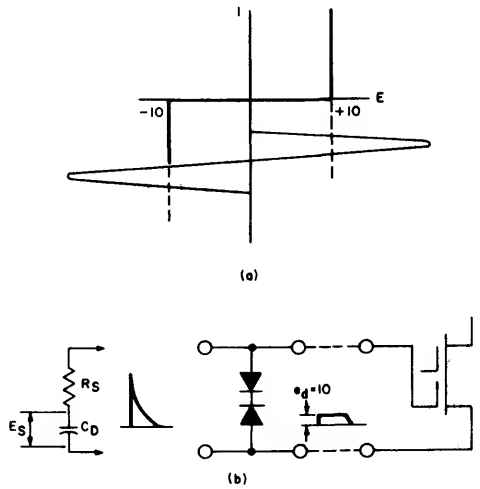


Fig. 5 - Transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).

Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the diode ideally adds no capacitance or loading to the rf input circuit.

The first phase in the development of gate-protected MOS field-effect transistors was, quite naturally, their construction in hybrid form. This form was used for initial measurements because it effectively enabled the physical separation of the diodes from the MOS pellet. This separation made it possible to measure the performance of the active device apart from the combined structure and thus obtain a more precise assessment of the loading effect of the diodes. The hybrid phase has now been followed by the development of monolithic gate-protected MOS field-effect transistors such as the RCA-40673. In this transistor, the diodes are an integral part of the MOS device and are internally connected as shown in Fig. 6.

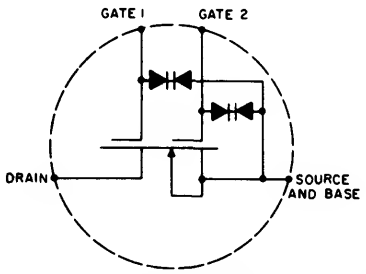


Fig. 6 - *Connection of integral protective diodes in dual-gate MOS transistor.*

Monolithic Gate-Protected MOS Transistors

In the design of a monolithic diode-protected MOS transistor, several factors must be taken into account. (1) The high-frequency performance of the device must be comparable to that of available unprotected units. (2) The device must be designed so that no additional assembly cost is incurred. (3) The silicon area must be used efficiently to provide the maximum number of devices per semiconductor wafer. (4) The diodes must provide adequate protection against the transients experienced primarily in handling but also when the transistor is finally installed in some piece of equipment.

One approach to integrating protective diodes into an MOS transistor structure on one chip is shown in Fig. 7. In this approach, the silicon substrate required for an n-channel depletion-type MOS device is the starting material. The n-type wells are diffused into the silicon to provide pockets for the protective devices. The surface concentration and depth of these wells are carefully controlled because both of these factors are important in determining diode characteristics.

The p^+-type regions are diffused into the n-type wells to form the diodes and around the periphery to isolate the diode structure from the surface of the MOS device and to provide a region into which the channels may be terminated. The size of the diodes is determined by the desired current-handling capability and the amount of capacitance that can be tolerated across the gate of the MOS transistor. The spacing of the diodes is determined by the area available and the desired amount of control of transistor action from diode to diode. After the diode structures are formed, they are covered by a protective oxide. The MOS device is then fabricated by conventional means.

Fig. 8 shows a photograph of a completed monolithic diode-protected dual-gate MOS transistor. In this structure,

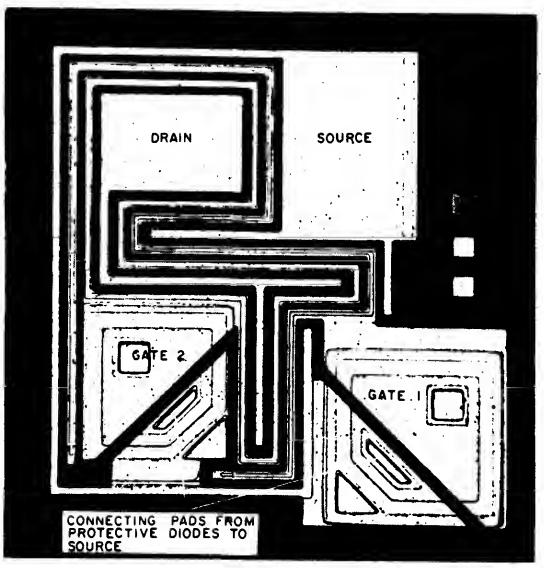


Fig. 8 - Completed monolithic diode-protected dual-gate MOS transistor.

one of the diodes of each pair has been located under the gate bonding pads. The small triangular metal pads

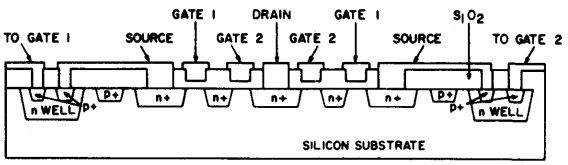


Fig. 7 - Structure of MOS transistor chip including protective diodes.

make contact with the second diode of each pair and connect it to the source metalization. In assembly, the source is shorted to the substrate so that a low-resistance path to ground is provided for the diodes. To ground the diodes under the second gate properly, it is necessary to break the metal of the first gate and terminate the first channel on the p^+-type guard band surrounding the diode structure of the second gate. This technique prevents spurious source-to-drain current which could result from the open nature of the structure.

Current-Handling Capability

Fig. 9 shows a typical diode transfer characteristic measured with a one-microsecond pulse width at a 4 x 10^{-3} duty cycle. The purpose of the protective diode is to limit the amplitude of the transient to a value that is below the gate breakdown voltage. Typically, a dual-gate transistor has a gate-to-source breakdown voltage rating of 20 volts. The curves in Fig. 9 show that the transfer characteristic of the signal-limiting diodes will constrain a transient impulse to potential values well below this 20-volt limit even when the input surge is capable of delivering hundreds of milliamperes.

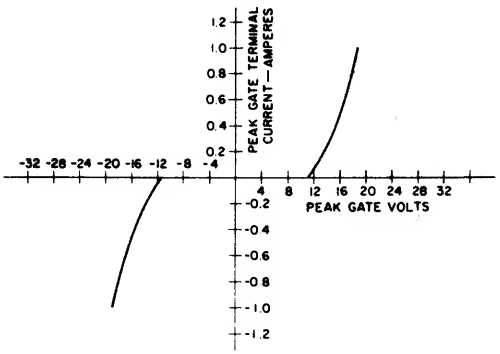


Fig. 9 - Typical diode transfer characteristic measured with 1-microsecond pulse width at 4 x 10^{-3} duty cycle.

The protection offered by the MOS signal-limiting diodes is more dramatically demonstrated when a gate-protected MOS transistor is compared to a high-frequency bipolar device. A laboratory experiment in which a static charge was accumulated in a capacitor and discharged through a circuit configuration like the one shown in Fig. 3 demonstrated that the special signal-limiting diodes made the protected-gate MOS field-effect transistor less vulnerable to static discharge damage than the bipolar transistor by a factor greater than two.

Input Capacitance and Resistance

The curves of input capacitance and input resistance as a function of drain current in Fig. 10 represent average readings taken from ten hybrid devices with diodes first connected and then disconnected (the readings for all ten devices were remarkably close to the averages). The curves indicate that the diodes increase input capacitance by about 2.5 picofarads and decrease input resistance by about 200 ohms.

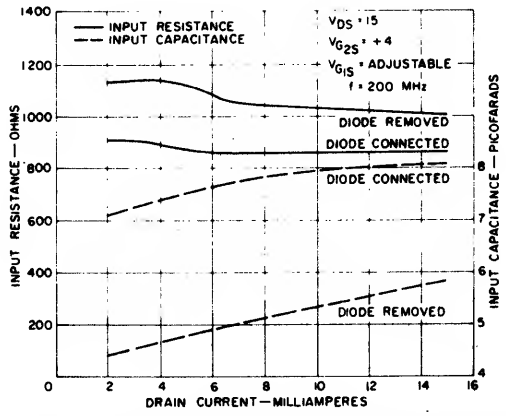


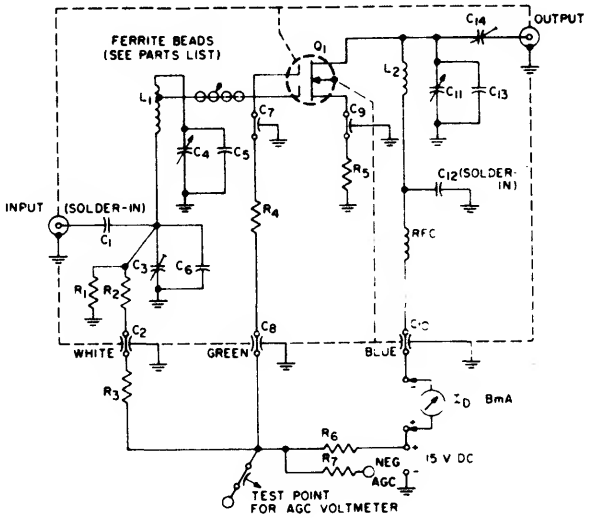
Fig. 10 - Input resistance and capacitances as a function of drain current for hybrid structures with and without diodes.

Power Gain and Noise Factor

In the final analysis, the question that must be answered is how the addition of the protective signal-limiting diodes affects circuit power gain and noise factor. Performance data taken on the ten units described above in the typical rf test circuit shown in Fig. 11 are given in Table 1. Noise-factor values show an average degradation of 0.25 dB when the diodes are connected. The power-gain values show that the change in this characteristic is insignificant.

Table 1 - Power Gain and Noise Factor at 200 MHz.

HYBRID UNIT	POWER GAIN (dB)		NOISE FACTOR (dB)	
	DIODES IN	DIODES REMOVED	DIODES IN	DIODES REMOVED
1	16.3	16.4	3.7	3.4
2	18.8	18.5	2.4	2.2
3	16.5	16.2	3.3	3.0
4	16.3	15.7	3.9	3.4
5	17.7	17.8	2.6	2.4
6	17.2	17.5	2.8	2.5
7	17.1	17.0	3.3	3.2
8	17.9	18.0	2.9	2.6
9	18.5	18.5	2.4	2.3
10	17.3	17.3	3.2	3.0



C_1: 100 picofarads, ceramic disc
C_2 C_7 C_8 C_9 C_{10}: 1000 picofarads, feed-through type
C_3: 1 to 10 picofarads, variable air (piston); JFD VAM-010, Johnson Co. No. 4335, or equivalent
C_4: 1.8 to 8.7 picofarads, variable air; Johnson Co. No. 160-104 or equivalent
C_5: 3 picofarads, tubular ceramic
C_6: 22 picofarads, ceramic disc
C_{11}: 1.5 to 5 picofarads, variable air; Johnson Co. No. 160-102 or equivalent
C_{12}: 100 picofarads, ceramic disc
C_{13}: 1.5 picofarads, tubular ceramic
C_{14}: 0.8 to 4.5 picofarads, variable air (piston); Erie 560-013 or equivalent
Ferrite beads: 4 beads on No. 24 wire between L_1 and socket; beads are Pyroferrio Co. "Carbonyl J" or equivalent: 0.093-inch OD, 0.03-inch ID, 0.063 inch thick
L_1: 4 turns 0.020-inch copper ribbon, silver-plated, 0.075 to 0.085 inch wide, 0.25-inch inside diameter, coil approximately 0.80 inch long
L_2: 4.5 turns 0.020-inch copper ribbon, silver-plated, 0.085 to 0.095 inch wide, 0.3125-inch inside diameter, coil approximately 0.90 inch long
Q_1: MOS transistor under test
RFC: Ohmite part No. Z235 or equivalent
R_1: 27,000 ohms
R_2: 47,000 ohms
R_3: 36,000 ohms
R_4: 1800 ohms
R_5: 275 ohms, ½ watt, 1%
R_6: 120,000 ohms
R_7: 1000 ohms

Fig. 11 - RF test circuit for dual-gate MOS transistors.

Conclusions

Gate-protected dual-gate MOS field-effect transistors such as the RCA-40673 make available to the circuit designer a device capable of good rf performance without the hazards previously associated with the handling and installation of MOS devices. Moreover, the gate protection is provided by signal-limiting diodes that do not significantly compromise dynamic range, noise factor, or power gain.

Acknowledgment

The authors thank L. Baar for collecting data and providing general support for the work described, and C. Tollin for fabricating the devices tested.

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AN-4125

MOSFET Biasing Techniques

by S. Reich

A wide variety of applications exist for field-effect transistors today including rf amplifiers and mixers, i-f and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits.

Several different FET structures have also evolved. The dual-gate metal-oxide-semiconductor FET, for example, appears particularly advantageous in rf stages because of low feedback capacitance, high transconductance and superior cross modulation with automatic-gain-control capability.

The rules for biasing FETs vary slightly depending upon the type of FET being applied. But we'll attempt to cover most of the possibilities by looking at several typical examples.

As you know, all FETs including junction devices, can be classified as depletion or enhancement types, depending upon the conductivity state of the channel at zero gate-to-source voltage or bias. In a depletion type, charge carriers are present and the channel is conductive when no bias is applied to the gate. Reverse bias depletes this charge and reduces channel conductivity; forward bias draws more charge carriers into the channel and increases conductivity. In an enhancement type, no useful channel conductivity exists at either zero or reverse gate bias; the gate must be forward-biased to produce active carriers and permit conduction through the channel.

Test circuits which can be used to measure the zero-bias drain current I_{DSS} of junction-gate and insulated-gate field-effect transistors are shown in Fig. 1. The junction-gate device, shown in Fig. 1(a), is always a depletion type and thus exhibits a reading for I_{DSS}. Insulated-gate or MOS devices may be either depletion or enhancement types; depletion types exhibit reasonable I_{DSS} readings in the circuit of Fig. 1(b), while enhancement types are cut off. The transistor symbol shown in Fig. 1(b) uses a solid channel line to indicate the "normally ON" channel of a depletion type. An enhancement type is represented by an interrupted channel line, that indicates the "normally OFF" channel.

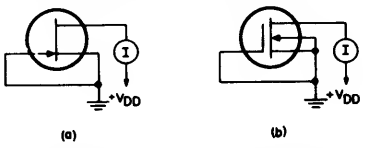


Fig. 1. I_{DSS} test circuits for (a) junction-gate and (b) insulated-gate field-effect transistors.

Although enhancement types are always operated (activated) in the enhancement mode (because application of reverse bias would simply cut the device off), depletion types can operate in either mode. Junction-gate devices can operate in the enhancement mode only within a very limited range because gate voltages exceeding 0.3 V also forward-bias the gate-to-source input diode and load the signal source. However, MOS depletion devices can operate in either the enhancement or the depletion mode without the constraints associated with input-diode loading.

The field-effect transistors shown in Fig. 1 are single-channel, single-gate, or triode-type devices. Although it is possible that the substrate of either the junction-gate or insulated-gate transistor may be used as a separate control element, in most circuits it is adequate as a control element and is extrinsically connected to the source or operated at a fixed potential.

When two separate control elements are required in a circuit, a dual-gate MOS transistor such as that shown in Fig. 2 is usually used. In this type of device, two independent gate electrodes that control individual channels are serially interconnected. In newer dual-gate MOS transistors, gate protection is provided by intrinsic back-to-back diodes, as shown in Fig. 2(b). The substrate in this type of device is in-

ternally connected to the source.

Biasing a single-gate MOS transistor

The bias circuit for a single-gate MOS transistor may take three forms, as shown in Fig. 3: (a) self-bias, (b) an external supply, or (c) a combination of the two. The design of a self-bias circuit is fairly straightforward. For example, if it is desired to operate a 3N128 MOS transistor (an n-channel, depletion device) with a drain-to-source V_{DS} voltage of 15 V and a

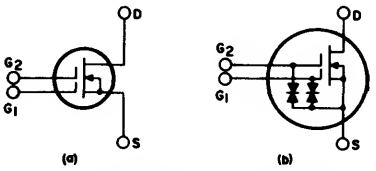


Fig. 2. Dual-gate MOS transistors. (a) conventional symbol, (b) modified symbol to show gate-protected device.

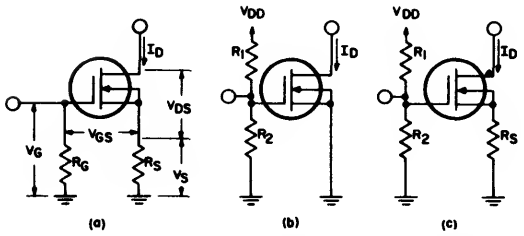


Fig. 3. Biasing circuits for single-gate transistors: (a) self-biasing; (b) external biasing; (c) a combination of self-biasing and external biasing.

small-signal transconductance g_{fs} of 7.4 mmhos, the drain current I_D required for the desired transconductance is first obtained from published transfer-characteristics curves such as those shown in Fig. 4(a). A published curve such as the one shown in Fig. 4(b) is then used to determine the gate-to-source voltage V_{GS} required for the desired value of I_D. The circuit parameters can then be calculated using $V_{DS} =$ 15 V, $I_D = 5$ mA, $V_{GS} = -1.1$ V and $V_G = 0$.

$$V_S = V_G - V_{GS} = 1.1 \text{ V} \quad (1)$$

$$R_S = V_S/I_D = 1.1/5 = 220\ \Omega \quad (2)$$

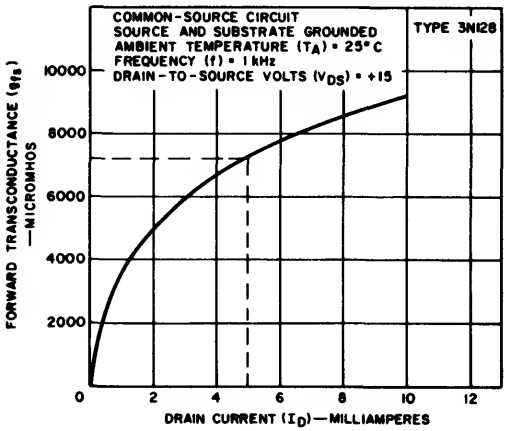
$$V_{DD} = V_{DS} + V_S = 15 + 1.1 = 16.1 \text{ V} \quad (3)$$

In a circuit designed for applied bias only, the problem becomes more complicated. For example, the voltage divider consisting of R_1 and R_2 in Fig. 3(b) may be required to apply a V_{GS} of -1.1 V. In addition to the fact that a negative supply is required, a more serious problem exists. The bias-voltage computations shown above were based on the solid-line curve shown in Fig. 4(b) for a typical device.

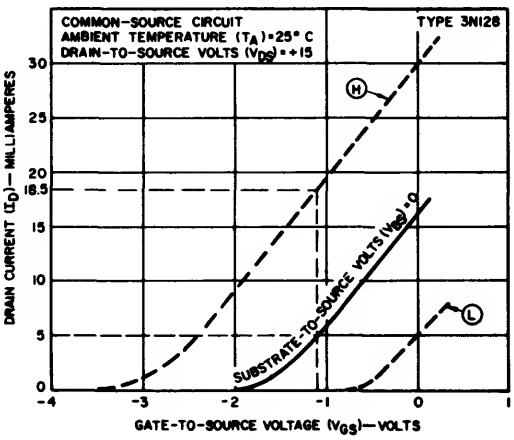
However, the drain currents for individual devices may cover a wide range of values, as indicated by the dashed curves H and L representing high- and low-limit devices, respectively. With a fixed-bias supply of -1.1 V, therefore, drain current could range from cutoff to 18.5 mA. Some form of dc feedback is obviously desirable to maintain the drain current constant over the normal range of product variation.

The combination bias method shown in Fig. 3(c) makes use of a larger value of R_S to narrow the range of drain current to plus or minus a few milliamperes. Figure 5 shows curves of I_{DSS} as a function of I_D for various values of R_S. The normal range of I_{DSS} for the 3N128 is from 5 to 25 mA, or a spread of 20 mA. The use of the 220-Ω source resistor R_S calculated in the previous example reduces this spread to about 5 mA, for a 4-to-1 improvement. Higher values of R_S achieve tighter control of the spread of drain-current values.

As an example, the circuit of Fig. 3(c) may



(a)



(b)

Fig. 4. (a) Transfer and (b) operating characteristics of the 3N128 single-gate MOS transistor.

be required to maintain drain current constant within ±1 mA for the same conditions given in the previous example. Figure 5 shows that a value of R_S equal to or greater than 1000 Ω will satisfy the required drain-current tolerance. However, a quiescent current of 5 mA through a source resistor of 1000 Ω produces a V_{GS} value of −5 V, which is incompatible with a drain current of 5 mA. Therefore, an applied bias must be used in conjunction with the self-bias. The circuit parameters for Fig. 3(c) are then calculated using $V_{DS} = 15$ V, $I_D = 5$ mA, $V_{GS} = -1.1$ V, and $R_S = 1000$ Ω.

$$V_S = I_D R_S = (0.005)\ (1000) = 5 \text{ V} \quad (4)$$

$$V_G = V_{GS} + V_S = -1.1 + 5 = 3.9 \text{ V} \quad (5)$$

$$V_{DD} = V_{DS} + V_S = 15 + 5 = 20 \text{ V} \quad (6)$$

$$\frac{V_{DD}}{V_G} = \frac{R_1 + R_2}{R_2} = \frac{20}{3.9} = 5.12 \quad (7)$$

The lower limits of R_1 and R_2 are established by determining the maximum permissible loading of the input circuit and setting this value equal to the parallel combination of the two resistors. For example, if the total shunting of the input circuit is to be no less than 50,000 Ω, R_1 and R_2 are calculated as follows:

$$\frac{R_1 R_2}{R_1 + R_2} = 50{,}000 \quad (8)$$

$$\frac{R_1 + R_2}{R_2} = 5.12 \quad (9)$$

$R_1 = 256{,}000$ Ω, and $R_2 = 62{,}000$ Ω.

In practice, the effects of input-circuit loading can frequently be eliminated by the use of the circuit arrangement shown in Fig. 5.

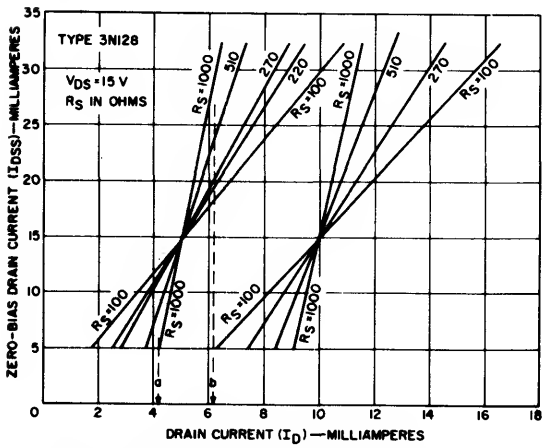


Fig. 5. Zero-bias drain current I_{DSS} as a function of drain current I_D for various values of source resistance R_S in a 3N128 single-gate MOS transistor.

The upper limits of R_1 and R_2 are usually determined by practical consideration of the resistor component values because the absolute values of gate-leakage current I_{GSS} are extremely small. In unique applications where I_{GSS} is a significant factor, a maximum value for the parallel combination of R_1 and R_2 can be determined by dividing the total permissible change in voltage V_G across the combination by the maximum allowable value of I_{GSS} at the expected operating temperature, as determined from the published data for the transistor used.

Because I_{GSS} consists of leakage currents from both drain and source, and these currents are usually measured with a maximum-rated voltage stress on the gate with respect to all other elements, the published value of I_{GSS} is generally much higher than that which could be expected under typical circuit conditions. As a result, the values of R_1 and R_2 determined in this manner are conservative.

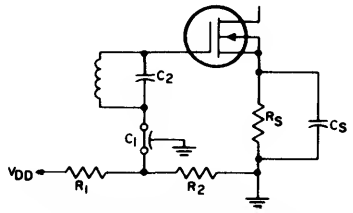


Fig. 6. Circuit used to eliminate input-circuit loading.

Substrate biasing

As mentioned previously, many single-gate FETs incorporate provisions for separate connection to the substrate because it is sometimes desirable to apply a separate bias to the substrate and use it as an additional control element. A simple arrangement for achieving this bias is shown in Fig. 7(a). In this circuit, the substrate bias V_{TS} is equal to $I_D (R_1 + R_2)$ and the gate bias V_{GS} is equal to $I_D R_1$.

One application in which substrate bias is mandatory is the attenuator circuit shown in Fig. 7(b). An MOS transistor is extremely useful as an attenuation device because it acts as a fairly linear resistance whose intrinsic conductivity can be drastically changed by means of a dc voltage applied to the gate. In the circuit of Fig. 7(b), for example, a signal applied

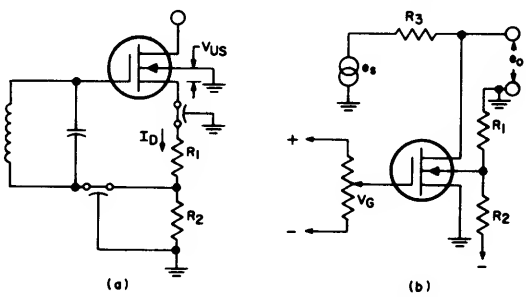


Fig. 7. Substrate biasing circuits.

to the drain can be attenuated by application of a positive voltage to the MOS transistor gate. The attenuation A_V obtained is given by

$$A_V = \frac{R_D}{R_D + R_s} \quad (10)$$

where R_D, the device channel resistance, is a function of bias voltage and can be varied from approximately 100 Ω to 10^5 MΩ. Because of the construction of the MOS transistor, however, the drain must always be positive with respect to the substrate so that the drain-to-source diode (diffusion) will not be biased into conduction. Therefore, the substrate must be back-biased to at least the peak value of the negative-going signal that might be applied to the drain. Figure 7(b) shows how this back-bias is obtained.

Biasing a junction-gate transistor

The biasing techniques that have been described for single-gate MOS transistors are directly applicable to junction-gate devices with one exception. Because the input gate of a junction-gate field-effect transistor consists of a back-biased diode, the device must always be biased so that the input-gate diode is not in conduction. Effectively, therefore, a junction-gate device will almost always be operated in the depletion mode.

Although the biasing considerations covered thus far are applicable to all types of single-gate transistors, it should be remembered that enhancement-type devices must be turned on before they can be used as amplifiers. Therefore, applied bias such as shown in Fig. 3(b) and 3(c) must always be used with these devices. In addition, it is desirable to narrow the range of drain current by means of a source resistor, such as that shown in Fig. 3(c), that produces self-bias after the transistor is turned on.

As an example of this type of biasing, it may be assumed that a 2N4065 p-channel enchancement-type MOS transistor is to be operated at room temperature with a supply voltage of 19 V, a source resistance of 1000 Ω, and a drain current of 1 mA, as shown in Fig. 8. To complete the bias circuit, it is necessary to determine the values of R_1 and R_2 to satisfy a total input-loading requirement of 10,000 Ω.

The 2N4065 transistor has a typical threshold voltage of −5.3 V and requires a gate voltage of approximately −9.2 V for a drain current of 1 mA. (The threshold voltage V_{TH} for an enhancement-type device is comparable to the cut-off voltage V_{GS} (OFF) for a depletion-type device, and is the value of gate voltage required to initiate drain current. It is usually specified for a drain-current value between 10 and 100 mA). Circuit parameters for the network of Fig. 8 are then calculated as follows:

$$V_S = I_S R_S = (-0.001)(1000) = -1 \text{ V} \quad (11)$$

$$V_{DS} = V_{DD} - V_S = -19 + 1 = -18 \text{ V} \quad (12)$$

$$V_G = V_{GS} + V_S = -9.2 - 1 = -10.2 \text{ V} \quad (13)$$

$$\frac{R_1 + R_2}{R_2} = \frac{V_{DD}}{V_G} = \frac{19}{10.2} = 1.86 \quad (14)$$

$$\frac{R_1 R_2}{R_1 + R_2} = 10{,}000\ \Omega \quad (15)$$

$$R_1 = 18{,}600\ \Omega \quad (16)$$

$$R_2 = 21{,}500\ \Omega \quad (17)$$

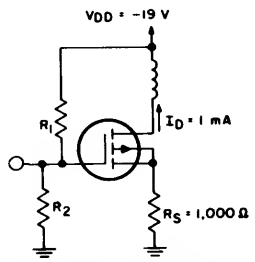


Fig. 8. Biasing circuit for an enhancement-type MOS transistor.

Biasing the dual-gate MOS transistor

A dual-gate MOS transistor such as that shown in Fig. 9(a) is actually a combination of two single-gate MOS transistors arranged in a cascode configuration, as depicted in Fig. 9 (b). The element voltages associated with each of the individual transistors can be analyzed as follows:

$$V_{DS} = V_{DS1} + V_{DS2} \quad (18)$$

$$V_{GS} = V_{DS1} + V_{GS2} \quad (19)$$

$$V_{G1S} = V_{GS1} \quad (20)$$

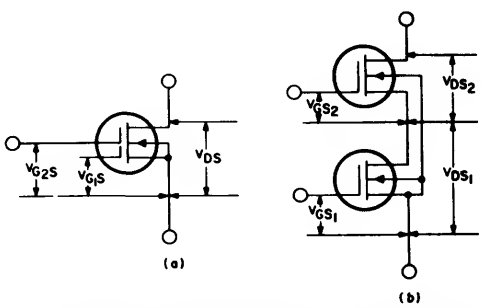


Fig. 9. Circuits showing element voltage associated with MOS dual-gate transistors.

Curves of the voltage distributions for the 3N140 dual-gate MOS transistor are shown in Fig. 10. It can be seen for an applied gate-No. 1-to-source voltage V_{G1S} of zero, a supply voltage V_{DD} of +15 V and a gate-No. 2-to-source volt-

age V_{G2S} of + 3 V ,the actual drain voltage across the grounded-source unit is approximately +2.75 V and gate No. 2 is 0.25 V positive with respect to its own source. These curves explain the logic behind the apparently high positive gate-No. 2 voltages (in the order of +4 V) recommended for typical operation of dual-gate MOS transistors.

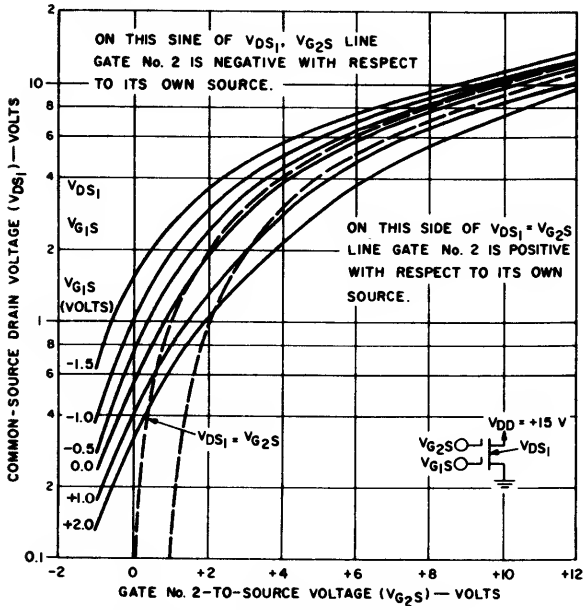


Fig. 10. Voltage distributions for the 3N140 dual-gate MOS transistor.

Operating curves for the 3N140 are shown in Fig. 11. These curves can be used to establish a quiescent operating condition for the transistor. For example, a typical application may require the 3N140 to be operated at a drain-to-source voltage V_{DS} of 15 V and a transconductance g_{fs} of 10.5 mmhos. As shown in Fig. 11(a), the desired value of g_{fs} can be obtained with a gate-No. 2-to-source voltage V_{G2S} of +4 V and a gate-No. 1-to-source voltage V_{G1S} of −0.45 V. From Fig. 11(b), the drain current compatible with these gate voltages is 10 mA.

Two biasing arrangements which can be used to provide these operating conditions for the 3N140 are shown in Fig. 12. For the application mentioned above, it may be assumed that shunt resistance for gate No. 1 should be 25,000 Ω and the dc potential on gate No. 2 should be fixed and at rf ground. The remaining parameters for the biasing circuits can then be obtained from the curves showing I_D as a function of R_S in Fig. 13, with $R_S = 270\ \Omega$:

$$V_S = I_D R_S = +2.7\ \text{V} \quad (21)$$

$$V_{G1} = V_{G1S} + V_S = +2.25\ \text{V} \quad (22)$$

$$V_{G2} = V_{G2S} + V_S = +6.7\ \text{V} \quad (23)$$

$$V_{DD} = V_{DS} + V_S = +17.7\ \text{V} \quad (24)$$

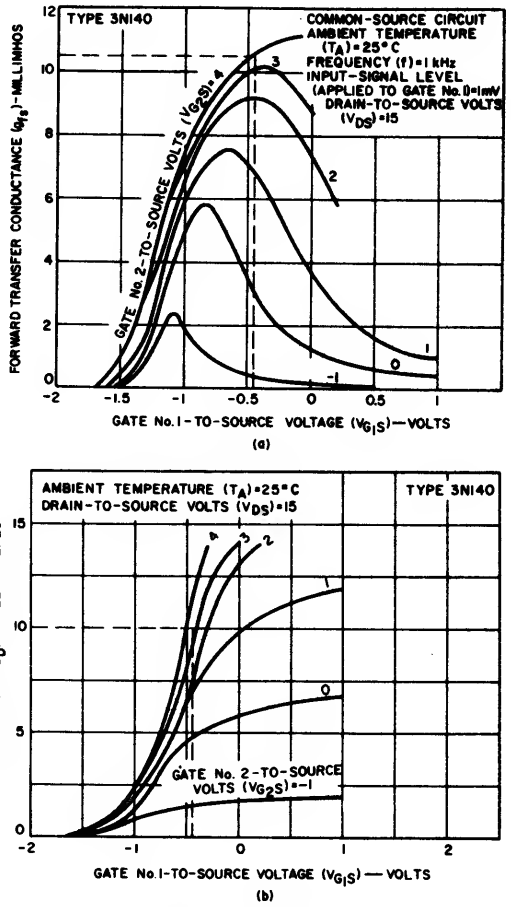


Fig. 11. Characteristics curves for the 3N140.

The values of the resistance voltage dividers required to provide the appropriate gate voltages are determined in the same manner as shown previously for single-gate transistors. For the circuit of Fig. 12(a), R_1 is 197,000 Ω, R_4 is 28,600 Ω, and $R_1 R_2 = 11/6.7$.

The circuit of Fig. 12(a) is normally used in rf-mixer applications and in rf-amplifier circuits which do not use agc. The circuit of Fig. 12(b) is recommended for the application of agc volt-

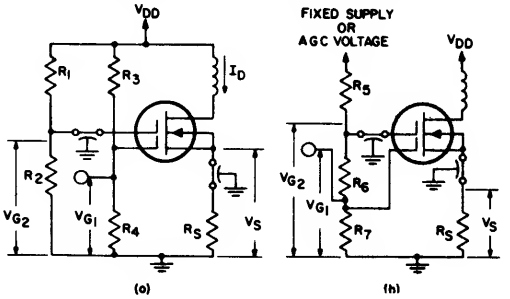


Fig. 12. Typical biasing circuits for the 3N140.

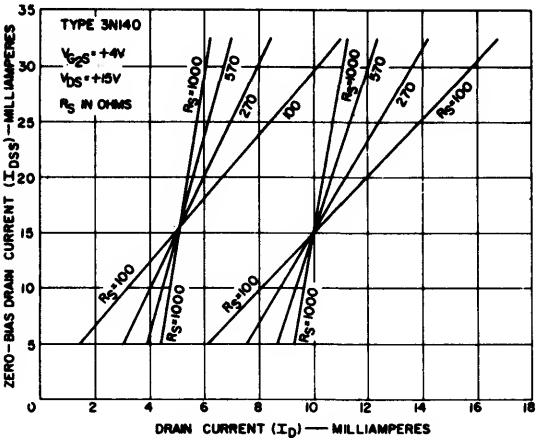


Fig. 13. Drain-current curves for various values of R_s for the 3N140.

age to rf-amplifier stages. In this circuit, the rf signal is applied to gate No. 1, and the agc voltage to gate No. 2.

The dual-gate MOS transistor is useful in agc-supplied rf amplifiers because almost no agc power is required by the device as a result of the high dc input resistance indigenous to the MOS transistor. Another advantage provided by the MOS transistor is revealed by the ease with which it obtains delayed agc action and good cross-modulation characteristics as a function of agc. The application of agc bias to gate No. 2 while the bias on gate No, 1 is changed improves the cross-modulation characteristics of the transistor as a function of agc applied.

Biasing to compensate for temperature variations

Unlike bipolar transistors, MOS transistors exhibit a negative temperature coefficient for typical values of drain current. That is, drain current and dissipation decrease as temperature increases, and there is no possibility of I_D runaway with elevated temperature. Unfortunately, transconductance and rf power gain also decrease as temperature increases. Figure 14 shows curves of drain current and transconductance as a function of temperature. These curves also show the compensating effects produced by the use of source resistance R_s; variations in drain current are reduced significantly by use of an R_s value of 1000 Ω.

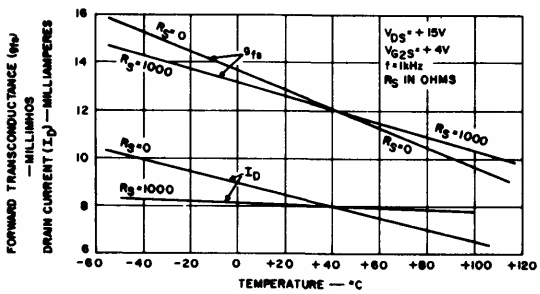


Fig. 14. Drain current and transconductance as a function of temperature for the 3N140.

Variations in transconductance can be virtually eliminated by application of a gain-control voltage from a temperature-dependent voltage-divider network to gate No. 2. For example, the values of the resistance voltage dividers in the circuit of Fig. 12(a) were determined to provide a transconductance of 9.5 mmhos at ambient temperature, and the device temperature was then varied through the range of −45 to +100°C. The values of gate-No. 2-to-source voltage V_{GSS} required to maintain a constant transconductance over the entire temperature range, for R_S values of zero and 1000 Ω are shown in Fig. 15.

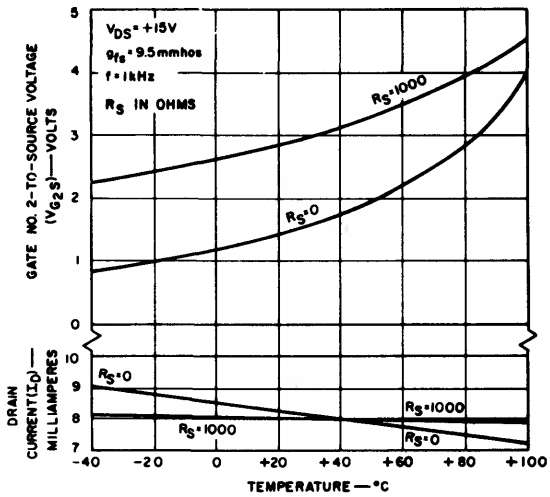


Fig. 15. Drain current and gate-No. 2-to-source voltage for constant I_D as a function of temperature for the circuit of Fig. 14 (b).

In a practical circuit, the required voltages can be applied to gate No. 2 if R_1, or the combination of R_1 and R_2, is a temperature-sensitive resistor that is thermally linked to the MOS transistor package. This thermistor network can be designed to provide a desired voltage characteristic at gate No. 2 either to keep the transconductance constant or to permit some variation with temperature to compensate for changes in other stages. The effects of temperature given in percentages on these other stages may be summarized as follows: R_{in}—one percent; C_{in}—one percent; $C_{feedback}$—one percent; R_{out}—plus 45 percent; C_{out}—one percent.

The data was measured on a 3N140 MOS transistor in the circuit of Fig. 12(a). Drain current was 8 mA, frequency was 200 MHz, and the temperature varied from 0 to 100°C.

Summary

All field-effect transistors may be biased similarly. Uniform quiescent operating points can be easily achieved in MOS field-effect transistors by employing circuit designs that incorporate a source resistance. For a given I_{DSS} range, the value of the source resistance inversely affects the in-circuit I_D spread. An increase in the value of the source resistance minimizes variations in I_D as a function of temperature. The dual-gate MOS field-effect transistor is ideally suited for use in gain-controlled stages; dual-gate transistor biasing can provide various types of agc action including temperature compensation to assure constant output. **EEE**

Acknowledgements

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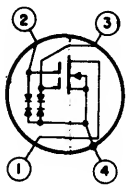
RF Applications of the Dual-Gate MOS FET up to 500 MHz

by L. S. Baar

The RCA dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in RF amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in RF applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

Gate-Protection Diodes

Fig. 1 shows the terminal diagram for the 3N200. Gate No. 1 is the input signal electrode and Gate No. 2 is normally used to obtain gain control. The back-to-back diodes are connected from each of the gates to the source terminal, lead No. 4. If short duration pulses greater than ±10 volts, generated for example by static discharge, are inadvertently applied to either gate, the protective diodes limit these voltages and shunt the current to the source terminal. Thus the gates, under normal operating conditions, are protected against the effects of overload voltages.[1]



LEAD 1 - DRAIN
LEAD 2 - GATE NO. 2
LEAD 3 - GATE NO. 1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE

Fig. 1 – Terminal diagram for the 3N200.

Operating Conditions

Typical two-port characteristics at 400 MHz including both "y" and "s" parameters, are given for the 3N200 in the RCA technical bulletin, File No. 437. This note makes use of the "y" parameters; however, designers who prefer the alternate method can, by parallel analysis, make use of the "s" parameters.

A recommended operating drain current (I_D) for the 3N200 is approximately 10 milliamperes with Gate No. 2 sufficiently forward biased such that a change in the bias voltage does not greatly affect the drain current. An adequate Gate No. 2-to-source voltage (V_{G2S}) is approximately +4 volts. The forward transadmittance (y_{fs}) increases with drain current, but saturates at higher current levels. The increase in RF performance at drain currents above 10 milliamperes is achieved only with less efficient use of input power.

To establish the optimum operating conditions for a type, consideration must be given to the range of variations in characteristics values encountered in production quantities of the type.[2] One important measure of type variation is the range of zero bias drain current (I_{DS}). The current range given in the 3N200 technical bulletin for I_{DS} is from 0.5 mA to 12 mA. A fixed bias condition intended to center the range of drain current at the desired level, still will produce an operating drain current range of 11.5 milliamperes with a resultant wide range of forward transconductance (g_{fs}). The drain current can be regulated by applying dc feedback with a bypassed source resistor (R_S). A good approximation of R_S (where $I_{DQ} \geq I_{DS}/2$) can be calculated by the use of the following formula*, assuming that V_{G1S} vs. I_{DS} is linear over the current range under consideration:

$$R_S \approx \left(\frac{1}{g_{fs(min.)}}\right)\left(\frac{\Delta I_{DS}}{\Delta I_{DQ}} - 1\right) \qquad \text{Eq. 1}$$

*See Appendix

where:

ΔI_{DS} is the current range given in the 3N200 technical bulletin

ΔI_{DQ} is the desired range of operating current

g_{fs}(min.) is the minimum forward transconductance at 1000 Hz

With the value of R_S established, then the Gate-No. 1 Voltage (V_{G1}) can be calculated from the equation

$$V_{G1} = V_{G1S} + I_{DQ} R_S \qquad \text{Eq. 2}$$

where V_{G1S} is estimated by:

$$V_{G1S} \approx \frac{I_{DQ} - I_{DS}}{g_{fs}(\text{avg.})} \qquad \text{Eq. 3}$$

where:

g_{fs}(avg.) is the average forward transconductance

To establish the Gate-No. 2 Voltage (V_{G2}), follow the same procedure described for calculating the Gate-No. 1 Voltage, except that a fixed V_{G2S} of approximately 4 volts is adequate.

If gain control is desired, apply a negative-going voltage to Gate No. 2. Because Gate No. 2 has little control in the voltage range of +2 to +5 volts, this characteristic may be used to effect AGC delay of the device in order to maintain the low noise figure until the RF signal is out of the noise-leve range.

Stability Considerations

Typical "y" parameter data as a function of frequency are given in Table 1. Maximum available gain (MAG) calculated from these data are also included to indicate ideal gain performance (i.e., $y_{rs} = 0$). The ability of the MOS FET to approach these gain levels depends on the device maintaining stable performance at the required operating frequency.

There are several methods which may be used to test for gain vs. stability. One of these methods, the Linvill Criteria (C), is defined by the equation:

$$C = \frac{y_{rs}\, y_{fs}}{2g_{is}\, g_{os} - R_e\, (y_{rs}\, y_{fs})} \qquad \text{Eq. 4}$$

A value for C which is less than 1 indicates unconditional stability. Applying the 400-MHz values taken from Table 1 to the Linvill Criteria yields a value of C = 0.615; substantially less than the value indicating unconditional stability.

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 100	200	300	400	500	UNITS
y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-15.0	-25.0	-35.0	-47.0	-60.0	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.4	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	-60.0	-25.0	0	14.0	20.0	degrees
Maximum Available Gain	MAG	32.0	24.0	17.5	13	10.0	dB

Table 1 -- "y" Parameters from 100 to 500 MHz

The following equation for Maximum Usable Gain $(MUG)^3$ is:

$$MUG = \frac{2K \left| y_{fs} \right|}{\left| y_{rs} \right| (1 + \cos \theta)} \qquad \text{Eq. 5}$$

where:

$\theta = \angle y_{fs} + \angle y_{rs}$

K = skew factor

$\angle y_{rs}$ = angle of reverse transadmittance

$\angle y_{fs}$ = angle of forward transadmittance

The skew factor, introduced in this equation, is a safety measure that establishes an arbitrary degree of skewing in the frequency response which may be introduced by regeneration. A value of 0.2 for K has been established on the basis of past experience. The value of MUG calculated at 400 MHz is 13.8 dB. This value of MUG is greater than the value of MAG, again indicating unconditional stability, since MAG, ignoring inherent feedback, is the conjugately matched gain. Therefore, neutralization or circuit loading is not required to insure stable performance, and the gain can approach MAG, limited only by circuit losses.

Reverse transadmittance (y_{rs}) is composed of several components, but the major ones are feedback capacitance (C_{rss}) and source-lead inductance (L_S). Therefore, care must be exercised in the application of the y_{rs} values, shown in Table 1, at the upper end of the usable frequency range. The 3N200 utilizes a JEDEC TO-72 package that has 4 leads. The data in Table 1 was compiled with the use of a socket which contacts the leads of the 3N200 as close as possible to the bottom of the package as specified by the JEDEC Standard Proposal SP-1028 "Measurement of VHF-UHF "y" Parameters". The leads are shielded from each other to eliminate stray capacitance between the leads, but some lead inductance is inevitable. If the device is soldered directly to the circuit components using commercial production techniques rather than by precise laboratory methods, then additional source lead inductance can be expected. Also, some additional capacitive coupling may result if the input and output circuits are not completely isolated from each other.

Because the published y_{rs} value for the 3N200 is very small, the circuit y_{rs} values may differ significantly from the y_{rs} values shown in Table 1 and hence, may result in an unstable operating condition. It is impossible to provide data for all possible mounting combinations, therefore, a recommended mounting arrangement is shown in Fig. 2. The source and substrate in the T0-72 package of the 3N200 are internally connected to lead No. 4 and the case. The source-lead inductance can be reduced, if the case is used as the source connection. Fig. 2 illustrates a partial component layout in which the case is held by a clamp or other fingered device. The clamp is soldered to a feedthrough capacitor to provide an effective, very-low inductance bypass to RF signals. This mounting arrangement still permits the use of a source resistor for DC stability, and enables the case to provide isolation between the input and output circuit in addition to the isolation afforded by the shield.

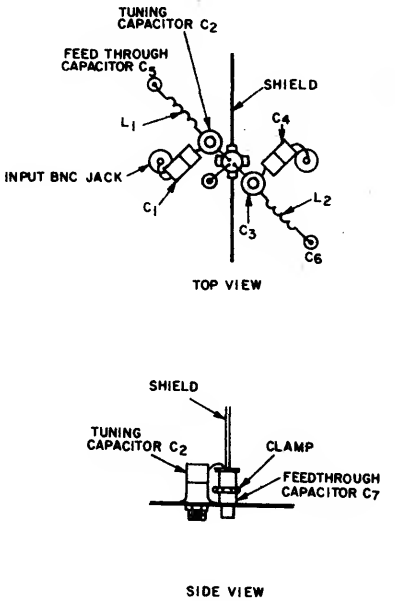


Fig. 2 – Partial component layout of 400-MHz amplifier circuit

The reduction of source-lead inductance provides in addition to greater stability, a lower input and output conductance. Table 2 shows the differences in "y" parameter values at 400 MHz when measured with the source connection made to lead No. 4 (in accordance with the published data for the 3N200) and when measured with the case connected directly to the ground plane of the test jig. The magnitude of reverse transadmittance is halved with a significant change in its phase angle. The input conductance is reduced by 30%, and the output conductance is reduced by 13%. A recalculation of the expressions for MAG, MUG, and Linvill Criteria (C) shows a significant improvement in gain and circuit stability.

While it is difficult to provide accurate information on the effects of shielding between the input and output circuits, its effect can be demonstrated when all other feedback components have been reduced to negligible values. The circuit, shown in Fig. 3 (for component layout see Fig. 2), was measured both with and without a shield. The maximum gain, without the shield, averaged 0.8 dB lower than with the use of the shield.

When receiver sensitivity is an important consideration in the design of an RF amplifier, a compromise must be made in the circuit power gain to achieve a lower noise

CHARACTERISTICS	SYMBOL	FREQUENCY (f) = 400 MHz		UNITS
		Normal Connection	Case Grounded	
Maximum Available Power Gain	MAG	13.0	15.7	dB
Maximum Usable Power Gain (unneutralized)	MUG	13.8	19.4	dB
Linvill Stability Factor, C	C	0.615	0.335	mmho
"y" Parameters				
Input Conductance	g_{is}	3.6	2.5	mmho
Input Susceptance	b_{is}	11.2	11.7	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.5	15.5	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-47.0	-40.0	degrees
Output Conductance	g_{os}	0.8	0.65	mmho
Output Susceptance	b_{os}	4.25	4.25	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.14	0.07	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	14.0	49.0	degrees

Table 2 – "y" Parameters at 400 MHz with source connection to lead No. 4 and with case connected to ground plane of test jig

factor. A contour plot of noise figure as a function of generator source admittance is shown in Fig. 4. Each contour is a plot of noise figure as a function of the generator source conductance and susceptance. Data for the noise figure were obtained from a test amplifier designed with very low feedback. Even though the area of very low-noise figure in the curves in Fig. 4 cover a broad range of source admittance, impedance-matching for maximum power gain could result in a relatively poor noise figure. As shown in Table 2, the input conductance (g_{is}) with the case grounded is 2.5 mmho. With the reactive portion tuned out, the noise factor at power matched conditions is almost 1 dB higher than the optimum noise figure. However, matching to 5.0 mmho results in a near optimum noise factor with a loss of only 0.5 dB in gain. In addition, impedance matching to high conductance

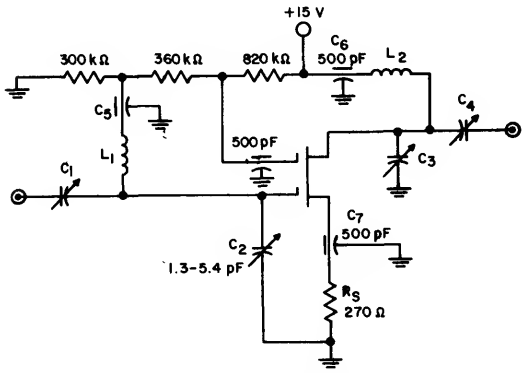


Fig. 3 – 400-MHz amplifier circuit

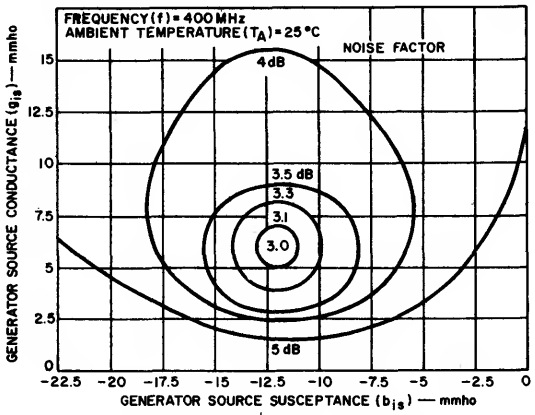


Fig. 4 – Noise factor vs. generator source (input) admittance (yis)

also benefits crossmodulation performance, as will be discussed in a later section.

Gate Protection Diodes

The diodes incorporated into RCA dual-gate MOS FETs, for gate protection, have been designed to minimize RF loading on the input circuits. The small amount of RF loading results in only a fraction of a dB loss in power gain and a negligible increase in the noise figure. The advantages of diode protection, greatly outweigh the slight loss in power gain, especially in an RF amplifier intended for the input stage of a receiver.

In addition to the protection afforded in normal handling, the diodes also provide in-circuit protection against events such as: static discharge due to contact with the antenna, delay in transmit-receive switching, or connection of an antenna with an accumulated charge to the receiver.

Crossmodulation

Crossmodulation is an important consideration because it is an inherent device characteristic where circuit considerations are secondary. Crossmodulation is the transfer of modulation from an undesired signal on a desired signal caused by the non-linear characteristics of a device.

Crossmodulation is proportional to the third-order term of the expansion of the I_D - V_{GS} curve. It is normally specified as the undesired signal voltage required to produce a crossmodulation factor of 0.01. The crossmodulation factor is defined as the percent modulation on a desired carrier by the modulated undesired signal divided by the percent modulation of the undesired signal.[4]

Inspection of the I_D - V_{G1S} curve of Fig. 5 offers an insight to the possible crossmodulation as a function of gain-reduction performance. When both channels of the 3N200 are fully conducting current, as shown by the V_{G2S} = 4-volt curve, the device approximately follows a square-law characteristic. If the I_D - V_{G1S} curve was ideal, the third-order term would be zero; but in practical cases, the

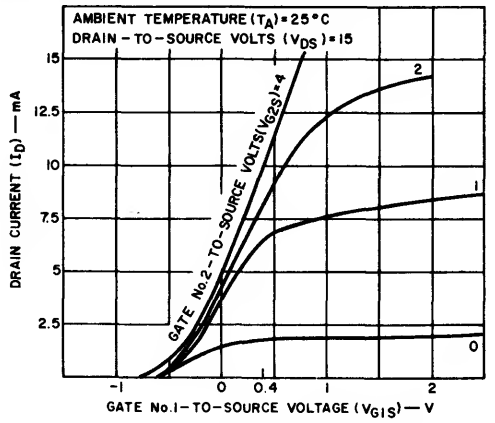


Fig. 5 – Drain current (I_D) vs. gate No. 1-to-source voltage (V_{G1S})

third-order term and crossmodulation have some low values. When the gain is reduced, by the application of bias to Gate No. 2, the square-law characteristic changes to a curve with a knee. Sharp curvatures usually result in larger high-order terms and poorer crossmodulation performance can be expected at lower gain conditions. If in Fig. 6, Circuit A, we assume a fixed bias (V_{G1S}) of approximately +0.4 volt, then the expected variation in crossmodulation is determined at the points where the ordinate at V_{G1S} = +0.4 volt crosses the curves. Crossmodulation performance at values of V_{G2S} = +4 volts to cutoff is as follows: good (low crossmodulation) at +4 volts, poorer at +2 volts, poorest at +1 volt, and again improves from zero volts to cutoff.

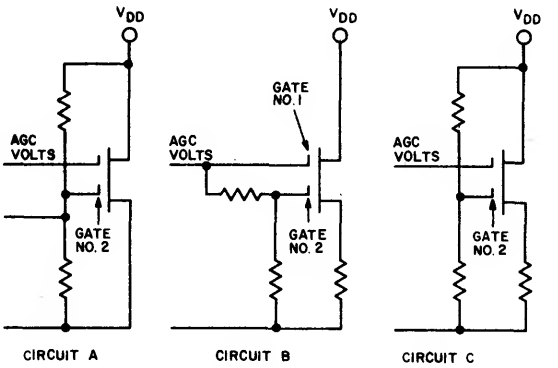


Fig. 6 – Biasing circuits using the 3N200

Curve A, Fig. 7 shows a curve of the undesired signal with a crossmodulation factor of 0.01 as a function of gain reduction. The curve indicates performance is poorest when gain reduction is in the 3- to 15-dB region; this region represents a Gate No. 2-voltage range of approximately 0.5 volt to 2 volts. The exception to the poor crossmodulation perform-

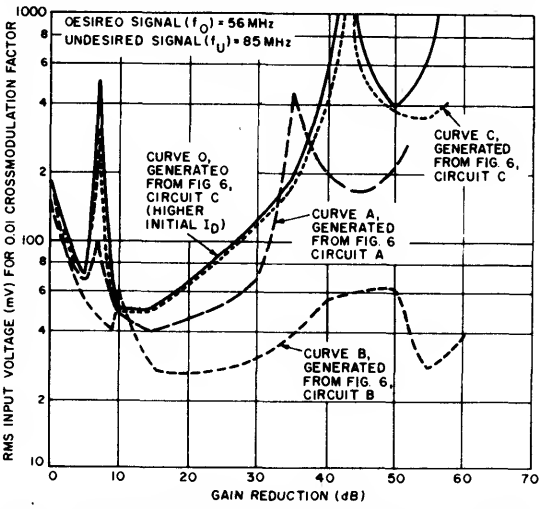


Fig. 7 – Crossmodulation vs. gain reduction using biasing circuits shown in Fig. 6

ance in this range is the sharp peak which occurs at the 5-dB level and is due to a curve inversion that takes place just prior to the knee. Beyond the 15-dB level, crossmodulation generally shows an improvement.

If Gate No. 1 is also reverse biased in conjunction with Gate No. 2 in the manner shown in Fig. 6, Circuit B, then the overall performance is poorer because the Gate No. 1 voltage will tend to follow the knee of each curve. This occurrence is evident in Fig. 7, Curve B. If Gate No. 1 is biased as shown in Fig. 6, Circuit C, the Gate No. 1-to-Source voltage intercepts the Gate No. 2 curves where the curvature is less severe, indicating as shown by Fig. 7, Curve C an improvement in crossmodulation performance. A further slight improvement is possible by the use of a higher initial operating drain current, which effectively moves the intercepts to the right on each curve. This improvement is indicated in Fig. 7, Curve D.

The curves in Fig. 7 establish that the biasing arrangement which provides optimum crossmodulation performance is the one in which Gate No. 1 forward bias increases as Gate No. 2 controls the gain. This biasing arrangement is easily accomplished by the use of a fixed Gate No. 1 voltage and a source resistor. As the Gate No. 2 bias voltage reduces the drain current, there is also a decrease in source voltage and an increase in the Gate No. 1-to-Source voltage. The gate-to-source voltage ratings must not be exceeded under any circumstances.

Summary

An RF amplifier, ideally, should provide high gain, a low-noise figure, and low crossmodulation. The 3N200 offers a good compromise in providing these three features. As indicated in the section on "Stability Considerations" a mismatch at the circuit input to a higher conductance level, provides an improved noise figure. The same mismatch condition also improves crossmodulation performance. The input signal at the gate of the device, when mismatched as indicated above, is lower than if it is power matched. The same ratio applies to any undesired signal and, thus, reduces the possibility of crossmodulation interference.

Appendix

The drain current of a device is established by the relationship

$$I_D = g_{fs} V_{G1S} + I_{DS}$$

where:

I_{DS} = drain current

at:

$V_{G1S} = 0$, $V_{G2S} = +4$ volts.

If a source resistor is used, as shown in Fig. A1, the gate No. 1-to-source voltage is

$$V_{G1S} = V_{G1} - I_D R_S$$

then

$$I_D = g_{fs} (V_{G1} - I_D R_S) + I_{DS} \quad \text{or}$$

$$I_D = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}}{1 + g_{fs} R_S}$$

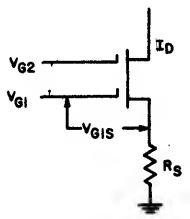


Fig. A1 – Bias circuit using the 3N200

The typical curves in Fig. A2 show drain current vs. Gate No. 1-to-Source Voltage as a function of I_{DS} level. These curves are almost linear when the typical operating drain current is in the 10-milliampere region. For the remainder of the analysis a linear relationship will be assumed for the required range of quiescent current. The assumption of linearity dictates that g_{fs} is a constant.

The required range of drain current is $I_{D2} - I_{D1}$

where:

$$I_{D2} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{max.})}{1 + g_{fs} R_S}$$

$$I_{D1} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(\text{min.})}{1 + g_{fs} R_S}$$

$$\Delta I_D = I_{D2} - I_{D1} = \frac{I_{DS}\,(\text{max.}) - I_{DS}\,(\text{min.})}{1 + g_{fs} R_S} = \frac{\Delta I_{DS}}{1 + g_{fs} R_S}$$

Solving the above equation for R_S gives

$$R_S = \frac{(\Delta I_{DS}/\Delta I_D) - 1}{g_{fs}}$$

where:

g_{fs} is equal to the expected minimum value at the required I_D

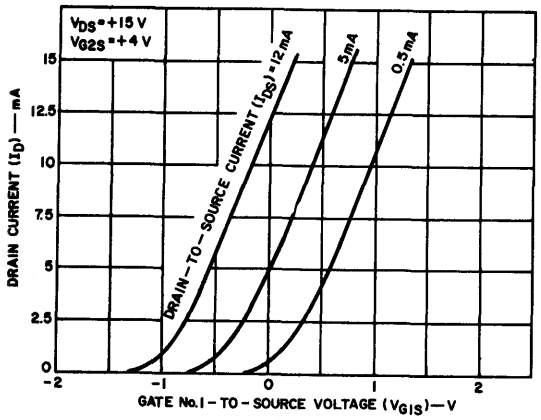


Fig. A2 – Drain current vs. gate No. 1-to-source voltage

References:

1. L. A. Jacobus and S. Reich, "Design of Gate-Protected MOS Field-Effect Transistors", RCA Application Note AN-4018
2. S. Reich, "Field-Effect Transistor Biasing Techniques", EEE, Sept. 1970
3. R. A. Santilli, "RF and IF Amplifier Design Considerations", IEEE Transactions on Broadcast and TV Receivers, Nov. 1967
4. H. Thanos, "Crossmodulation on Transistorized TV Tuners", IEEE Transactions on Broadcast and TV Receivers, Vol. 9 No. 3, Nov. 1963

AN-4590

Using MOS FET Integrated Circuits in Linear Circuit Applications

by S. Reich

Although the discrete metal-oxide-semiconductor (MOS) field-effect transistor (FET) has been available for many years,[1] its usage has been comparatively limited. Designers have been reluctant to employ MOS FET devices in their circuits because the gate oxide in a discrete device is vulnerable to damage by static electricity discharges encountered during handling and/or electrical transients found in circuit applications. RCA engineers have now successfully combined MOS FET and integrated-circuit (IC) fabrication techniques to produce a simple monolithic MOS FET IC in which back-to-back diodes are connected in shunt with the gate oxide to restrict the gate potential appearing across the gate oxide. The simple gate-protected IC's are of major significance because their immunity to damage by static electricity or by in-circuit transients is on a par of excellence with that of other solid-state devices intended for similar types of applications. Consequently, circuit designers can now practically utilize the many unique MOS FET characteristics, viz., high input impedance, square-law transfer characteristic, wide dynamic range, dual-gate configuration, etc. For example, the square-law transfer characteristic is especially desirable in the maintenance of low cross-modulation characteristics in rf amplifiers.[2,3] This paper contains a brief review of the device theory, followed by a survey of some linear circuit applications for the MOS FET IC.

REVIEW OF DEVICE THEORY

The operating voltage applied to the MOS FET determines whether the device will function as a resistor, an amplifier, or a diode. This section will provide a review of these various MOS FET operational modes. Subsequently, the useful operational modes will be employed in typical applications.

Fig. 1 is a sketch, for zero gate-to-source voltage, of I_D as a function of V_{DS} for an n-channel depletion-type MOS FET. Changes in the conductivity pattern are shown in the simplified conductivity profile for each region of operation.

Ohmic – Region 'A' depicts an I_D-V_{DS} curve that is characteristic of a resistance. The shape of this curve is a function of V_{DS} (drain-to-source voltage). Its slope is governed by V_{GS} (gate-to-source voltage). The V_{DS}/I_D characteristic i.e., its resistance value, is controlled by the gate voltage.

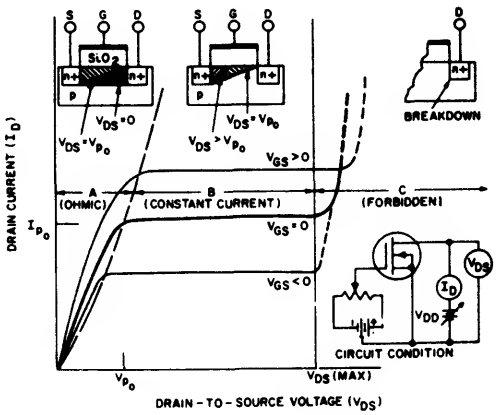


Fig. 1–Regions of operation – n-channel depletion MOS FET.

As V_{DS} is increased, it produces an electrostatic stress in the channel that modifies the channel conductivity as shown. The channel is completely pinched off beyond V_{Po} (pinch-off voltage). Increasing V_{DS} serves only to maintain I_D at a constant level.

Amplifier[4] – For a fixed gate-voltage, I_D is at a constant level in region 'B'. A change in V_{GS} produces a change in I_D; thus in region 'B' the device exhibits the transconductance characteristic that is essential in amplifier operation (i.e., $G_m = dI_D/dV_{GS}$).

"Forbidden" Region – Increase of V_{DS} beyond its rated maximum could produce avalanching in the drain-to-substrate diffusion (diode). Therefore MOS FET devices should not be operated in this region.

The dual-gate device is a serial arrangement of two single-gate devices. This arrangement improves the MOS FET performance by reducing capacitance from output to input (drain to gate 1), and provides an added control element that adds to the versatility of the MOS FET.

Gate Protection

A gate-protection system, which can be incorporated as an integral part of the transistor structure, has been developed for dual-gate MOS transistors. In devices that include this protection system, a set of back-to-back diodes is fabricated on the semiconductor pellet and connected between each insulated gate and the source. (The low junction-capacitance of the small diodes represents a relatively insignificant addition to the total capacitance that shunts the gate.) Fig. 2 is a profile drawing and schematic symbol for an n-channel dual-gate-protected depletion-type MOS field-effect transistor. The MOS FET IC metallization pattern, including the connections to the drain, gate 1, gate 2, source, and protective devices, all on a single monolithic structure, is shown in Figure 3.

The back-to-back diodes do not conduct unless the gate-to-source voltage exceeds typically ±10 volts. The transistor, therefore, can handle a very wide dynamic signal swing without significant conductive shunting effects by the diodes (leakage through the "nonconductive" diodes is very low, typically 1 na). If the potential on either gate exceeds typically +10 volts, the upper diode (shown in Fig. 2) of the pair associated with that particular gate becomes conductive in the forward direction and the lower diode breaks down in the backward (Zener) direction. In this way, the back-to-back diode pair provides a path to shunt excessive positive charge from the gate to the source. Similarly, if the potential on either gate exceeds typically -10 volts, the lower diode becomes conductive in the forward direction and the upper diode breaks down in the reverse direction to provide a shunt path for excessive negative charge from the gate to the source. The diode gate-protection technique is described in more detail in the following section on integrated gate protection.

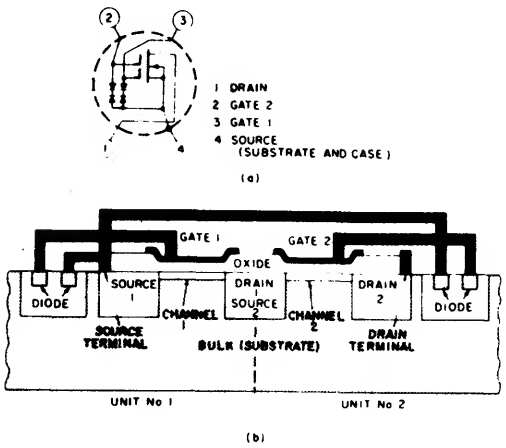


Fig. 2–Protected dual-gate MOS FET IC: (a) schematic diagram; (b) profile sketch.

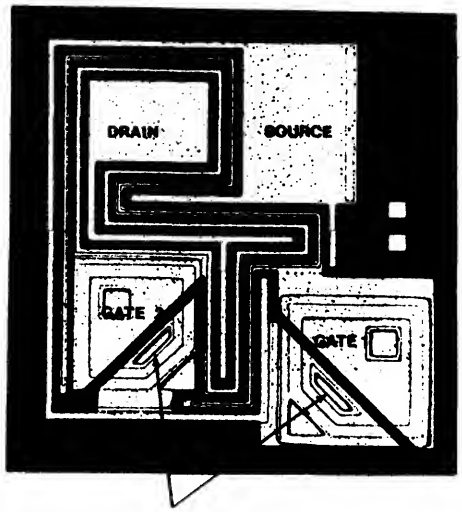


Fig. 3–Monolithic protected dual-gate MOS FET IC.

Integrated Gate Protection

The advent of an integrated system of gate-protection in MOS field-effect transistors has resulted in a class of solid-state devices that exhibits ruggedness on a par with other solid-state rf devices. The gate-protection system mentioned in the preceding section offers protection against static discharge during handling operations without the need for external shorting mechanisms. This system also guards against potential damage from in-circuit transients. Because the integral gate-protection system has provided a major impact on the acceptability of MOS field-effect transistors for a broad spectrum of applications, it is pertinent to examine the rudiments of this system.

Fig. 4 shows a simple equivalent circuit for a source of static electricity that can deliver a potential e_O to the gate input of an MOS transistor. The static potential E_S stored in

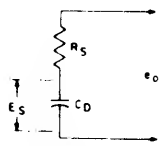


Fig. 4–Equivalent circuit for source of static electricity.

an "equivalent" capacitor C_D must be discharged through an internal generator resistance R_S. Laboratory experiments indicate that the human body acts as a static (storage) source with a capacitance C_D ranging from 100 to 200 picofarads and a resistance R_S greater than 1000 ohms. Although the upper limits of accumulated static voltage can be very high, measurements suggest that the potential stored by the human body is usually less than 1000 volts. Experience has also indicated that the likelihood of damage to an MOS transistor as a result of static discharge is greater during handling than when the device is installed in a typical circuit. In an rf application, for example, static potential discharged into the antenna must traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the gate terminal of the MOS transistor. The ideal gate-protection signal-limiting circuit is a configuration that allows for a signal, such as that shown in Fig. 5(a), to be handled without clipping or distortion, but limits the amplitude of all transients that exceed a safe operating level, as shown in Fig. 5(b). An arrangement of back-to-back diodes, shown in Fig. 5(c), meets these requirements for protecting the gate insulation in MOS transistors.

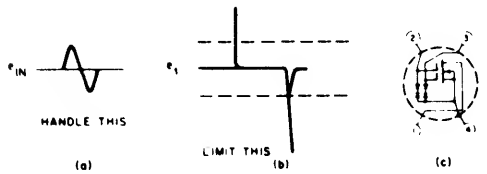


Fig. 5—Gate-protection requirements and solution.

Ideally, the transfer characteristic of the protective signal-limiting diodes should have an infinite slope at limiting, as shown in Fig. 6(a). Under these conditions, the static potential across C_D in Fig. 6(b) discharges through its internal impedance R_S into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, which have an infinite transfer slope, would then limit the voltage present at the gate terminal to its knee value, e_d. The difference voltage e_s appears as an IR drop across the internal impedance of the source R_S, i.e., $e_s = E_S - e_d$ where E_S is the potential in the source of static electricity and e_d is the diode voltage drop. The instantaneous value of the diode current is then equal to e_s/R_S. During physical handling, practical peak values of currents produced by static-electricity discharges range from several milliamperes to several hundred milliamperes.

Fig. 7 shows a typical transfer characteristic curve measured on a typical set of back-to-back diodes used to protect the gate insulation in an MOS field-effect transistor that is nominally rated for a gate-to-source breakdown

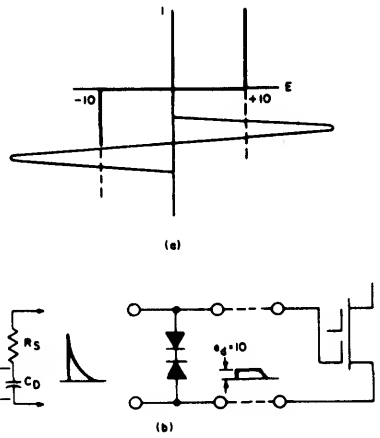


Fig. 6—Ideal transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).

voltage of 20 volts. The transfer-characteristic curves show that the diodes will constrain a transient impulse to potential values well below the ±20 volt limit, even when the source of the transient surge is capable of delivering several hundred milliamperes of current. (These data were measured with 1-microsecond pulses applied to the protected gate at a duty factor of 4×10^{-3}).

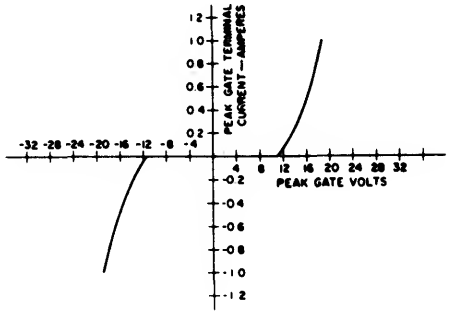


Fig. 7—Typical diode transfer characteristic.

Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the ideal diode adds no capacitance or loading to the rf input circuit. This ideal diode in practice simply does not exist, but integrated circuit techniques made possible the development of a gate-protected MOS FET IC that is close to the ideal. For example, Fig. 8 shows typical 200-MHz input characteristic changes brought about by the addition of the integrated circuit diodes. Their effect on power gain and noise factor is shown by the data given in Table I. These data indicate that there are no discernible reductions in power gain and a trivial noise factor increase of about 0.25 dB.

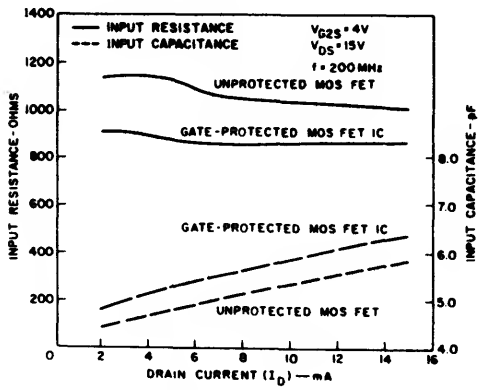


Fig. 8—Input resistance and capacitance as functions of drain current for the MOS FET with and without diodes.

Table I - Power Gain and Noise Factor at 200 MHz

UNIT	POWER GAIN (dB)		NOISE FACTOR (dB)	
	DIODES IN	DIODES REMOVED	DIODES IN	DIODES REMOVED
1	16.3	16.4	3.7	3.4
2	18.8	18.5	2.4	2.2
3	16.5	16.2	3.3	3.0
4	16.3	15.7	3.9	3.4
5	17.7	17.8	2.6	2.4
6	17.2	17.5	2.8	2.5
7	17.1	17.0	3.3	3.2
8	17.9	18.0	2.9	2.6
9	18.5	18.5	2.4	2.3
10	17.3	17.3	3.2	3.0

The Triode-Connected Protected Dual-Gate IC

The dual-gate MOS FET can be connected so that it functions as a single-gate device, as shown in Fig. 9. The triode-connected configuration has curve tracer (drain family) characteristics that look like the 'real' triode. The curves in Fig. 10 show that characteristics for the triode MOS FET (3N128) and the triode-connected dual-gate MOS FET (3N187) are essentially similar.

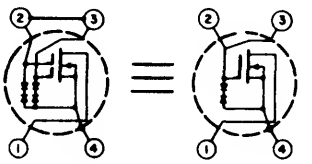


Fig. 9—Dual-gate MOS FET IC in a single-gate configuration.

Triode-Connected-Device Characteristics

Some useful triode-connected-device characteristics are provided in Table II in the form of comparisons with dual-gate and single-gate devices. It should be noted that the difference in I_{DS} level between the 3N187 and the 3N200 carries over to their triode-connected versions. A curve showing I_{DSS} for triode connection versus I_{DS} for the dual-gate configuration (i.e., V_{G2S} = 4 volts) is shown in Fig. 11.

A plot of the triode-connected dual-gate transfer characteristics (I_D vs. V_{GS}) is shown in Fig. 12; similarly, g_{fs} curves are given in Fig. 13 as functions of I_D. Curves for typical dual-gate operation are available in commercial data sheets.[5,6]

Dual gates connected as tetrodes and triodes were evaluated for $R_{D(ON)}$ where 'on' resistance compares favorably with single-gate devices. Typical variations in $R_{D(ON)}$ as a function of gate voltage are shown in Fig. 14.

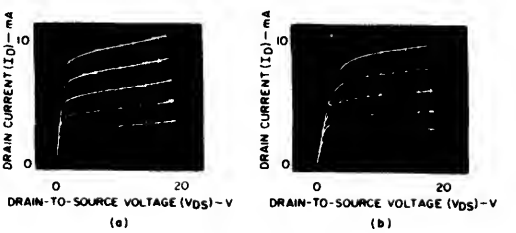


Fig. 10—Drain families: (a) for triode-connected protected dual-gate device; (b) for triode.

Table II – Comparison of Typical Electrical Characteristics for Triode-Connected Dual-Gate, Dual-Gate, and Triode MOS FET Devices

CHARACTERISTIC	CONDITIONS	TRIODE–CONNECTED		DUAL–GATE CIRCUIT*		SINGLE GATE	UNITS
		3N187	3N200	3N187	3N200	3N128	
I_{DS}	V_{DS} = 15 v	6.0	2.0	15	5	15	mA
g_{fs}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	7.0	8.5	12	15	9	mmho
$V_{G1S(OFF)}$	V_{DS} = 15 v, I_D = 50 μA	-2.0	-1.0	-2.0	-1.0	-1.5	V
I_{G1SS}	V_{GS} = ±6 v	2.0	2.0	1.0	1.0	10^{-4}	nA
C_{iss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	10.0	10.0	6.0	6.0	5.5	pF
C_{rss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	0.5	0.5	0.02	0.02	0.2	pF
C_{oss}	V_{DS} = 15 v, I_D = 10 mA, f = 1 kHz	2.0	2.0	2.0	2.0	1.4	pF
$R_{DS(ON)}$	V_{DS} = 1 v, V_{GS} = 0	160	250	100	150	300	ohm

*V_{G2S} = 4 v except for I_{GSS} measurement, where V_{G2S} = 0.

It should not be inferred from these comments that all single-gate applications can be handled by the protected dual-gate device. The advent of MOS FET opened application areas in which circuit requirements imposed leakage-current limits in the picoampere range. For these applications the present generation of protective gate devices do not suffice and it is necessary to employ a "classical" MOS FET type (e.g., 3N128) and exercise precautions against gate-insulation puncture.

SURVEY OF LINEAR APPLICATIONS

This section shows typical circuit arrangements. Some are documented, and others are design ideas for use of dual-gate MOS FET's with integrated diodes in applications using tetrode and triode-connected configurations.

Choppers

The circuits shown in Fig. 15 use the dual-gate MOS FET IC in chopper or gating circuits. In the shunt-circuit configurations shown in Figs. 15(a) and 15(b), the MOS device is normally conductive, i.e., e_o is low. A negative gating-pulse turns off the MOS device so that approximately 50 percent of e_g appears at the output terminals. Circuit (a) features the use of an additional control potential (V_{G2}). A dc potential may be applied as shown to the second gate, thereby establishing the value of desired channel 'on' resistance (R_{DS}). Alternatively, circuitry can be arranged so that the second gate can function as a "coincidence-gate", i.e., to reduce e_o to a low value, a positive-going pulse must be applied to gate 2 simultaneously with a positive-pulse to gate 1.

All circuits in Fig. 15 make reference to Note (A). The circuit diagrams show a "jumper" connected between two terminals in the drain-to-ground-return circuits. The circuits as drawn assume a peak generator level (e_g) of less than 0.2 volts. Should the signal exceed this value, it is possible that the "n-p" parasitic diode between the drain and semi-

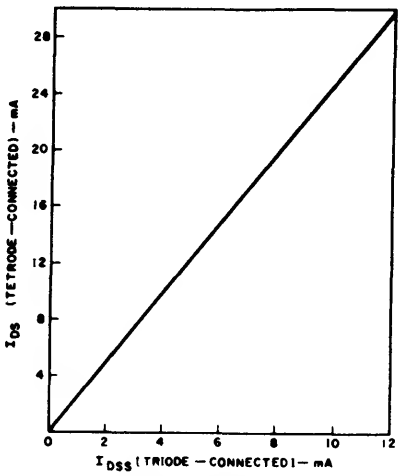


Fig. 11—Correlation of zero-bias drain current for the protected dual-gate device in tetrode (I_{DS}) and triode (I_{DSS}) configurations.

conductor substrate will be driven into conduction and load the signal. This contingency may be obviated (with a simultaneous improvement in attenuator linearity) by connecting a suitable dc potential in lieu of the "jumper", so that a positive potential is applied to the drain. The magnitude of this voltage should equal or exceed the peak value of the rms signal from e_g.

Circuits shown in Figs. 15(c) and 15(d) function in a manner opposite to those described above, i.e., output voltage appears at e_o in the absence of a gating signal. Consequently, a negative gating signal reduces the level of e_o. The dual-gate configuration can be made into an 'or' circuit, i.e., a negative signal applied to gate 2 of sufficient magnitude to override V_{G2} will also reduce the level at e_o.

Attenuators

Fig. 16 shows the dual-gate device in an attenuator circuit. In Fig. 16(a) both gates are used as control elements. This type of circuitry is particularly attractive when control of the attenuator must be located at some remote location. A dc potential on gate 1 has greater control on the channel resistance than is the case for gate 2. Thus an arrangement can be used whereby gate 2 provides a "fine" attenuator adjustment and gate 1 controls "course" adjustment. The circuit in Fig. 16(b) shows the dual-gate device in a triode-connected attenuator circuit. Curves showing typical variations in resistance as a function of gate-voltage were given in Fig. 14.

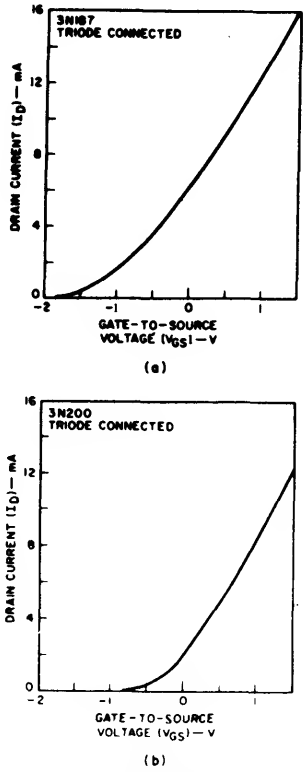


Fig. 12—Triode-connected protected dual-gate MOS FET IC transfer characteristics.

Constant-Current Sources

The characteristics of the MOS FET IC in the region beyond pinch-off make the device suitable for constant-current supplies, as illustrated in Fig. 17 (using a "triode-connected" dual-gate device).

The dual-gate device may be used to obtain higher values of current-regulation with the circuit depicted in Fig. 18. A supply circuit with a maximum output voltage capability of about 4.0 to 5.0 volts is required for V_{G2}. Values greater than this will have negligible effect on output current control.

The circuits in Fig. 19 use the MOS FET constant-current characteristic to make a regulated constant-voltage reference source by feeding I_{DS} through a fixed-value resistor.

In any typical amplifier application using the MOS FET device, e.g., in Fig. 20, the voltage developed across a bypassed source resistance provides a well-regulated fixed reference voltage (if the amplifier stage is not subjected to

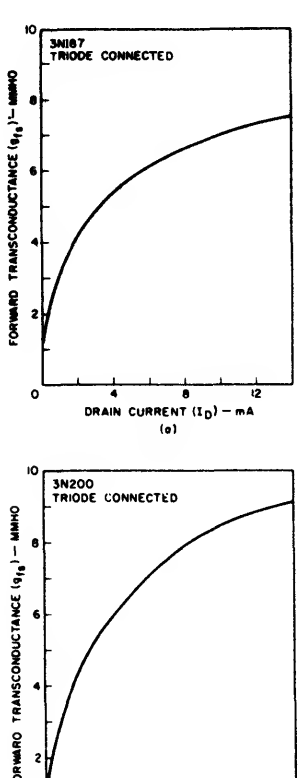


Fig. 13—Triode-connected protected dual-gate MOS FET IC transconductance characteristics.

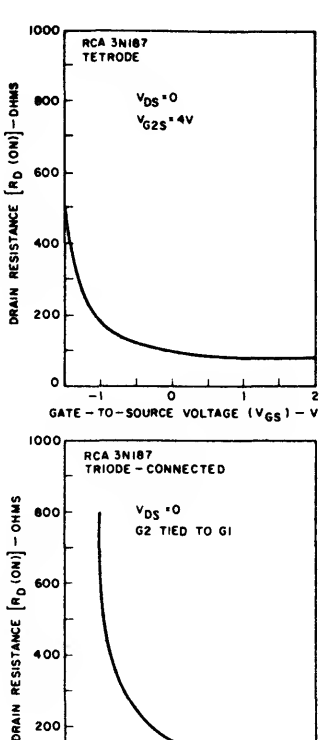


Fig. 14—"ON" resistance as a function of gate voltage for tetrode- and triode-connected protected dual-gate MOS FET IC's.

varying bias conditions, such as those encountered in connection with AGC). When a reference voltage is obtained in this manner, it is advisable to feed it to other circuitry through an adequate decoupling network.

General-Purpose Amplifier Circuits

Fig. 21 shows three basic single-stage amplifier configurations that utilize dual-gate-protected MOS FET IC's as triodes and as tetrodes in common source, common-drain, and common-gate circuits. Each configuration has its own particular advantages for specific applications. The dual-gate device has an added advantage in any of these configurations in that gate 2 provides (a) reduced gate-to-drain capacity by an order of magnitude, and (b) a convenient means for controlling the gain of the stage by adjusting the dc potential applied to gate 2.

A dual-gate device is shown in Fig. 22 as a shunt-type attenuator to control the input level to a source-follower. The source-follower uses the dual-gate MOS FET with gate 2 available as a control for adjusting the gain of the source-follower. The jumper in the ground return path of the generator can be used to insert a positive voltage on the drain for the reasons explained above.

Fig. 23 shows a circuit using the "triode-connected" dual-gate device in a simple 20-dB preamplifier for extending the sensitivity range of an oscilloscope or ac voltmeter. It can also be used in audio circuits as a phono preamplifier or microphone preamplifier. It is shown as self-contained, i.e.,

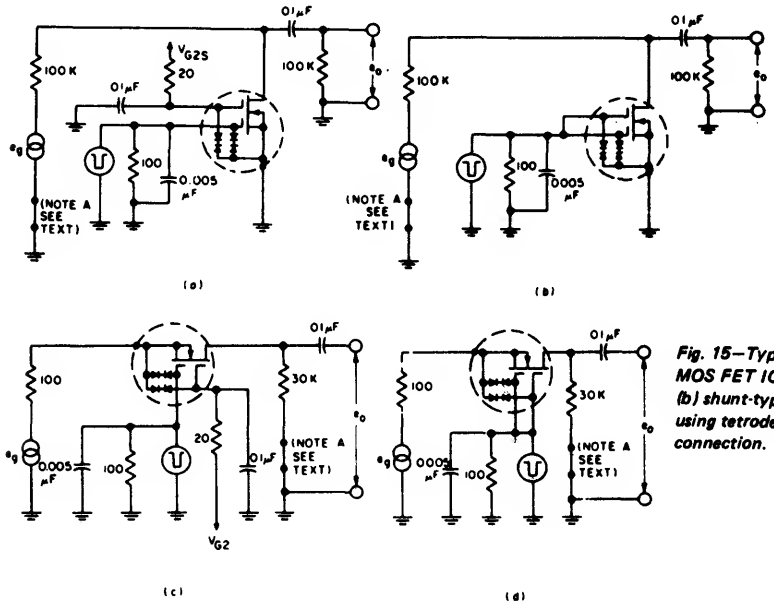


Fig. 15—Typical chopper circuits using protected dual-gate MOS FET IC's. (a) shunt-type using tetrode connection; (b) shunt-type using triode connection; (c) series-type using tetrode connection; (d) series-type using triode connection.

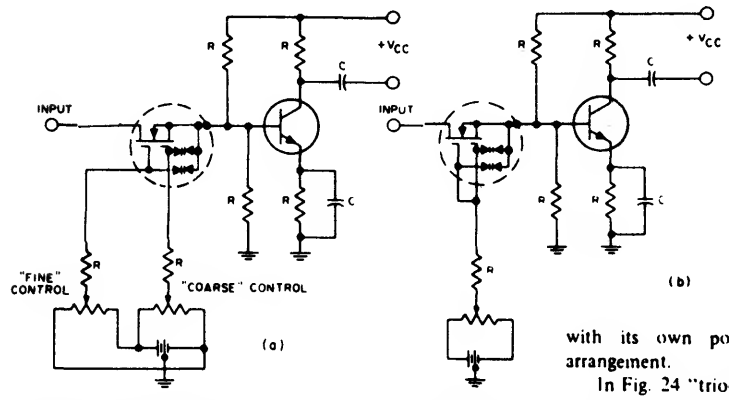


Fig. 16—Attenuator circuits using the protected dual-gate MOS FET IC: (a) variable series-type attenuator with coarse and fine controls; (b) variable series-type attenuator using triode-connected configuration.

with its own power supply and a by-pass switching arrangement.

In Fig. 24 "triode-connected" MOS FET devices are used in a simple differential amplifier configuration in which the "triode-connected" gates of the two devices are biased from a single source (the junction of R1 and R2). This arrangement is possible because the 3N187 has a typical gate current (I_{GSS}) in the triode configuration of 2 nanoamperes. Therefore, the bias can be supplied through R3 with a negligible voltage offset. Resistor R5 is used to null out the effects of slight differences in device characteristics so that the offset-voltage at e_o can be set to zero.

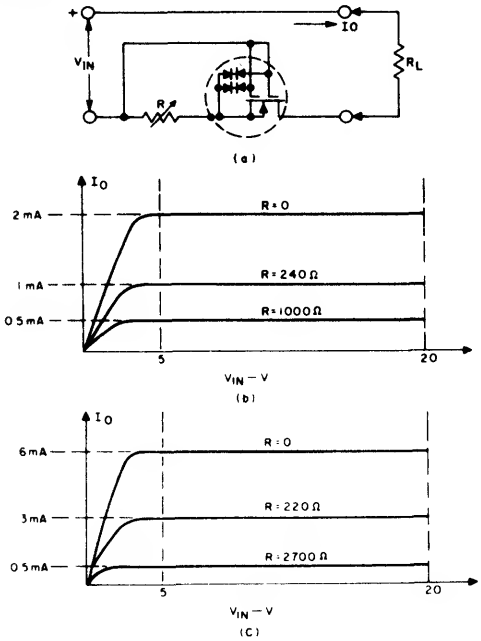


Fig. 17–Constant-current supply using protected dual-gate MOS FET IC in triode configuration: (a) basic circuit; (b) typical I_o vs. V_{in} for RCA-3N200 in the basic circuit; (c) typical I_o vs. V_{in} for RCA-3N187 in the basic circuit.

The circuit in Fig. 25 shows another differential amplifier configuration, in which the offset voltage at e_0 can be set to zero by means of appropriate potentials supplied to the No. 2 gates, adjustment being provided by R6.

The circuit shown in Fig. 26 is a frequency-selective amplifier intended for operation within the audio frequency range of 10 Hz to 20 kHz. Frequency-selective circuits are used for selective coding, i.e., in garage-door openers, narrowing the bandwidth response in CW receivers to

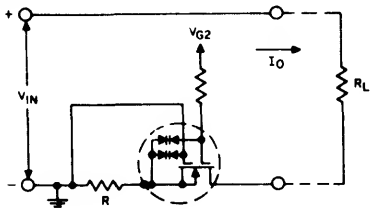


Fig. 18–Protected dual-gate device as a constant-current source.

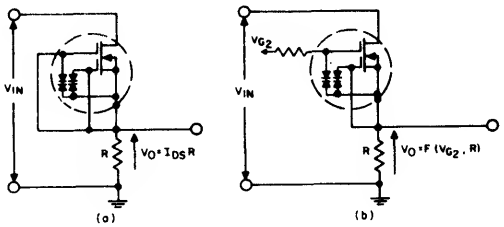


Fig. 19–Voltage-reference circuits using protected dual-gate MOS FET IC: (a) as triode; (b) as tetrode.

eliminate unwanted side bands, and in systems requiring some form of keying impulse (e.g., synchronizing the narration in a tape recorder with slides).

The frequency-selective circuit shown is an audio amplifier with a twin-"T" RC filter circuit in its output. This network provides regenerative feedback to the input circuit at an audio frequency predetermined by the selection of capacitors C5, C6, and C7. The peaking control R7 fine-tunes the twin-"T" for the desired frequency of operation, and potentiometer R8 adjusts the level of feedback for desired performance. The circuit as shown in Fig. 26 is selective at an audio frequency of 1200 Hz. Table III below lists values of the bridge capacitors for operation at other frequencies.

RF Amplifiers, Oscillators, and Mixers

The circuit in Fig. 27 is a converter used to convert 10-MHz WWV broadcasts to 1.5 MHz for reception on a standard broadcast-band receiver. The MOS FET IC is used in the dual-gate configuration as a mixer and is triode-

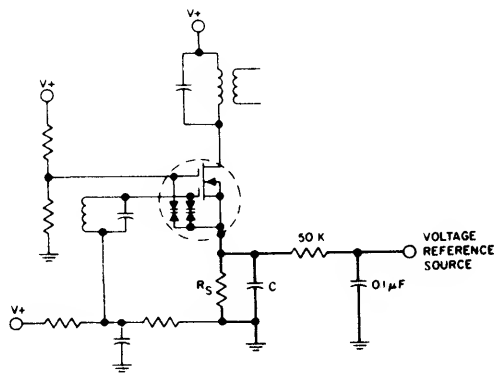


Fig. 20–Typical amplifier using bypassed source resistor as a voltage source.

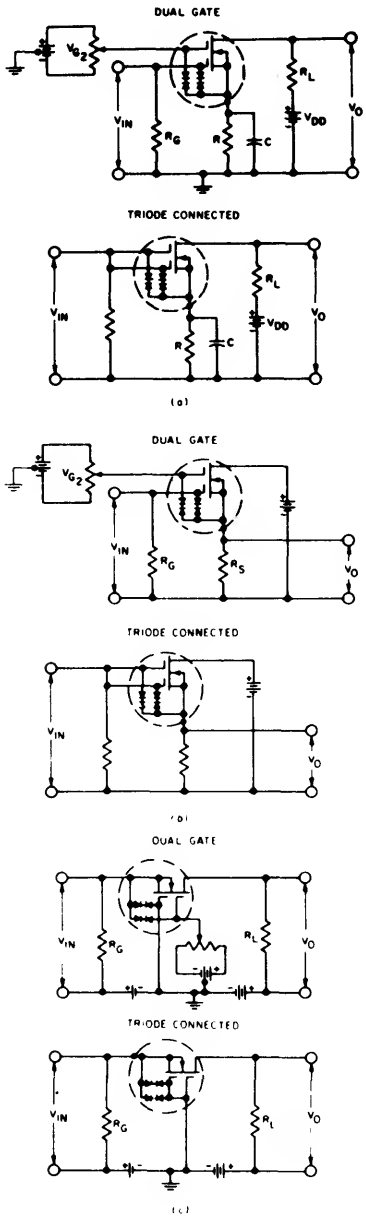


Fig. 21–Three basic single-stage amplifier configurations that use protected dual-gate MOS FET IC's as triodes and tetrodes: (a) common source; (b) common drain; (c) common gate.

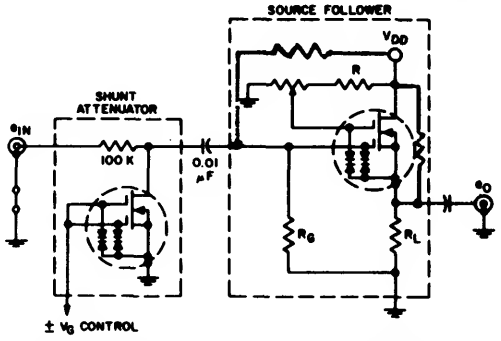


Fig. 22–Shunt-type attenuator controlling input level to source-follower.

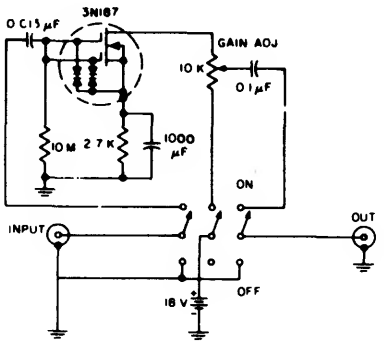


Fig. 23–Protected dual-gate MOS FET IC preamplifier.

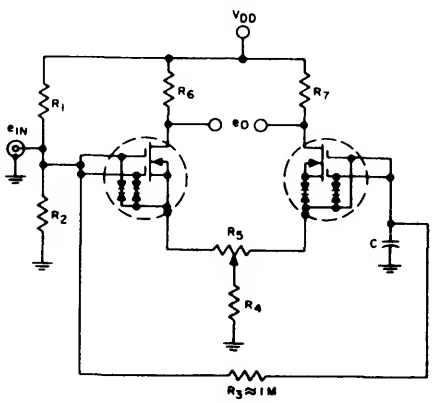


Fig. 24–Triode-connected MOS FET IC's in a simple differential amplifier circuit.

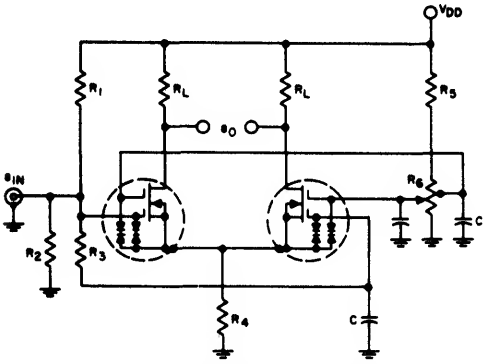


Fig. 25–Protected dual-gate MOS FET IC's in typical differential amplifier circuit using gate 2 for balance control.

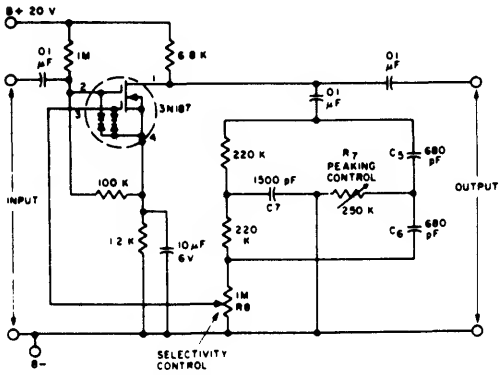


Fig. 26–Selective audio-frequency amplifier.

Table III – Capacitor values for Fig. 26

FREQUENCY (Hz)	C5, C6 (pF)	C7 (pF)
150	5,600	12,000
300	2,700	6,200
600	1,300	3,000
2400	330	750
4800	160	360
9600	82	180

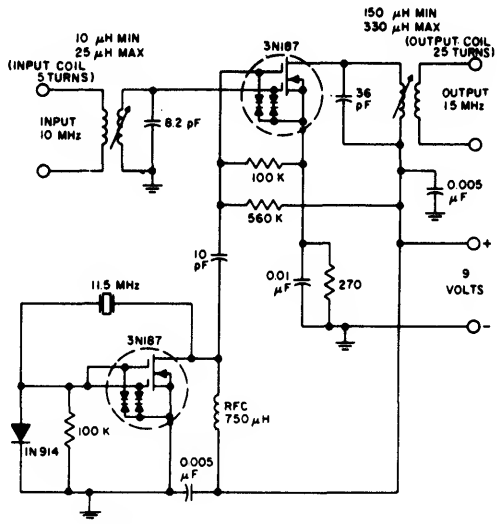


Fig. 27–10 MHz-to-1.5 MHz converter for WWV reception.

connected in a crystal oscillator circuit. MOS FET characteristics are very attractive for use in highly stable oscillator circuits because the inherent reactive components, C_{iss} and C_{oss}, are relatively invariant over a very wide temperature range. Additional types of oscillator circuits in a number of different arrangements are shown in Fig. 28.

It is also feasible to use the MOS FET IC as a keyed oscillator, by utilizing a circuit arrangement shown in Fig. 29. A negative voltage at gate 2 will key the oscillator. Additionally, the level of the oscillator output can be controlled by variation of R_L. It should be understood that any of the oscillator configurations shown above are adaptable to the circuit arrangement in Fig. 29.

A dual-gate-protected MOS FET IC is used in Fig. 30 as a regenerative amplifier/detector. The circuit is basically an amplifier with controlled feedback adjusted to the verge of oscillation, as shown in Fig. 30. Gate 2 provides a convenient means to adjust the amplifier gain to the requisite level. Detection is accomplished in the gate 1 input circuit by the interaction of the diode in parallel with the 100-kilohm resistor and the 270-picofarad capacitor.

A typical circuit that utilizes the MOS FET IC in the pix IF section of a TV receiver is shown in Fig. 31. This circuit utilizes gate 2 for AGC. The reverse AGC bias[7] applied to gate 2 in the circuit of Fig. 31 has the secondary effect of making gate 1 move in a positive direction. Evaluations of the relationship between AGC and crossmodulation show that it is desirable to allow the voltage between gate 1 and the source to move in a positive direction when gate 2 is reverse-biased. Various circuit arrangements have been used

to achieve this action. Reference to a more comprehensive review on crossmodulation as a function of bias is given in the bibliography.[2,3]

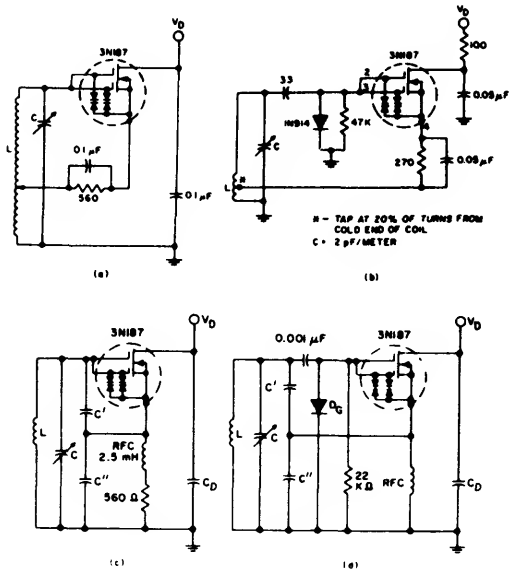


Fig. 28–Oscillator circuits using MOS FET IC's: (a) and (b) Hartley oscillators; (c) and (d) Colpitts oscillators.

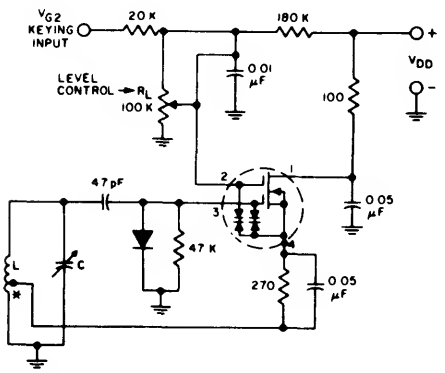


Fig. 29–Gate-keyed oscillator using MOS FET IC.

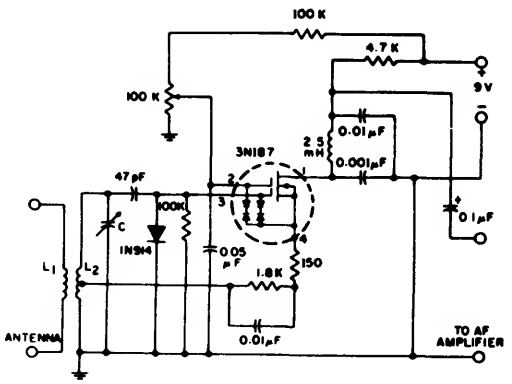


Fig. 30–Protected dual-gate MOS FET IC regenerative receiver.

A typical circuit for an FM tuner is shown in Fig. 32. The biasing arrangement for the rf stage incorporates provisions for AGC. The circuit in Fig. 33 is an rf amplifier designed for 200-MHz operation. The typical power gain for a 3N187 in this circuit is 18 db, with a noise factor of 3.5 dB.

Typical circuits for a TV tuner are shown in Figs. 34(a)-(d). Fig. 34(a) is the rf stage operating at a current level of approximately 10 milliamperes. Gate 1 is about 2 volts above ground potential. When AGC applied to gate 2 is advanced the drain current decreases, with a consequent reduction in voltage drop across the 270-ohm source resistances.[7]

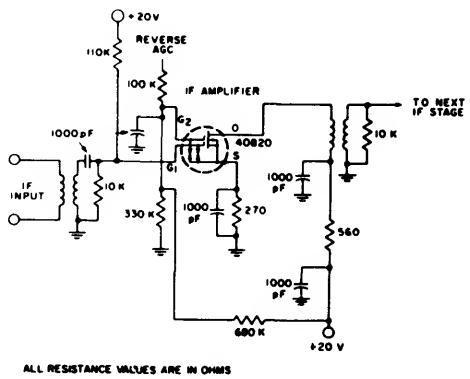
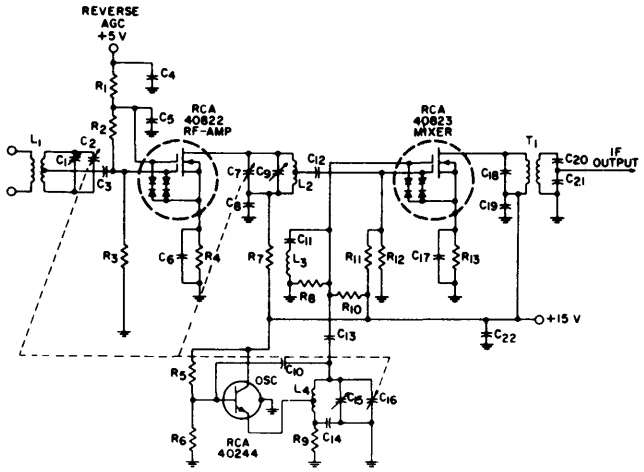
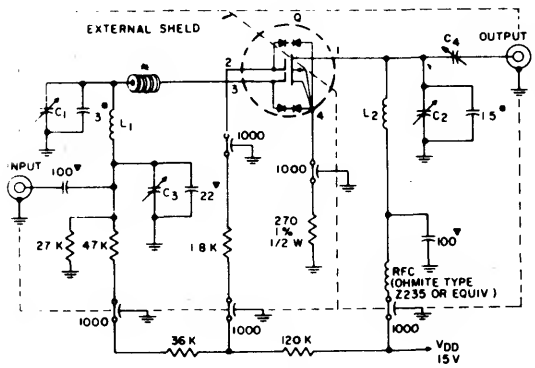


Fig. 31–TV IF amplifier stage utilizing RCA-40820 MOS FET IC.



C1, C9, C15 = Trimmer capacitor, 2 to 14 pF
C2, C7, C16 = Ganged tuning capacitors, each section = 6 to 19.5 pF
C3, C6, C14, C17, C22 = 2000 pF, ceramic
C4, C5 = 1000 pF, ceramic disc
C8, C19 = 0.01 μF, ceramic disc
C10 = 3.3 pF, NPO ceramic
C11 = 270 pF
C12 = 500 pF, ceramic disc
C13 = 3 pF, NPO ceramic
C18 = 68 pF, ceramic
C20 = 50 pF, ceramic
C21 = 1200 pF, ceramic
L1 = antenna coil, 4 turns of No. 18 bare copper wire, inner diameter, 9/32 inch, winding length, 3/8 inch, nominal inductance, 0.86 μH, unloaded Q, 120; tapped approximately 1 1/4 turns from ground end, antenna link approximately 1 turn from ground end
L2 = rf interstage coil, same as L1 antenna link
L3 = rf choke, 1 μH
L4 = oscillator coil; 3 1/4 turns of No. 18 bare copper wire; inner diameter, 9/32 inch; winding length, 5/16 inch; nominal inductance, 0.062 μH, unloaded Q, 120; tapped approximately 1 turn from low end
R1, R10 = 0.56 megohm, 0.5 watt
R2 = 0.75 megohm, 0.5 watt
R3 = 0.27 megohm, 0.5 watt
R4, R13 = 270 ohms, 0.5 watt
R5 = 22000 ohms, 0.5 watt
R6 = 56000 ohms, 0.5 watt
R7 = 330 ohms, 0.5 watt
R8, R12 = 0.1 megohm, 0.5 watt
R9 = 4700 ohms, 0.5 watt
R11 = 1.6 megohms, 0.5 watt
T1 = first if (10.7 MHz) transformer, double-tuned with 90 per cent of critical coupling, primary: 15 turns of No. 32 enamel wire, space wound at 60 turns per inch on 0.25-by-0.5-inch slug; secondary: 18 turns of No. 36 enamel wire, close wound on 0.25-by-0.25 inch slug, both coils wound on 9/32-inch coil form.

Fig. 32–FM tuner using RCA-40822 and RCA-40823 MOS FET IC's for the rf amplifier and mixer stages.



#Ferrite bead (4); Pyroterric Co. "Carbonl J" Q = 3N187 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.
All resistors in ohms
All capacitors in pF
▼ Disc ceramic
• Tubular ceramic
C1 = 1.8-8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.
C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.
C3 = 1-10 pF piston-type variable air capacitor. JFD Type VAM-010; Johanson Type 4335, or equivalent
C4 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.
L1 = 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon, internal diameter of winding = 0.25 in., winding length approx. 0.08 in.
L2 = 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16 in. ID. Coil = .90 in. long.

Fig. 33–200-MHz amplifier using the RCA-3N187 MOS FET IC.

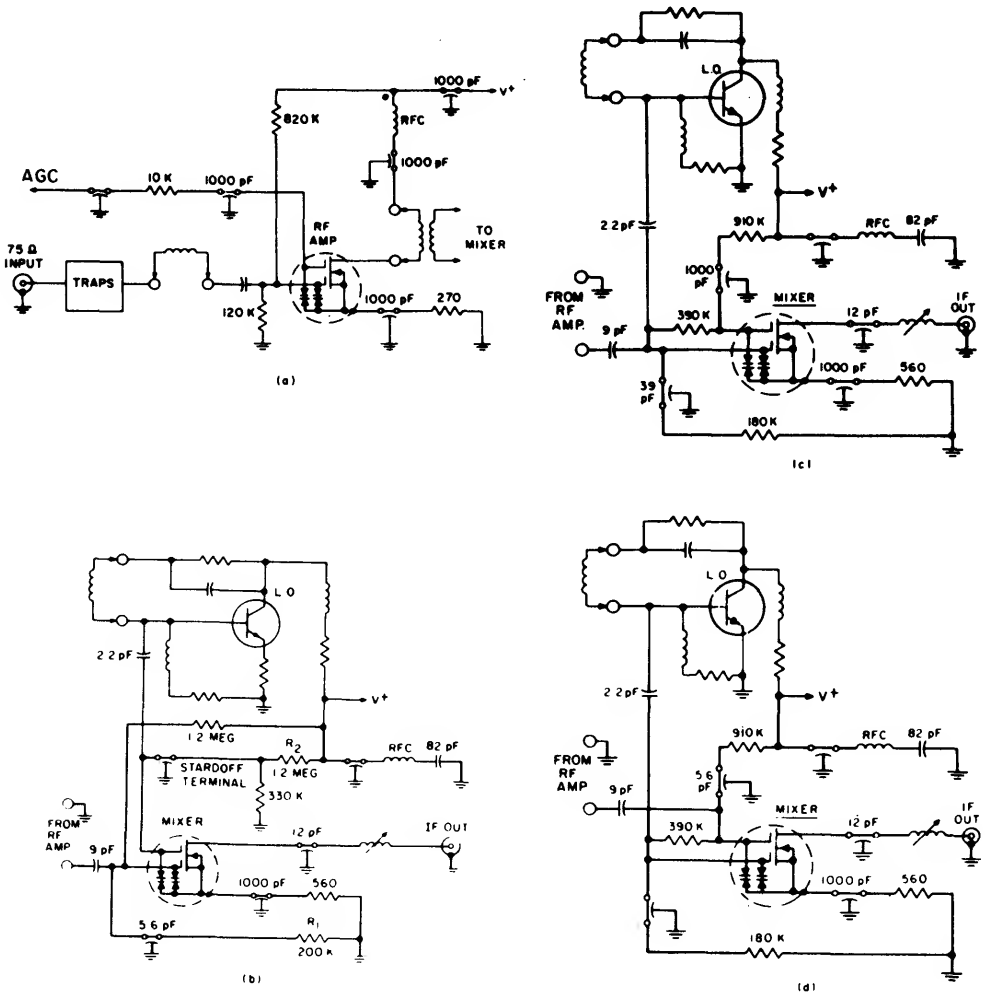


Fig. 34—Typical circuits using protected dual-gate MOS FET IC's in a TV tuner for (a) rf stage, (b) mixer with rf on gate 1, oscillator on gate 2; (c) mixer with both rf and oscillator on gates 1 and 2; (d) mixer with rf on gate 2 and oscillator on gate 1.

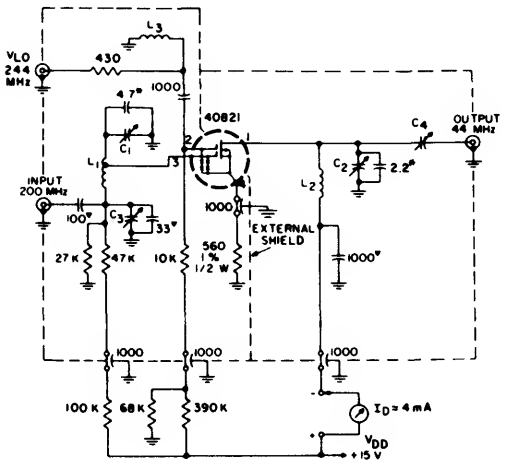
Because the voltage on gate 1 is fixed, the effect of applying AGC is to make the gate-to-source voltage drift in a positive direction as a negative gate 2 (AGC) voltage is applied. In these cases, as in the earlier IF system shown in Fig. 31, this circuit arrangement optimizes tuner performance for crossmodulation.[2]

The rf stage in Fig. 34(a) can work into any of the mixer circuits shown in Figs. 34(b), (c), and (d).

Fig. 34(b) is a mixer circuit arrangement with oscillator injection into gate 2 and the rf signal applied to gate 1. Fig. 34(c) utilizes gate 1 and gate 2 as the input elements for both rf signal and oscillator. Fig. 34(d) shows the rf signal applied to gate 2 and oscillator injection on gate 1.

Each of the above circuit arrangements has its own desirable characteristics, and the subject of mixer performance deserves a much more detailed discussion than can be accommodated here. In this context it is intended to demonstrate feasibility in terms of circuit arrangements.

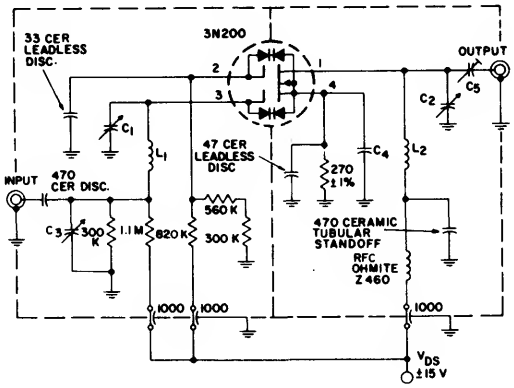
A mixer circuit with component values used in the laboratory for measuring conversion power gain from 200 to 44 MHz is shown in Fig. 35.[8]



▼ Disc. ceramic.
• Tubular ceramic.
All resistors in ohms
All capacitors in pF
C1, C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.
C3 = 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C4 = 0.9-7 pF compression-type capacitor: ARCO 400 or equivalent
L1 = 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C1 end of winding.
L2 = Ohmite Z-235 RF choke or equivalent.
L3 = J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.
NOTE: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig. 35—Mixer circuit for 200 MHz-to-44 MHz conversion, using the RCA-40821 MOS FET IC.

Protected dual-gate MOS FET's have been used in applications operating at frequencies up to 500 MHz. They are useful in such uhf applications as rf amplifiers and mixer circuits. For example, the RCA-3N200 has the capability to provide a typical rf power gain of 12.5 dB with 4.5-dB noise factor at 400 MHz in a common-source configuration without the need for neutralization. A circuit with this capability is shown in Fig. 36.



All resistances in ohms
All capacitances in pF
C1, C2 = 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent
C3 = 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent
C4 = Approx. 300 pF - capacitance formed between socket cover & chassis
C5 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent
L1, L2 = inductance to tune circuit

Fig. 36—Using the RCA-3N200 MOS FET IC in a 400-MHz amplifier.

CONCLUSIONS

The preceding discussions outlined numerous practical applications that utilized the unique technical features of the RCA protected dual-gate MOS FET IC. A summary of these technical features includes:

1. Wide dynamic range – MOS FET IC's will handle both positive and negative signal excursions.
2. Crossmodulation and spurious response performance is inherently better than with other active devices such as bipolars and single-gate FET's.
3. The very low gate-leakage permits AGC circuitry with virtually no power requirements.

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2 E.F. McKeon "Crossmodulation Effects in Single Gate and Dual Gate MOS Field Effect Transistors" RCA Application Note AN-3435.

3 S. Reich and L.S. Baar, "A Comparison of Solid-State and Electron Tube Devices For TV-Receiver RF and IF Stages." IEEE Transactions on Broadcast and TV Receivers, Vol. BTR-13, pag. 41, April 1967.

4 J.R. Burns, "High Frequency Characteristics of Two Insulated Gate Field Effect Transistor" RCA Review, Vol. XXVIII No. 3, Sept. 1967, pp. 385-417.

5 3N187 Data Sheet, RCA File #436.

6 3N200 Data Sheet, RCA File #437.

7 S. Reich, "MOS FET Biasing Techniques," EEE, Sept. 1970.

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4. Two input control elements make the device adaptable for mixers, remote-control gain circuits, coincidence gate circuits, etc. The device can also function as a triode-equivalent when the two gates are connected to a single terminal.
5. An exceptionally high transconductance.
6. Negative temperature coefficient for drain current, so that thermal runaway is virtually impossible.
7. Extremely low feedback capacity, typically 0.02 picofarad; this means very low oscillator feedthrough from the mixer stage back to the antenna.
8. The low feedback capacity enables the dual-gate MOS FET IC to provide good rf power gain in common-source amplifiers without the need for neutralization.
9. In addition to the above features, the new MOS FET IC provides protection against static electricity discharges encountered during handling and/or in circuit applications. This protection was achieved with insignificant compromises in overall device performance.

ICAN-4072

Applications of the RCA CA3048 Integrated-Circuit Amplifier Array

by
L. Kaplan

The RCA CA3048 integrated circuit is an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip. The circuit is housed in a 16-lead dual-in-line plastic package. It has an operating and storage temperature range of -25°C to +85°C. Each amplifier in the array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The noise in the CA3048 is inherently very low and is tightly controlled in rigorous factory and quality-control testing.

The combination of low noise, high gain, and high input impedance make, the CA3048 a very versatile unit. and numerous applications suggest themselves for its use.

CIRCUIT DESCRIPTION

Fig. 1 shows the complete schematic of the CA3048 integrated-circuit amplifier array. Each amplifier (A_1 through A_4) provides two stages of voltage gain.

The input stage is basically a differential amplifier with a Darlington transistor added on the one side. The output stage consists of a combination of three transistors and associated resistors connected in an inverting configuration. For example, in amplifier A_3, Q_{19} is the Darlington input transistor, and Q_{20} and Q_{21} are the differential-pair transistors. The load resistor R_{29} for the differential input stage is located in the collector lead of transistor Q_{20}. Transistors Q_{13}, Q_{14}, and Q_{17} are used in the output stage. Transistor Q_{17} is the actual output transistor; transistors Q_{13} and Q_{14} raise the input impedance of the output stage so that the loading of the 30,000-ohm source resistance R_{29} (i.e., load resistor for the differential-amplifier input stage) is small. The ratio of total collector resistance to emitter resistance $[(R_{31} + R_{38})/R_{50}]$ in the output stage is 1000/200, or 5. In view of the small source loading, the stage gain, therefore, is essentially equal to 5.

A feedback network (R_{41}, R_{42}, R_{46}, and D_7) is connected between the output terminal and the base of transistor Q_{21}. The resistor values are chosen so that the output transistor is biased at approximately 5 milliamperes for maximum dynamic range. Diode D_7 compensates for variations in the base-to-emitter voltage of Q_{21} with changes in temperature. Because the other transistor (Q_{20}) of the differential amplifier has two emitter-base junctions in series, two diodes, D_3 and D_4, are required for temperature compensation. Diodes D_3 and D_4 also provide temperature compensation for the differential-pair transistor Q_1 in amplifier A_2 (similarly diodes D_5 and D_6 are shared by amplifiers A_1 and A_4).

Diodes D_3 and D_4 and diodes D_5 and D_6 are connected to their respective inputs through a relatively stiff voltage divider (for amplifier A_3, the divider consists of R_{27} and R_{28}). The input to amplifier A_3 is normally applied to the base of the Darlington transistor Q_{19}. The 100-kilohm resistor R_{37} supplies bias current to this transistor. The voltage drop across resistor R_{37} is small because of the very small base current of transistor Q_{19}.

Each amplifier of the CA3048 may be viewed as an ac operational amplifier in which a fixed resistance is permanently connected between the output and the inverting input. The built-in feedback resistor delimits the characteristics of the CA3048 amplifiers in the following ways:

1. The impedance as viewed from the noninverting input terminal consists mainly of the 100 kilohm input-bias resistance (R_{13}, R_{15}, R_{37}, or R_{39}). This resistance is shunted by the input capacitance of approximately 10 picofarads and the additional resistive loading presented by the input impedance of the Darlington input pairs. When the amplifier is operated under open-loop conditions (inverting input at ac ground), the total input impedance consists of 90 kilohms in shunt with the input capacitance. When the built-in feedback loop is allowed to function (by insertion of an unbypassed resistance in the noninverting input lead), then the loading caused by the Darlington input pairs is reduced, and the input resistance rises asymptotically towards 100 kilohms.
2. The impedance as viewed from the inverting input terminal is small (in the order of 40 to 50 ohms.)
3. When the CA3048 is used in its normal mode of operation, each amplifier in the array may be represented by the equivalent circuit shown in Fig. 2. (The capacitances shown are the sum of the device capacitances, socket capacitances, and stray capacitances.) The transconductance G_m, which is equal to the product of the voltage gain and the output conductance (10^{-3}mho), is typically 0.8 mho at midband.

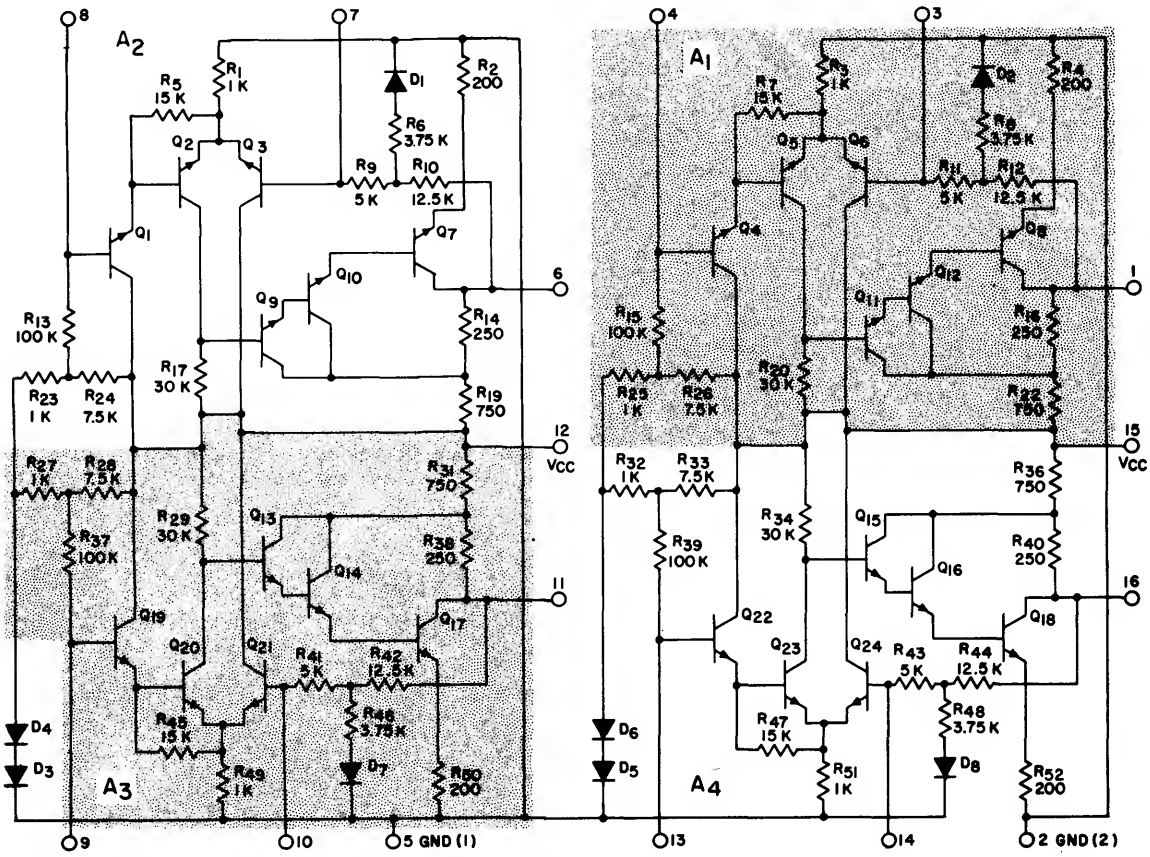


Fig. 1 - Schematic of the CA3048 integrated-circuit amplifier array.

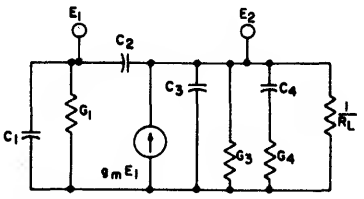


Fig. 2 - Equivalent circuit of a CA3048 amplifier.

GAIN-FREQUENCY RESPONSE

Curves of the transconductance of any amplifier in the CA3048 array as a function of frequency up to 30 MHz show two break points. At frequencies above the first break point, which occurs at 300 kHz, the transconductance rolls off at a rate of 6 dB per octave to 12 MHz. At frequencies above 12 MHz, the rate of roll-off increases to 12 dB per octave. At frequencies up to 12 MHz, therefore, the transconductance of any amplifier in the CA3048 array is expressed by the following equation:

$$g_m = \frac{\omega_o g_{mo}}{\omega_o + S} \qquad (1)$$

where S is the complex frequency, g_{mo} is the mid-band transconductance, and $\omega_o = 2\pi \times 300 \times 10^3$.

Fig. 3 shows the open-loop transconductance for an amplifier in the CA3048 array as a function of frequency. This response indicates potential uses of the CA3048 integrated circuit at frequencies that extend into the video range.

STABILITY

The equivalent circuit shown in Fig. 2 can be used to determine the stability of the amplifiers in the CA3048 array under various conditions of loading when undesirable external capacitance is present in the wiring and socket. With no external generator connected to the circuit, the input conductance G_1 is equal to 1/100000 mho, and the output conductance G_3 is equal to 1/1000 mho (for amplifiers A_1, A_2, A_3, or A_4, respectively, G_1 is equal to $1/R_{15}$, $1/R_{13}$, $1/R_{37}$, or $1/R_{29}$, and G_3 is equal to $1/(R_{16} + R_{22})$, $1/(R_{14} + R_{19})$, $1/(R_{31} + R_{38})$, or $1/(R_{36} + R_{40})$. The capacitance C_4 and the conductance G_4 shown in Fig. 2 represent an external damping network which can be varied or deleted as demanded by stability or gain-bandwidth requirements.

A necessary and sufficient condition for a system to be stable is that the roots of the characteristic equation of the system have no positive real parts. The characteristic equation for the circuit of Fig. 2 is obtained by expansion of the circuit determinant and collection of the coefficients of the complex frequency S. The equation assumes the following form:

$$A_1 + A_2S + A_3S^2 + A_4S^3 + A_5S^4 = 0 \qquad (2)$$

After much tedious algebra, the coefficients are determined as follows:

$$A_1 = \omega_o G_1 G_3 G_4$$

$$A_2 = \omega_o G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3) - g_{m_o} G_2] + G_1 G_3 (C_3 \omega_o + G_4)$$

$$A_3 = \omega_o \{C_2C_3(G_1 + G_3 + G_4 - g_{m_o}) + C_1 [C_3(G_3 + G_4) + C_2G_4]\} + G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3)] + G_1G_3C_3$$

$$A_4 = G_4 [C_1(C_2 + C_3) + C_2C_3] + C_3 [C_1(\omega_o C_2 + G_3) + C_2(G_1 + G_3)]$$

$$A_5 = C_1C_2C_3 \qquad (3)$$

With the aid of a computer, it is possible to check very quickly many combinations of circuit values for stability by solving for the roots of Eq. (2) with different circuit values assigned to the various components.

Although there are many variables involved, it is possible to state in a general sense the results of several solutions of Eq. 2.

The system cannot oscillate without capacitor C_2 to introduce positive feedback. The analysis is reduced, therefore, to the determination of the maximum value of C_2 before oscillation occurs. With careful printed-circuit-board layout, the feedback capacitance C_2 is small, and the system is usually stable. If a socket is used the feedback capacitance is greatly increased, and

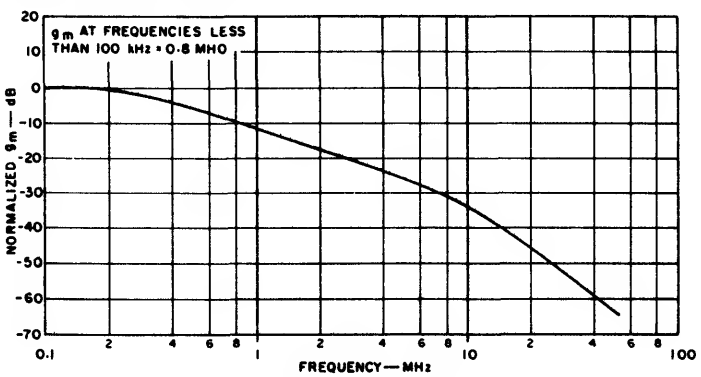


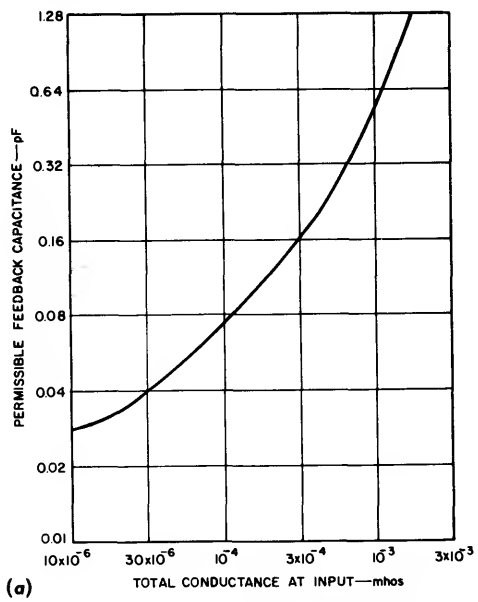
Fig. 3 - Typical gain-frequency response for a CA3048 amplifier.

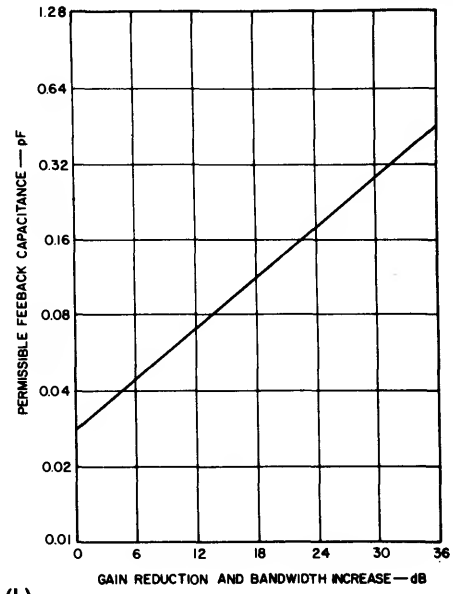
stabilization of the circuit is generally required.

As with any two-port network, any increase in source or load conductance aids stability. In addition, analyses of Eq. (2) show that addition of shunt capacitance at the input is a very effective stability technique when the source impedance is high. Introduction of negative feedback into the circuit [which is simulated in Eq. (2) by a decrease in the value assigned to the transconductance g_m and an increase in the cutoff frequency] also improves circuit stability.

Another stability method, which is effective for any source impedance or gain value, is the addition of a damping network such as that formed by capacitance C_4 and conductance G_4 in Fig. 2. In this method, the value of C_4 is chosen so that its reactance is equal to the parallel combination of R_3 and R_L at the highest frequency of desired amplification. The value of R_4 is made small so that the gain is reduced at high frequencies and is typically 1/10 or 1/20 the value of the parallel combination of R_3 and R_L.

The series of curves in Fig. 4 show the results of the computation for the roots of E_q. (2). It should be noted that the maximum value shown for capacitance C_2 is that obtained just before oscillation occurs. Severe peaking of the response (or ringing) may result before the listed value of C_2 is reached. It is advisable, therefore, to maintain the capacitance of C_2 well below the indicated value.





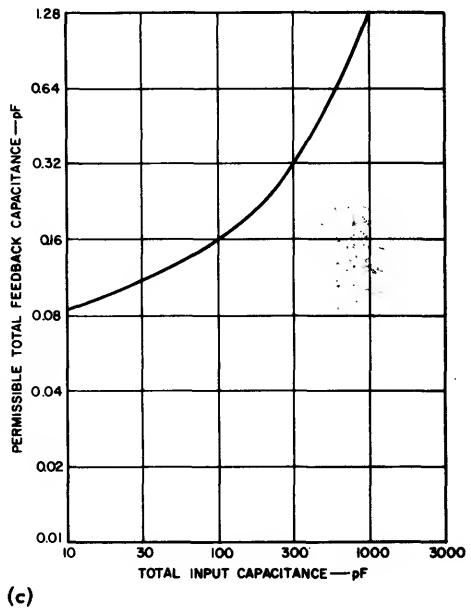


Fig. 4 - Stability curves for a CA3048 amplifier: (a) permissible feedback capacitance as a function of the total conductance at the input; (b) permissible feedback capacitance as a function of gain reduction and of bandwidth increase; (c) permissible feedback capacitance as a function of the total input capacitance.

OUTPUT SWING VS. SUPPLY VOLTAGE

Fig. 5 shows the output voltage for any one of the CA3048 amplifiers as a function of supply voltage. The solid lines represent the performance obtained with the full open-loop gain. The dotted line shows the improvement obtained when 12 dB of negative feedback is added by inclusion of a 150-ohm unbypassed resistor in the inverting-input lead. The values obtained for this curve are those which prevail when the output is loaded only by the measuring equipment. It should be realized that any substantial loading will tend to reduce the magnitude of the available output voltage for equivalent distortion figures. For example, an additional 1000-ohm load exactly balances the internal load resistor, and would reduce the available output voltage by 50 per cent.

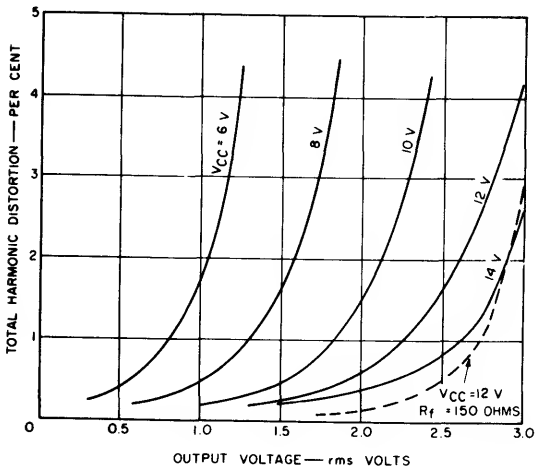


Fig. 5 - Total harmonic distortion of a CA3048 amplifier as a function of output voltage for different value of dc supply voltage.

NOISE

Fig. 6 shows output noise obtained when a single amplifier of the CA3048 is operated at 40 dB gain into a "C" filter. Table I shows typical values of noise voltage (E_{noise}) and current (I_{noise}) for the CA3048 at spot frequencies of 10, 100, 1000, 10000, and 100000 Hz. From these values, the equivalent input noise voltage for any value of source resistance may be computed by use of the following equation:

$$E_{equiv} = \sqrt{(E_{noise})^2 + (I_{noise}\, R_{source})^2} \qquad (4)$$

Laboratory measurements have shown that the noise performance of the CA3048 is not significantly affected by variation of the supply voltage. The values shown in Fig. 6, therefore, may be used with supply voltages down to about 2 volts if it is remembered that the open-loop gain decreases to about 35 dB at a supply voltage of 2.5 volts.

TABLE I
TYPICAL NOISE VOLTAGE AND CURRENT FOR AN AMPLIFIER IN THE CA3048 ARRAY

Frequency (Hz)	E_{noise} (volts)	I_{noise} (amperes)
10	30.5×10^{-9}	7.5×10^{-12}
100	17×10^{-9}	4.3×10^{-12}
1000	8×10^{-9}	1.2×10^{-12}
10000	6×10^{-9}	0.5×10^{-12}
100000	4×10^{-9}	0.3×10^{-12}

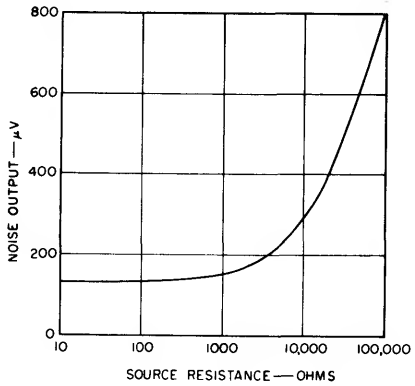


Fig. 6 - Noise output as a function of source resistance for a CA3048 amplifier.

CIRCUIT APPLICATIONS

In all the foregoing discussions, a single amplifier has been described as though it existed alone. The CA3048, however, consists of four separate amplifiers, which may be used independently or in combination. A glance at the complete schematic of the CA3048 reveals other aspects worthy of consideration.

Two supply-voltage terminals and two ground terminals are indicated. Terminal No. 12 supplies the V_{CC} voltage to amplifiers A_2 and A_3, and terminal No. 15 supplies the V_{CC} voltage to amplifiers A_1 and A_4. The ground return for amplifiers A_1 and A_4 is provided by terminal No. 2; all other ground returns are provided by terminal No. 5.

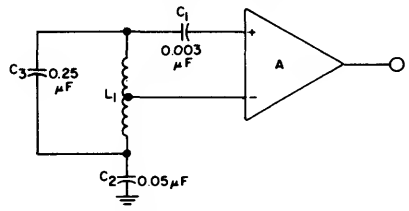
When two units are cascaded, it is preferred to let amplifiers A_2 and A_3 be the input units, and amplifiers A_1 and A_4 be the output units. This arrangement permits separation of both the V_{CC} and ground lines for low- and high-level signals.

If resistive decoupling is used, amplifiers A_2 and A_3 can be operated at lower V_{CC} voltages to effect a savings in current consumption.

Hartley Oscillator

The Hartley oscillator is easily designed and constructed using the CA3048 amplifier. No feedback capacitor is required, and it is possible to extract "square", sawtooth, or sinusoidal waveshapes.

In the circuit shown in Fig. 7, the tap on the coil is located at one-fourth the total turns, capacitors C_1 and C_2 provide dc blocking, and capacitor C_3 tunes with inductor L_1 ($\omega_o = 1/\sqrt{L_1C_3}$). When the circuit is operated from a 12-volt supply, the output voltage is a clipped sine wave that has a peak-to-peak value of about 7 volts. The voltage at the inverting input is a sawtooth that has a peak-to-peak value of about 0.300 volt. If an unclipped sine wave is desired, it is available across the coil L_1. A sine wave can be obtained in the single-ended connection if the value of C_2 is made large with respect to C_3 so that it effectively bypasses the sawtooth to ground; the voltage across L_1 is then sinusoidal with respect to ground.



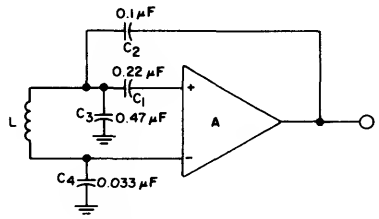
A IS ANY AMPLIFIER OF THE CA3048

Fig. 7 - Hartley oscillator.

Colpitts Oscillator

A tunable Colpitts oscillator is readily designed using one of the amplifiers of the CA3048 array. Fig. 8 shows an example of the CA3048 used in this way. Capacitors C_1 and C_2 are dc blocking capacitors; the series combination of capacitors C_3 and C_4 resonates with coil L. The ratio of C_3 to C_4 determines the relative amounts of signal fed back to the two inputs, and may be chosen on the basis of stability or strength of oscillation.

For the component values shown in Fig. 8, the frequency of oscillation is 33.536 kHz with a 12-volt supply and decreases to 33.546 kHz when the supply voltage is reduced 25 per cent to 9 volts.



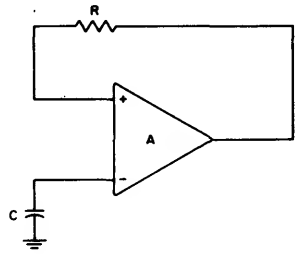
A IS ANY AMPLIFIER OF THE CA3048

Fig. 8 - Colpitts oscillator.

Three waveshapes are available from the Colpitts oscillator. A sawtooth waveform is obtained at the output, a sinusoidal waveform is obtained at the inverting input, and a clipped sinusoidal waveform appears at the noninverting input.

Astable Multivibrator

The CA3048 may be connected as an astable multivibrator with the addition of only two external components. An example of this type of operation is shown in Fig. 9.



A IS ANY AMPLIFIER OF THE CA3048

Fig. 9 - Astable multivibrator.

The resistor R introduces positive feedback into the circuit, and the capacitor C sets the period of the waveform. The operation of the circuit can be explained more easily if it is assumed that transistor Q_{17} (of amplifier A_3) has just turned OFF so that the voltage at terminal No. 11 becomes very positive. This positive voltage is fed through R to the base of Q_{19} to maintain the conduction of this transistor and to hold transistors Q_{21}, Q_{13}, Q_{14}, and Q_{17} cut off. Meanwhile, capacitor C charges through the internal bias resistors R_{41} and R_{42}. When the voltage on capacitor C reaches the level at which transistor Q_{21} begins to become forward-biased, some current is diverted from Q_{20} to Q_{21} and Q_{13}, Q_{14}, and Q_{17} begin to turn ON. The action is regenerative because the negative-going voltage from the collector of Q_{17} feeds a negative-going signal back to the base of Q_{19} to enhance the switching action. When C discharges to the point at which Q_{21} turns OFF, Q_{20} begins to turn ON and the process repeats itself.

Two waveforms are available from the astable multivibrator circuit, both at low impedance. A rectangular waveform that has a peak-to-peak amplitude of 7 volts or greater is obtained from the output terminal. The waveform available at the inverting input is an isosceles triange that has a peak-to-peak amplitude of approximately 0.220 volt.

With the circuit as shown, reliable oscillation is obtained for values of the resistor R in the order of 2.2 megohms, with supply voltages as low as six volts.

4-Channel Linear Mixer

Fig. 10 illustrates the use of the CA3048 as a linear mixer. Each input is connected to its own CA3048

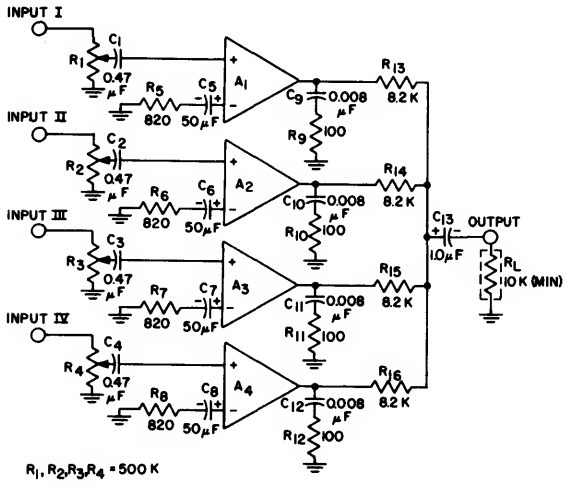


Fig. 10 - Linear mixer.

amplifier through the gain-control potentiometers R_1, R_2, R_3, and R_4. Capacitors C_1, C_2, C_3, and C_4 block the dc voltage at the inputs.

The gain of any input to the corresponding output is 20 dB for the circuit values shown and a load impedance of 10000 ohms or greater. Resistors R_5, R_6, R_7, and R_8 program the gain of the system, and may be varied to provide more or less gain, depending on the requirements of the application. The curve in Fig. 11 illustrates the effect of variation in the resistance in the feedback circuit of the CA3048. The difference in the 20 dB gain indicated for the mixer circuit and the approximately 34 dB shown in Fig. 12 results from the loss in the combining circuit that consists of R_{13}, R_{14}, R_{15}, R_6, and R_L.

A resistor-capacitor combination (R_9, C_9, R_{10}, C_{10}, R_{11}, C_{11}, R_{12}, C_{12}) connected to the output of each amplifier stabilizes the amplifiers when source and load conductances are too small to provide adequate damping.

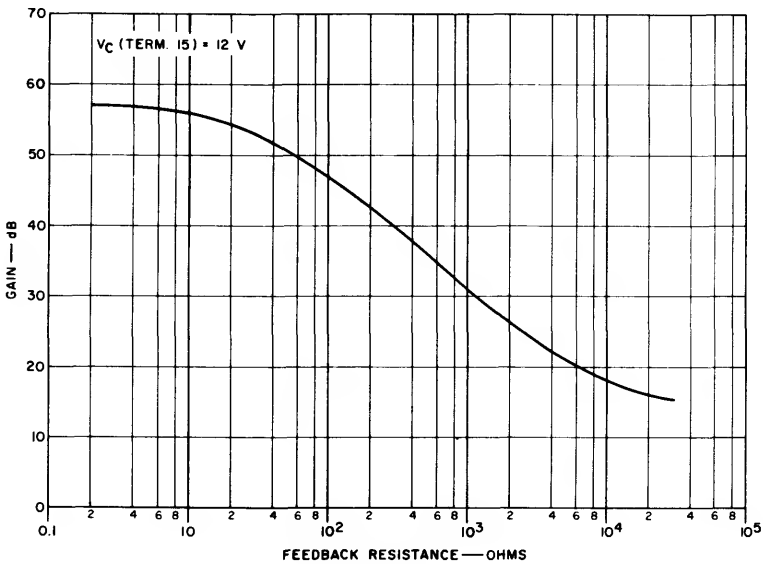


Fig. 11 - Gain of a CA3048 amplifier as a function of feedback resistance.

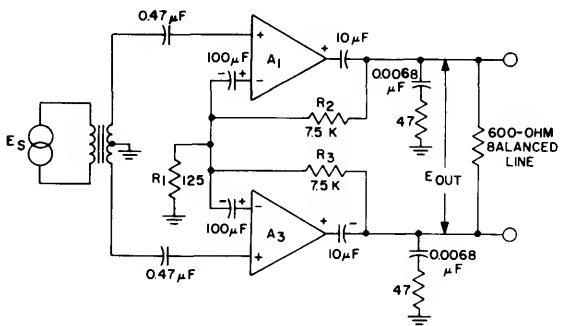


Fig. 12 - Balanced-line driver.

The input impedance of each amplifier of the CA-3048 is nominally 90 kilohms. In the linear mixer, however, the input potentiometers R_1 through R_4 are 500 kilohms. The effective impedance presented to the device, therefore, is quite high except when the circuit is adjusted for maximum gain. At this time, the impedance decreases to about 75 kilohms.

Driver for 600-ohm Balanced Line

Two amplifiers of the CA3048 may be connected to drive a 600-ohm balanced line at levels up to 1 volt rms with a gain of 40 dB. When the circuit is connected as shown in Fig. 12, the distortion is less than 1 per cent at an output level of 1 volt and a gain of 40 dB.

The output of the circuit is limited to a value slightly greater than 1 volt rms, primarily because of drive-current limitations to the output transistors. In this respect, it is self-protecting. Should a short circuit develop across the line, the circuit will not destroy itself.

Resistor R_1 in Fig. 12 is common to the output and input circuits of both amplifiers A_1 and A_3. Should a gain unbalance exist, or should the input signals be of unequal amplitude, then the outputs would tend to become unbalanced with respect to ground. For example, if amplifier A_1 had the larger output, a signal in phase with the output at A_1 would be developed across resistor R_1. In this event, the voltage developed at R_1 would tend to reduce the output of amplifier A_1 because this voltage is applied to the inverting input. At the same time, the voltage at R_1 is applied to the inverting input of amplifier A_3 and tends to increase the effective input voltage of that amplifier and, in this way, help to restore balance. The balancing effect takes place regardless of the cause of the initial unbalance.

Gain-Controlled Amplifier

Any amplifier of the CA3048 may be used as a gain-controlled amplifier in order to accommodate a wide range of input signal amplitude. Fig. 13 shows one amplifier of the CA3048 used in this type of configuration. By variation of the dc potential at the gate No. 1 of the MOS transistor Q_1, the gain of the amplifier may be varied from 14 dB to 49 dB. In this circuit, the MOS transistor Q_1 acts as a variable impedance in the feedback loop of the CA3048.

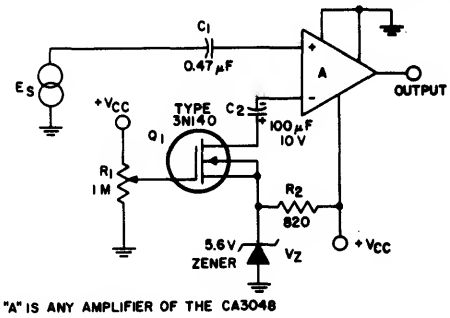


Fig. 13 - Gain-controlled amplifier.

In a circuit such as that shown in Fig. 13, the voltage gain may be expressed as follows:

$$\frac{E_o}{E_s} = \frac{A\,(R_a + R_f)}{R_f + R_a(A + 1)} \qquad (5)$$

where R_a is the equivalent resistance of the MOS transistor and R_f is the feedback resistance, which includes the internal feedback resistance of the integrated circuit together with any paralleled external feedback resistance.

As the value of resistor R_a approaches zero, the gain of the circuit approaches the open-loop gain of the amplifier (A). For very large values of resistor R_a the gain of the circuit approaches A/(A + 1), or approximately unity. The maximum theoretical agc range then is A.

The practical agc range of this circuit is limited on the high end by the "ON" resistance of the MOS transistor, and on the low end by the finite input impedance of the CA3048. In the circuit shown in Fig. 13, the range of control is 35 dB.

There is no necessity for direct current to flow in the MOS transistor, and if a low impedance source of about five volts is available, this voltage may be substituted for the Zener diode-resistor combination so that the power requirements of the circuit are further reduced.

Distortion, which is inherently low, ranges from 0.65 per cent at minimum gain (output of 2 volts rms) to 0.4 per cent at maximum gain.

ICAN-5269

Integrated Circuits For FM Broadcast Receivers

by R.L. Sanquini

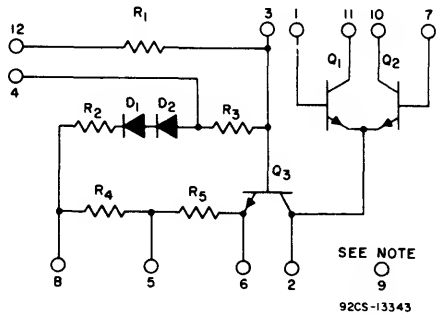
Silicon monolithic integrated circuits have certain design features which make them more attractive than discrete-component circuits for consumer electronic applications. These features include small size, light weight, high reliability, and more potential circuit functions per dollar of cost. Until recently, the major limitation to the extensive use of integrated circuits in commercial FM (88-to-108-MHz) broadcast receivers has been the relatively high cost of such circuits when they were designed to perform the same functions as their discrete-circuit counterparts. This limitation has now been removed by the introduction of high-reliability, low-cost, multifunction integrated circuits such as the RCA CA3005, CA3011, CA3012, CA3013, and CA3014. With these circuits, high-performance inexpensive FM receivers can be designed to meet the rigorous standards set by high-quality commercial FM receivers using vacuum tubes and transistors.

This note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

FM Tuner

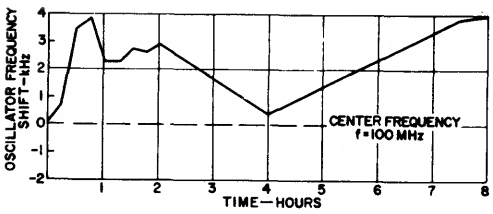
The CA3005 is the basic building block for the three front-end approaches discussed below. A schematic diagram of the CA3005 is shown in Fig. 1. Fig. 2 shows a single-chip front end that uses one CA3005 and a two-gang capacitor tuning system. The CA3005 performs the functions of rf amplifier, oscillator, and mixer in a unique manner.

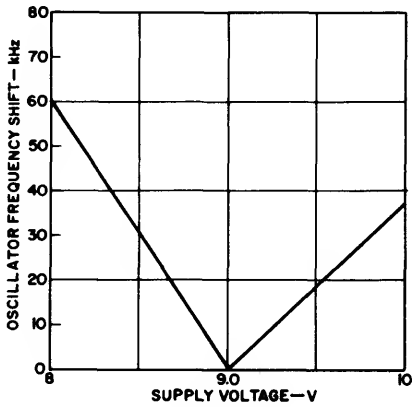
The circuit operation may best be explained by reference to Figs. 1 and 2. The first function of the current-sink transistor Q_3 in Fig. 1 is to supply the emitter currents for the differential-amplifier transistors Q_1 and Q_2. Positive feedback from the collector of Q_2 (terminal 10) to the base of Q_1 (terminal 1) through the 5-picofarad capacitor shown in Fig. 2 establishes the oscillator function; the frequency of oscillation is determined by the tuned circuit L_2 and C_2. Because the output impedance at the collector of Q_3 is high compared to the input impedance at the emitter of Q_1 and Q_2, Q_3 is isolated from Q_1 and Q_2 and receives very little oscillator signal. The rf input signal

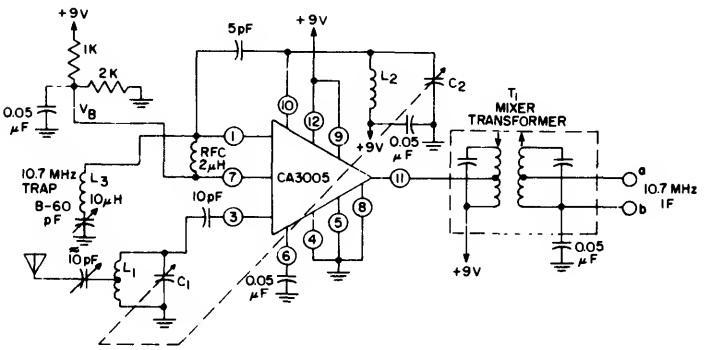


Note: Connect terminal 9 to most positive dc supply voltage.

Fig.1 - Schematic diagram of RCA CA3005 integrated-circuit rf amplifier.







L_1 – 4 turns of No. 22 wire, center-tapped; 1/4" O.D. coil form, "E" mat'l slug

L_2 – 6 turns No. 32 wire on toroid core; Radio Industries Inc., 1/4" O.D., No. 8 mat'l

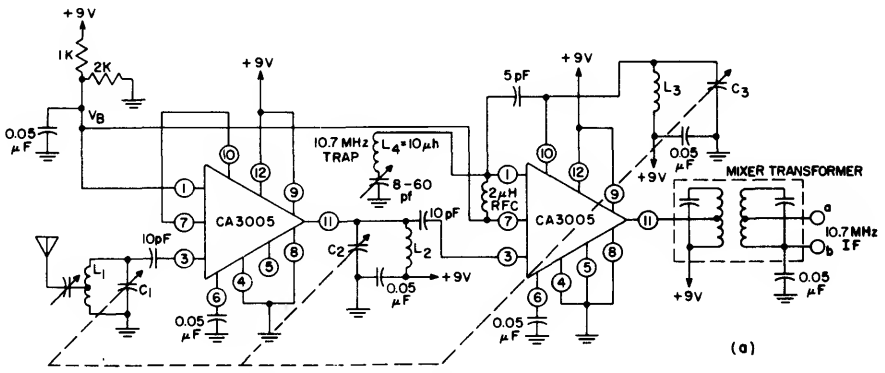
T_1 – TRW No. 21629, or equiv.

Fig.2 - Single-chip front end using the CA3005. Curves show oscillator stability with time and supply voltage.

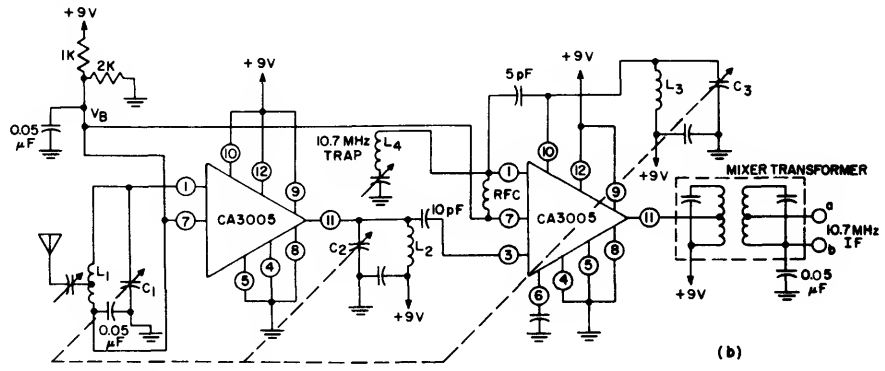
is applied to the base of Q_3 (terminal 3), amplified, and injected into the emitter of Q_1 and Q_2 to mix with the oscillator signal. The 10.7-MHz intermediate frequency is obtained from the collector of Q_1 (terminal 11).

The CA3005 draws a total current of 4.5 milliamperes from the +9-volt supply. The front end shown in Fig. 2 has a power gain of 15 dB and a sensitivity of 10 microvolts for 30 dB of quieting; it can handle a maximum input signal of 7 millivolts. Automatic frequency control can be applied to the oscillator in a conventional manner by connection of a voltage-dependent capacitor (diode) to the oscillator tuned circuit L_2 and C_2. Curves of oscillator stability as a function of time and supply voltage are also shown in Fig. 2.

The approach to the front end shown in Fig. 2, although economical, results in only adequate performance. Improved performance can be obtained by addition of an rf amplifier to the mixer-oscillator circuit, as shown in Fig. 3. In this figure, a CA3005 used as an rf amplifier and a three-gang capacitor tuning system are added to the basic single-chip circuit to provide higher power gain, lower noise figure, and improved selectivity. The CA3005 is connected as a cascode amplifier in Fig. 3(a) and in an emitter-coupled configuration in Fig. 3(b). Both configurations require no neutralization.



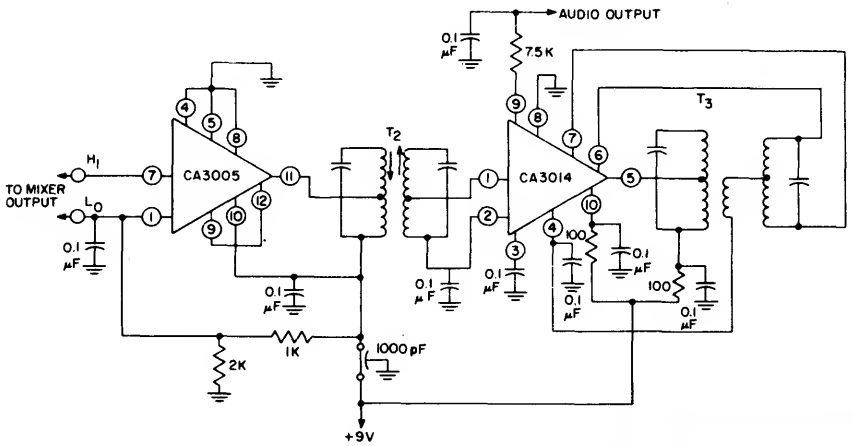
L_1 – 4 turns No.22 wire; center- tapped; 1/4-inch outer-diameter coil form; "E" material slug
L_2 – Same as L_1 without center tap
L_3 – 6 turns No.32 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No.8 material
Mixer Transformer – TRW No. 21629, or equiv.



L_1 – 4 turns of No.22 wire; center-tapped; 1/4-inch outer-diameter coil form; "E" material slug
L_2 – Same as L_1 without center tap
L_3 – 6 turns of No.22 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No.8 material
Mixer Transformer – TRW No. 21629, or equiv.

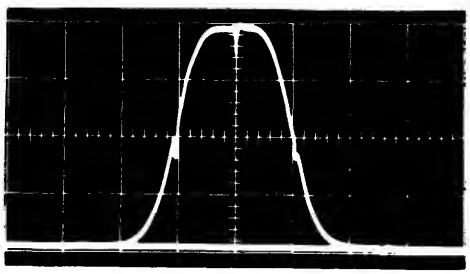
Fig.3 - Two-chip front ends using CA3005 rf amplifier connected (a) in cascode, and (b) in emitter-coupled configuration.

The cascode front end has a higher power gain (28 dB, as compared to 24 dB for the emitter-coupled configuration), but the emitter-coupled front end has better cross-modulation characteristics. The emitter-coupled amplifier can handle interfering signals up to about 15 millivolts with 10 per cent cross-modulation at maximum gain, while the capability of the cascode amplifier is limited to that of a single transistor.[1] The cascode front end has a sensitivity of 2 microvolts for 30 dB of quieting, while the emitter-coupled front end has a sensitivity of 3 microvolts. Reverse agc can be applied to both configurations by variations of the voltage at terminal 12 from 9 volts (maximum gain) to 3 volts (full cutoff) from a 0.5-milliampere agc source. Both amplifiers have a dynamic agc range of 60 dB.

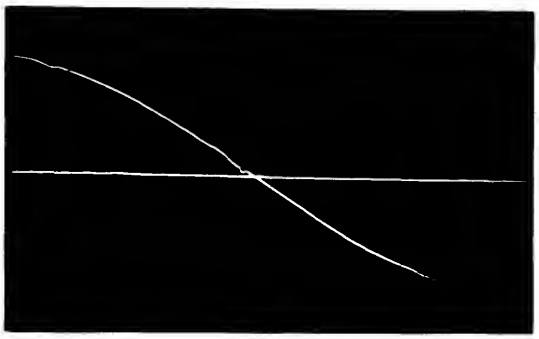


T_2 = TRW No. 22468 or equiv.

T_3 = TRW No. 21590 or equiv.



10.7-MHz IF SELECTIVITY CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)



DETECTOR "S" CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)

Fig.4 - Two-chip 10.7-MHz if amplifier, limiter, and discriminator using CA3005, CA3014, and Interstage transformer. Photographs show selectivity curve, detector "S" curve.

FM IF Amplifier, Limiter, and Detector

Fig. 4 shows a 10.7-MHz FM if strip and detector that uses a CA3005 and a CA3014 to provide 95 dB of gain. The schematic diagram of the CA3005 was shown in Fig. 1; the CA3014 schematic is shown in Fig. 5. The heart of both these integrated circuits is the differential amplifier, which is probably the best simple configuration on the market today for symmetrical limiting over a wide input-voltage range. The differential-amplifier configuration is also ideal for integration because the parameters that are most important in integrated-circuit design (matched V_{BE}, matched beta, and resistor ratios) are the easiest to control on a single silicon chip. In the FM if strip, therefore, three advantages are obtained: high performance, low cost, and fewer individual components.

The input limiting knee for the if strip shown in Fig. 4 is 30 microvolts. The recovered audio obtained from terminal 9 of the CA3014 is 220 millivolts rms. The if selectivity curve and the detector "S" curve are also shown in Fig. 4. The AM rejection referenced to a 30-percent modulated (FM and AM) signal with the AM signal at 30 millivolts is 50 dB.

The 10.7-MHz if-amplifier circuit of Fig. 4 operates as follows: The 10.7-MHz FM signal from the mixer is applied to terminal 7 of the CA3005. The gain from this point to the input of the CA3014 is 25 dB. The interstage transformer T_2 is designed so that the collector output of the CA3005 at terminal 1 does not saturate. As a result, bandpass spreading is kept to a minimum over large swings in input voltage. The 10.7-MHz FM signal receives additional gain of 70 dB and limiting from terminal 1 to terminal 5 in the CA3014. The FM output at terminal 5 is applied to the primary winding of the phase-shift (discriminator) transformer T_3. The secondary winding, which is connected to terminals 6 and 7, is in quadrature with the primary voltage at the center frequency, 10.7 MHz. As the FM signal varies, the phase shift of the secondary voltage follows the modulation. The detected output at the base of Q11 in the CA3014 (terminals 6 and 7) is thus amplified and buffered. The recovered audio is taken from the low-impedance terminal 9.

If more selectivity in the if strip is desired, an additional double-tuned transformer can be added to the circuit.

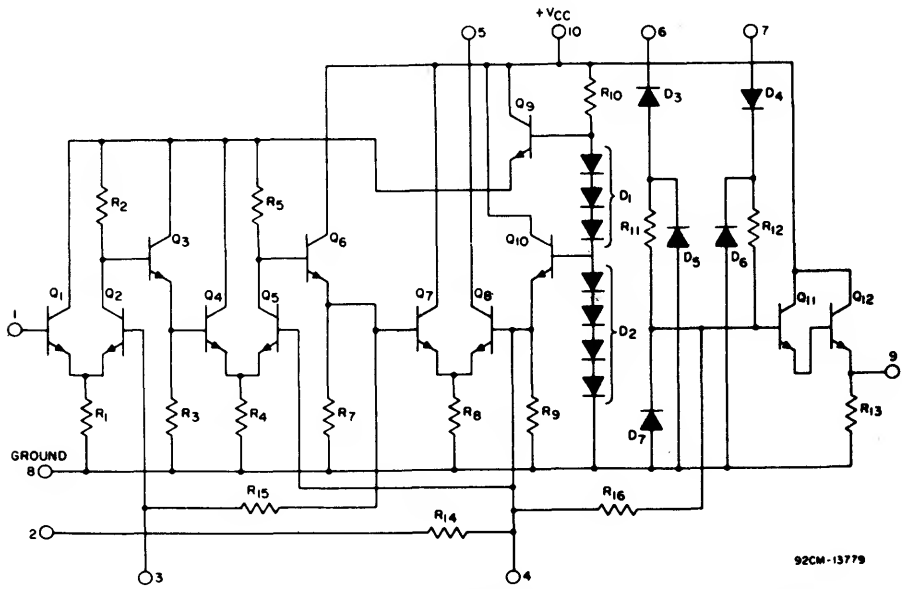


Fig. 5 - Schematic diagram of RCA CA3014 wide-band amplifier-discriminator.

Fig.6 shows an approach in which the two transformers areplaced immediately after the mixer stage. Fig.7 shows the details of the input filter and Fig.8 shows the schematic of the CA3012 used in the if stages of this circuit. When the transformers (10.7-MHz filter) are placed immediately after the mixer, better adjacent-channel rejection is obtained.

References

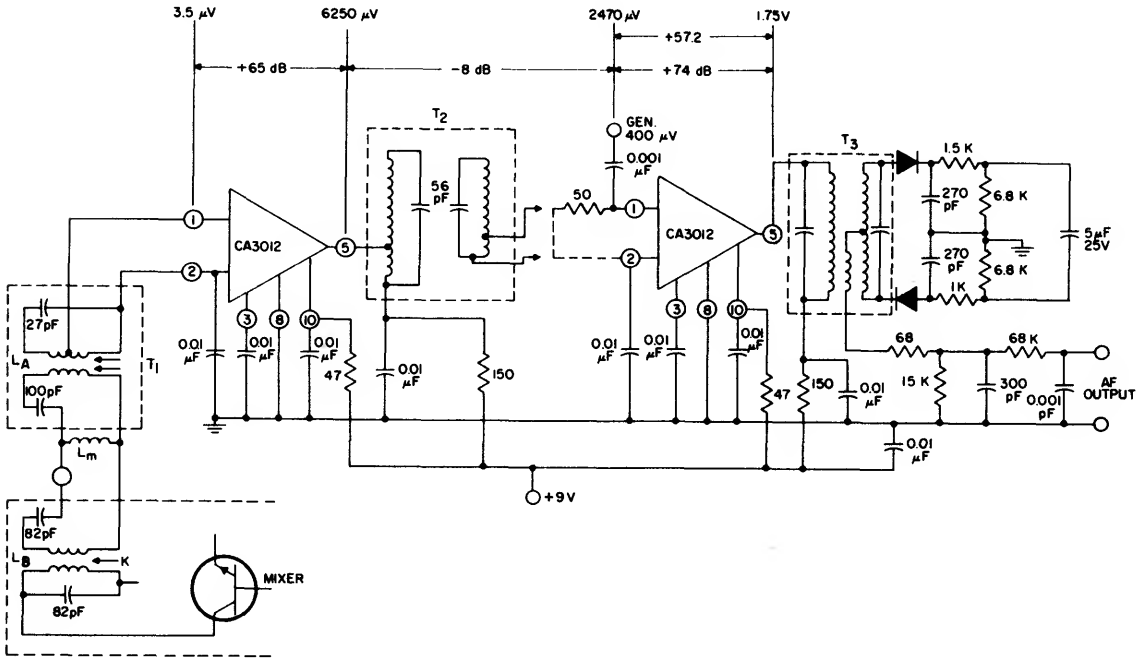
1. "Application of RF Amplifier-Mixer Integrated Circuits CA3004, CA3005, and CA3006," RCA APPLICATION NOTE ICAN-5022, November 1965

2. Mischa Schwartz, INFORMATION TRANSMISSION MODULATION AND NOISE, McGraw-Hill Book Company, 1959

3. J. Avins, "It's a television first. . . receivers with integrated circuits," ELECTRONICS, March 21, 1966

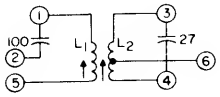
4. RCA Technical Bulletins: CA3005, CA3011-3012, CA3013-3014

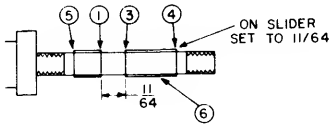
5. R. L. Sanquini, "Multipurpose Chips Cut Costs of FM Receiver," ELECTRONICS, May 16, 1966



T_1 - for details see Fig.7
T_2 - TRW No.22960-R2 or equiv.
T_3 - TRW 23148 or equiv.

Fig.6 - 10-MHz if amplifier and detector.





Winding 1-5 - 17 turns #36SE or equiv., $Q_\mu \approx 70$
Winding 3-4 - 40 turns #36SE or equiv., $Q_\mu \approx 75$
Winding 4-6 - 5 turns max; RX-Meter-900 ohms (no load)
Tuning slug: Winding 1-5 - Carbonyl TH or equiv., 1/4" long
Winding 3-4 - Carbonyl TH or equiv., 5/16" long
Front End: $KQ \leq 1$, $Lm = K\sqrt{LA\ LB} = 0.049\ \mu H$

TEST CIRCUIT:

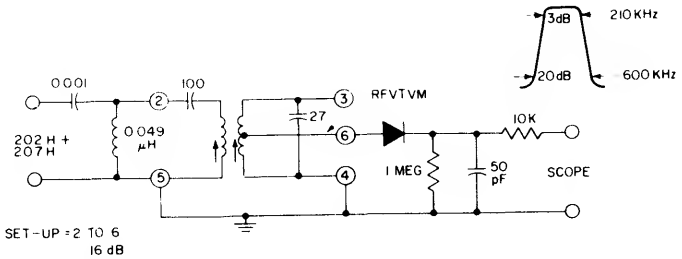
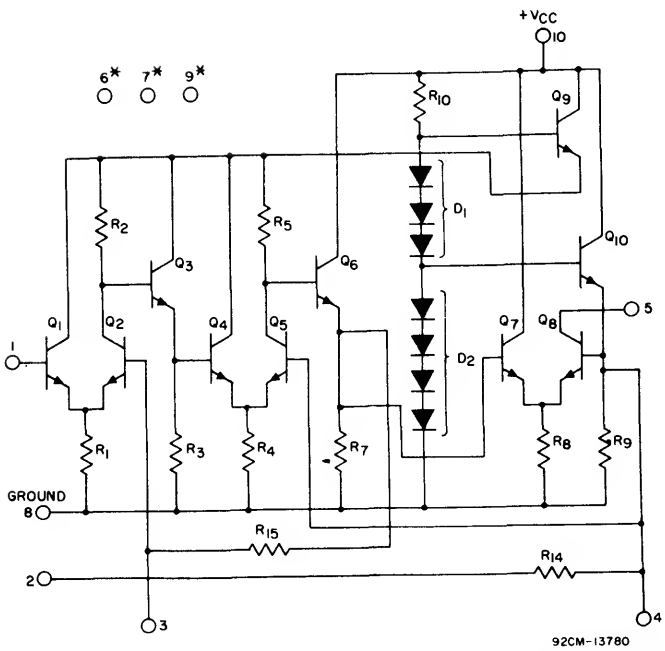


Fig.7 - Details of 10.7-MHz input filter, T_1.



92CM-13780

* Internal Connection - Do Not Use
Note: R_6 Deleted

Fig.8 - Schematic diagram of RCA CA3012 wide-band amplifier.

Application Of The RCA-CA3018 Integrated-Circuit Transistor Array

by G.E. Theriault, A.J. Leidich, and T.H. Campbell

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers. Because the CA3018 has the feature of device balance, it is useful in special applications of the differential amplifier, and can be used to advantage in circuits which require temperature compensation of base-to-emitter voltage.

CIRCUIT DESCRIPTION AND OPERATING CHARACTERISTICS

The circuit configuration for the CA3018 is shown in Fig. 1. In a 12-lead TO-5 package, because it is necessary to provide a terminal for connection to the substrate, two transistor terminals must be connected to a common lead. The particular configuration chosen is useful in emitter-follower and Darlington circuit connections. In addition, the four transistors can be used almost independently if terminal 2 is grounded or ac grounded so that Q3 can be used as a common-emitter amplifier and Q4 as a common-base amplifier. In pulse video amplifiers and line-driver circuits, Q4 can be used as a forward-biased diode in series with the emitter of Q3. Q3 may be

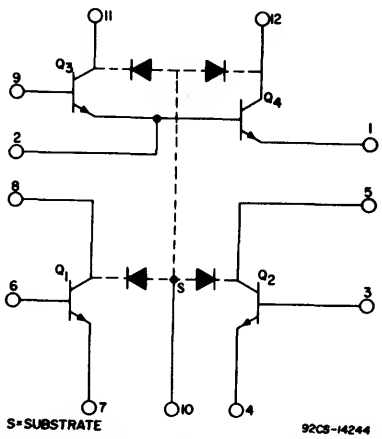


Fig. 1—Schematic diagram and TO-5 terminal connections for the CA3018 integrated-circuit transistor array.

used as a diode connected to the base of Q4; in a reverse-biased connection, Q3 can serve as a protective diode in rf circuits connected to operational antennas. The presence of Q3 does not inhibit the use of Q4 in a large number of circuits.

In transistors Q1, Q2, and Q4, the emitter lead is interposed between the base and collector leads to minimize package and lead capacitances. In Q3, the substrate lead serves as the shield between base and collector. This lead arrangement reduces feedback capacitance in common-emitter amplifiers, and thus extends video bandwidth and increases tuned-circuit amplifier gain stability.

Operating characteristics for the CA3018 are given in the technical bulletin.

CIRCUIT APPLICATIONS

The applications for the CA3018 are many and varied. The typical applications discussed in this Note have been selected to demonstrate the advantages of four matched devices available on a single chip. These few examples should stimulate the generation of a great many more applications.

Video Amplifiers

A common approach to video-amplifier design is to use two transistors in a configuration designed to reduce the feedback capacitance (appearing as a Miller capacitance) inherent in a single triode device. Three configurations which utilize two devices are (1) the cascode circuit, (2) the single-ended differential-amplifier, and (3) the common-collector, common-emitter circuit. In all three circuits, the output-to-input feedback capacitance is minimized by isolation inherent in the configuration. The availability of four identical transistors in a common package provides a convenient vehicle for these circuit configurations for video-amplifier design. Two of the many possible circuit variations are discussed below.

Broadband Video Amplifier. A broadband video-amplifier design using the CA3018 is shown in Fig. 2. This amplifier may be considered as two dc-coupled stages, each consisting of a common-emitter, common-collector configuration. The common-collector transistor provides a low-impedance source to the input of the common-emitter transistor and a high-impedance, low-capacitance load at the common-emitter output. Iterative operation of the video amplifier can be achieved by capacitive coupling of stages.

Two feedback loops provide dc stability of the broadband video amplifier and exchange gain for bandwidth. The feedback loop from the emitter of Q_3 to the base of Q_1 provides dc and low-frequency feedback; the loop from the collector of Q_4 to the collector of Q_1 provides both dc feedback and ac feedback at all frequencies.

The frequency response of the broadband video amplifier is shown in Fig. 3. The upper 3-dB break occurs at a frequency of 32 MHz. The low-frequency 3-dB characteristics are determined primarily by the values of capacitors C_1, C_2, and C_3. The low-frequency 3-dB break

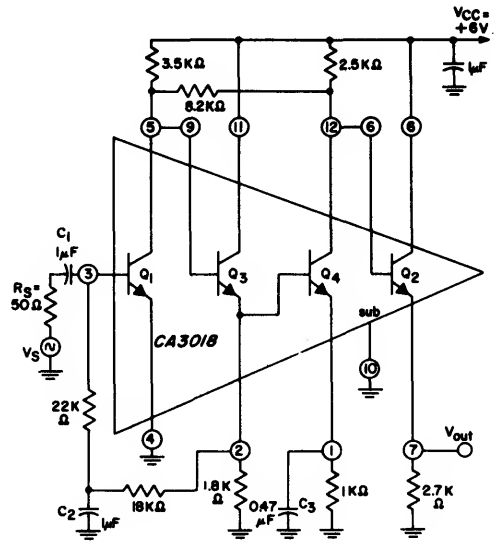


Fig. 2—Schematic diagram for a CA3018 broadband video amplifier.

occurs at 800 Hz. The mid-frequency gain of 49 dB is constant to within 1 dB over the temperature range from −55° to +125°C. The upper 3-dB break is constant at 32 MHz from −55°C to +25°C, and drops to 21 MHz at +125°C.

The total power dissipation over the entire temperature range is 22.8 milliwatts. The dc output voltage varies from 2.33 volts at −55°C to 3 volts at +125°C. The tangential sensitivity occurs at 20 microvolts peak-to-peak. The dynamic range is from 20 microvolts peak-to-peak to 4 millivolts rms at the input.

The circuit of Fig. 2 demonstrates a typical approach that can be altered, especially with regard to gain and bandwidth, to meet specific performance requirements.

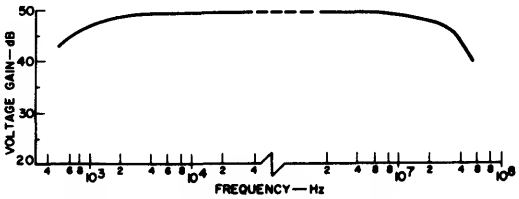


Fig. 3—Voltage gain as a function of frequency for the broadband video amplifier of Fig. 2.

Cascode Video Amplifier. The cascode configuration offers the advantages of common-emitter gain with reduced feedback capacitance and thus greater bandwidth. Fig. 4 shows a typical circuit diagram of a cascode video amplifier using the CA3018. Transistors Q_2 and Q_1 comprise the common-emitter and common-base portions of

the cascode, respectively. The common-base unit is followed by cascaded emitter followers (Q_3 and Q_4) which provide a low output impedance to maintain bandwidth for iterative operation.

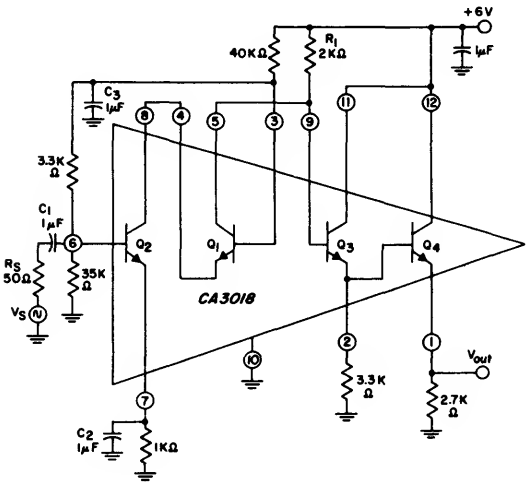


Fig. 4—Schematic diagram for a CA3018 cascode video amplifier.

The frequency response of the cascode video amplifier is shown in Fig. 5. The lower and upper 3-dB points occur at frequencies of 6 KHz and 11 MHz, respectively. The lower 3-dB point is primarily a function of capacitors C1, C2, and C3. The upper 3-dB point is a function of the devices and of the load resistor R_1, and is 10.5 MHz at −55°C and 5 MHz at +125°C.

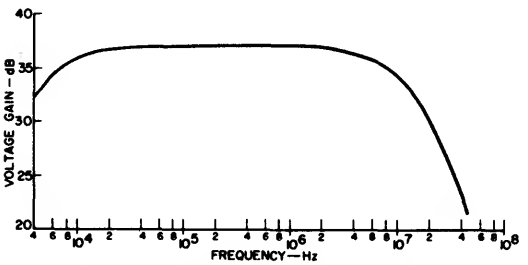
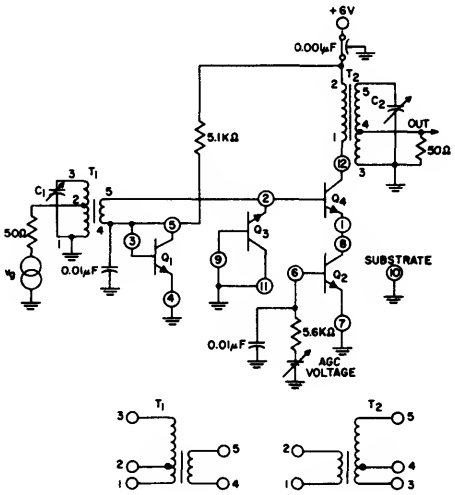


Fig. 5—Voltage gain as a function of frequency for the cascode amplifier of Fig. 4.

The mid-frequency voltage gain of the amplifier is 37 dB ± 1 dB over the temperature range from −55°C to +125°C. The power dissipation varies from 16.8 milliwatts at −55°C to 17.6 milliwatts at +125°C. The amplifier has a tangential sensitivity of 40 microvolts peak-to-peak and a useful dynamic input range from 40 microvolts to 16.6 millivolts peak-to-peak.

15-MHz RF Amplifier

Fig. 6 shows a typical design approach for a tuned amplifier for use in the frequency range of 2 to 30 MHz in military receivers. This circuit was designed for a mid-band frequency of 15 MHz to demonstrate its capability. Gain is obtained in a common-emitter stage (Q_4). Transistor Q_2 is used as a variable resistor in the emitter of Q_4 to provide improved signal-handling capability with agc. Transistor Q_1 is used as a bias diode to stabilize Q_4 with temperature, and the reverse breakdown of Q_3 as a diode is used to protect the common-emitter stage from signal overdrive of adjacent transmitters.



L = 0.8 μH	L = 0.8 μH
Q_o = 200	Q_o = 200
T_{1-3} = 6T	T_{3-5} = 6T
T_{1-2} = 1T	T_{1-2} = 4T
T_{4-5} = 2T	T_{3-4} = 1T

#22 wire on Q-2 material, CF107 Torroid from Indiana General.

C_1, C_2 = Arco 425 or equiv.

Fig. 6—Schematic diagram for a CA3018 15-MHz rf amplifier.

The tuned-circuit design of Fig. 6 utilizes mismatching to obtain stability. Although the usable stable gain for a common-emitter amplifier using this type of transistor is 26 dB at 15 mHz, the tuned rf amplifier was designed for a total gain of 20 dB to obtain greater stability and more uniform performance with device variations. The general performance characteristics of the circuit are as follows:

Power Gain	20 dB
Power-Gain Variation from −55 to +125°C	±1 dB

Bandwidth	315 kHz
Noise Figure at Full Gain	7.4 dB
AGC Range	45 dB
Power Dissipation	1.8 mW

Fig. 7 shows the cross-modulation characteristics of the circuit for in-band signals. For out-of-band undesired signals, the cross-modulation performance is improved by the amount of attenuation provided by the input tuned circuit. Cross-modulation performance also improves (i.e. more interfering signal voltage is required for cross-modulation distortion of 10 per cent) with increased agc as a result of the degeneration in the emitter of Q_4.

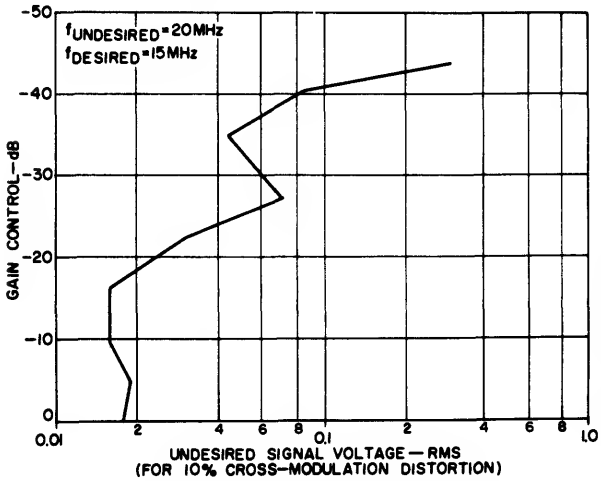


Fig. 7—In-band cross-modulation characteristic of 15-MHz amplifier of Fig. 6 (data taken with untuned input).

Final If Amplifier Stage and Second Detector

Fig. 8 illustrates the use of the CA3018 as a last if amplifier and second detector (0.1 volt emitter voltage on terminal 1). The bias on transistor Q_4 is maintained at approximately cutoff to permit the cascaded emitter-follower configuration (Q_3 and Q_4) to be used as a second detector. Because this stage is driven by a common collector configuration, the input impedance to the detector can be kept high. A low output load impedance can be used as a result of the output current capability of the cascaded emitter-follower configuration. The input impedance (terminal 9) of approximately 9000 ohms is largely determined by the bias network. A minimum if input power of 0.4 microwatt must be delivered to terminal 9 for linear operation. The audio output power for 60 per cent modulation for this drive condition is 0.8 microwatt. Linear detection is obtained through an input range of 20 dB for 60 per cent modulation. This detector arrangement requires less power-output capability from the last if amplifier than a conventional diode detector yet allows a low dc load resistor to achieve a good ac-to-dc ratio for the first audio amplifier.

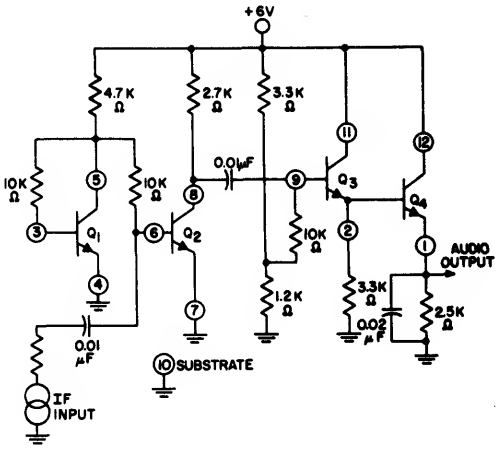


Fig. 8—Schematic diagram for a CA3018 final if amplifier and second detector.

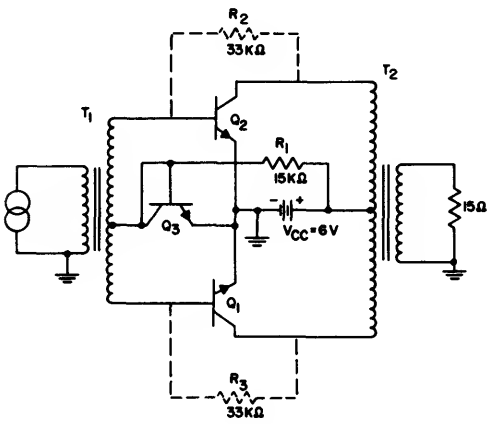
The if amplifier of Fig. 8 has a voltage gain of 30 dB at 1 MHz. Transistor Q_1 is used in the base-bias loop of the common-emitter amplifier Q_2 to stabilize the output operating point against temperature variations. This arrangement also eliminates the need for an emitter resistor and bypass capacitor, and thus provides a larger voltage-swing capability for Q_2. If Q_2 is biased conventionally with base-bias resistors, Q_1 can be made available for the first audio or agc amplifier.

Class B Amplifier

Characteristics were obtained on a low-level class B amplifier to establish the idling-current performance of nearly identical devices on a single chip with respect to temperature variations. The transistors in the CA3018 can be used only for low-power class B operation (maximum output of 40 milliwatts) because of the h_{FE} roll-off and moderately high saturation resistance at high currents. A typical circuit is shown in Fig. 9. Idling-current bias is provided to Q_1 and Q_2 by use of transistor Q_3 as a diode (with collector and base shorted) and connection of a series resistor to the supply. The idling current for each transistor in the class B output is equal to the current established in the resistance-diode loop. Because the resistor R_1 is the predominant factor in controlling the current in the bias loop, the bias current is relatively independent of temperature. In addition, because the devices have nearly equal characteristics and are at the same temperature, the idling current is nearly independent through the full military temperature range. The total idling current for transistors Q_1 and Q_2 in Fig. 9 varies from 0.5 to 0.6 milliampere from -55 to $+125$°C. Excellent balance between output devices is achieved throughout the range.

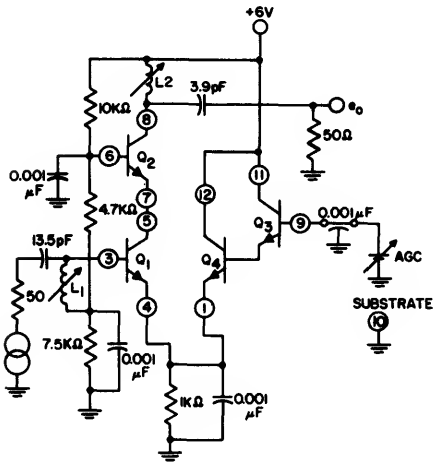
AC feedback as well as dc feedback can be obtained by substitution of two resistors R_2 and R_3 in place of R_1,

as shown by the dotted lines in Fig. 9. These two resistors, which have a parallel combination equal to R_1, are connected between collector and base of transistors Q_2 and Q_1. The added feedback reduces the power gain by approximately 6 dB (30 to 24 dB), but improves the linearity of the circuit. Although the output-power capability for the circuit shown in Fig. 9 is approximately 18 milliwatts, output levels up to 40 milliwatts can be obtained in similar configurations with optimized components.



T_1 — ADC Products No. 5SX1322 or equiv.
T_2 — Chicago Standard Trans. Corp. No. TA-10 or equiv.
Note: R_1 is removed when R_2 and R_3 are added.

Fig. 9—Schematic diagram for a CA3018 class B amplifier.



L_1 = 0.11 to 0.17 μH
L_2 = 0.5 to 0.8 μH

Fig. 10—Schematic diagram for a CA3018 100-MHz cascode amplifier.

100-MHz Tuned RF Amplifier

Fig. 10 illustrates the use of the CA3018 in a 100-MHz cascode circuit with an agc amplifier. Transistors Q_1 and Q_2 are used in a cascode configuration, and transistors Q_3 and Q_4 are used to provide an agc capability and amplification. With a positive-going agc signal, current in the cascode amplifier is transferred to the Darlington configuration by differential-amplifier action. This agc amplifier has the advantage of low-power drive (high input impedance). In addition, the emitter of Q_1 can be back-biased with respect to the base to provide larger input-signal-handling capability under full agc conditions.

The operating characteristics of the amplifier shown in Fig. 10 are as follows:

Power Gain	— 26 dB
Agc Range	— 70 dB
3-dB Bandwidth	— 4.5 MHz
Noise Figure	— 6.8 dB
Power Dissipation	— 7.7 mW

The response characteristic is shown in Fig. 11

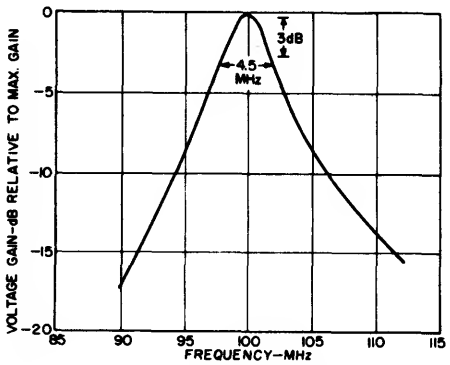


Fig. 11—Response characteristic of 100-MHz amplifier of Fig. 10.

ICAN-5299

Application Of The RCA-CA3019 Integrated-Circuit Diode Array

by G.E. Theriault and R.G. Tipping

The RCA-CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits.

The CA3019 features all-monolithic-silicon epitaxial construction designed for operation at ambient temperatures from −55°C to 125°C. It is supplied in a 10-terminal TO-5 low silhouette package.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, the CA3019 is particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes.

CIRCUIT CONFIGURATION AND OPERATING CHARACTERISTICS

Fig. 1 shows the circuit diagram and terminal connections for the CA3019. Diodes D_1 through D_4 are internally interconnected to form a diode quad, while diodes D_5 and D_6 are available as independent diodes. Each diode is formed from a transistor by connection of the collector and the base to form the diode anode and use of the emitter for the diode cathode (this technique is one of five methods by which the transistor structure can be utilized as a diode). This diode configuration, in which the collector-base junction is shorted, is the most useful connection for a high-speed diode because it has the lowest storage time. The only charge stored is that in the base. This configuration also exhibits the lowest forward voltage drop, and is the only one which has no p-n-p transistor action to the substrate. The diode has the emitter-to-base reverse breakdown voltage characteristic (typically 6 volts).

The monolithic process produces a substrate diode between the collector of a transistor and its supporting substrate, as shown in Fig. 2. Connected at each diode anode, therefore, is the cathode of a substrate diode for which the anode is the substrate (terminal 7). In some applications, the substrate can be left floating because a forward bias on any substrate diode creates a self reverse-bias on

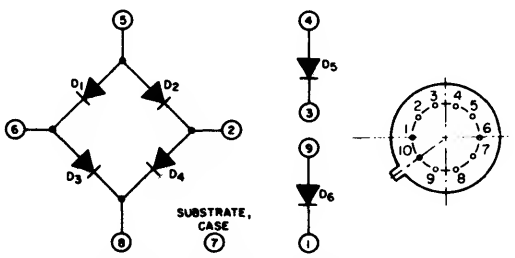
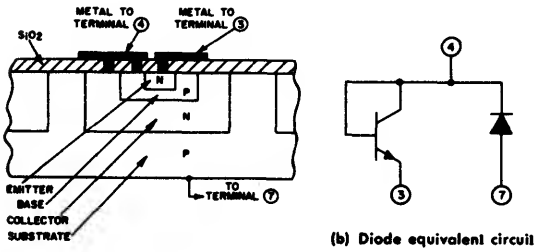


Fig. 1—Schematic diagram and terminal connections for the CA3019 integrated-circuit diode array.

the other substrate diodes. However, the uncertainty of this bias and the capacitive feedthrough paths provided by the substrate make it advisable to apply a reverse bias to all substrate diodes by returning the substrate through terminal 7 to a dc voltage which is more negative than the most negative voltage on a diode anode. Such reverse bias is most important when ac circuit balance is essential because the capacitance of the substrate diodes is a nonlinear function of the voltage across them. In such circuits, the changing capacitance of these parasitic elements can make good balance over a wide dynamic range impossible.



(a) Cross section of monolithic diode structure

(b) Diode equivalent circuit

Fig. 2—Diagram and equivalent circuit of the monolithic array.

Reverse bias of the substrate diodes is always indicated, therefore, and should be omitted only if the inclusion of such bias is not possible or practical. Terminal 7 may be returned to a negative power supply as long as the combined value of that supply voltage and the maximum positive voltage on any diode anode does not exceed the maximum rating of 25 volts. In systems that use single power supplies, the active circuit may be raised above ground potential and the signals coupled into the diodes by capacitive or inductive means.

The operating characteristics of the CA3019 integrated diode array are determined primarily by the individual diode characteristics, which are given in the technical bulletin.

APPLICATIONS

Although there are many possible applications for the CA3019, this note describes a few practical circuits to stimulate the thinking of the potential user. Besides the obvious uses as separate diodes and possible quad combinations, some of which are covered in the following discusssion, it should be noted that shorting of terminals 2 and 6 in the quad effectively provides two diodes in series. This diode connection can be used as the elements of special balanced mixers, as ring modulators, and as compensating networks that provide two diode drops. Fig. 3 shows an example of a typical synthesizer mixer circuit.

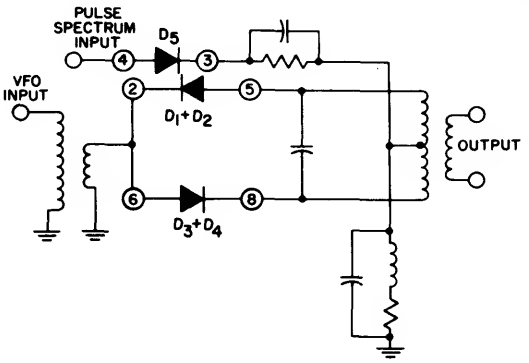


Fig. 3—Typical synthesizer mixer circuit.

Shorting of terminals 5 and 8 provides two independent sets of back-to-back diodes useful for limiting and clipping, as shown in Fig. 4.

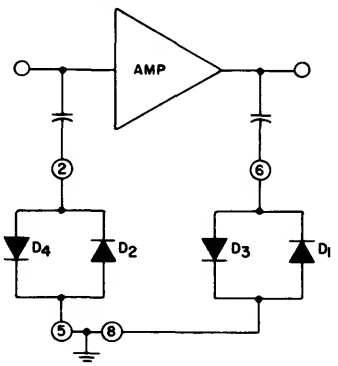


Fig. 4—Limiters using the CA3019.

Balanced Modulator

Fig. 5 shows the use of the CA3019 as a balanced modulator which minimizes the carrier frequency from the output by means of a symmetrical bridge network. A carrier of one polarity causes all the diodes to conduct, and thus effectively short-circuits the signal source. A carrier of the opposite polarity cuts off all the diodes and allows signal current to flow to the load. If the four diodes are identical, the bridge is perfectly balanced and no carrier current flows in the output load. Table I lists the characteristics of the balanced modulator.

High-Speed Gates

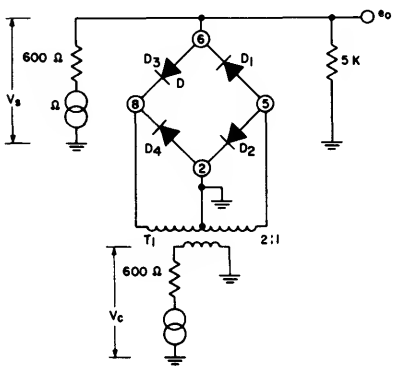
In high-speed gates, the gating signal often appears at the output and causes the output signal to ride a "pedestal." A diode-quad bridge circuit can be used to balance out the undesired gating signal at the output and reduce the pedestal to the extent that the bridge is balanced.

TABLE I. CHARACTERISTICS OF BALANCED MODULATOR OF FIG.5

Carrier Voltage VRMS at 30 KHz	0.75		0.75		0.75		0.50		1.0	
Signal Voltage mVRMS at 2 KHz	77		245		770		245		245	
Output Frequency KHz	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*	*Output Voltage mV rms*	*db Below Vs*
28 and 32*	34	6.5	115	7	440	5	51	14	170	3
30	0.7	41	0.82	49	2.6	50	0.1	68	3.6	37
26 and 34	0.02	72	0.05	72+	0.48	64	0.04	72+	0.07	71
24 and 36	0.03	69	0.49	54	60	22	0.58	52.5	0.6	53
22 and 38	0.001	72+	0.01	72+	1.4	55	.015	72+	0.02	72+

* Double-Sideband, Suppressed-Carrier Output.

All other outputs are spurious signals.

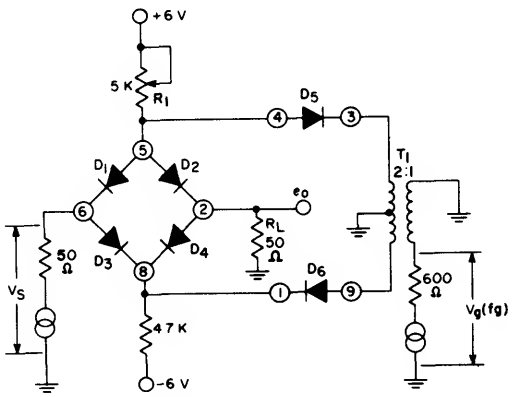


T_1 — Technitrol No. 8511660 or equiv.

Fig. 5—Balanced modulator using the CA3019.

A diode-quad gate functions as a variable impedance between a source and a load, and can be connected either in series or in shunt with the load. The circuit configuration used depends on the input and output impedances of the circuits to be gated. A series gate is used if the source and load impedances are low compared to the diode back resistance, and a shunt gate is used if the source and load impedances are high compared to the diode forward resistance.

Series Gate. Fig. 6 shows the use of the CA3019 as a series gate in which the diode bridge, in series with the load resistance, balances out the gating signal to provide a pedestal-free output. With a proper gating voltage (1 to 3 volts rms, 1 to 500 kHz), diodes D_5 and D_6 conduct during one half of each gating cycle and do not conduct during the other half of the cycle. When diodes D_5 and D_6 are conducting, the diode bridge (D_1 through D_4) is not conducting and the high diode back resistance prevents the input signal V_s from appearing across the load resistance R_L; when diodes D_5 and D_6 are not conducting, the diode bridge conducts and the low diode forward resistance allows the input signal to appear across the load resistance. Resistor R_1 may be adjusted to minimize the



T_1 — Technitrol No. 8511666 or equiv.

Fig. 6—Series gate using the CA3019.

gating voltage present at the output. The substrate (terminal 7) is connected to the −6-volt supply. Fig. 7 shows the on-to-off ratio of the series gate as a function of frequency.

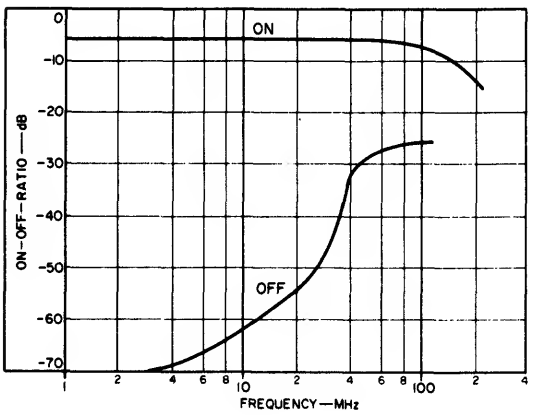
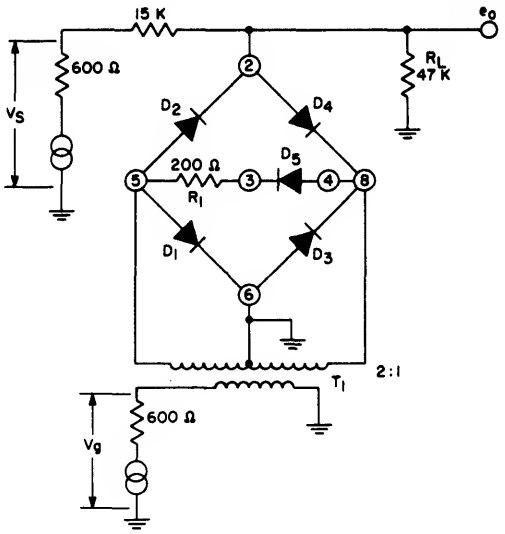


Fig.7—On-to-off ratio for the series gate of Fig.6 as a function of frequency.

Shunt Gate. Fig. 8 shows the use of the CA3019 as a shunt gate in which the diode bridge, in shunt with the load resistance, balances out the gating signal to provide a pedestal-free output. When the gating voltage V_g is of sufficient amplitude, the diode bridge (D_1 through D_4) conducts during one half of each gating cycle and does not conduct during the other half of the cycle. When the diode bridge is conducting, its low diode forward resistance shunts the load resistance R_L and prevents the input signal V_s from appearing at the output; when the diode bridge is not conducting, its high diode back resistance allows the input signal to appear at the output. Diode D_5 and resistor R_1 keep the transformer load nearly constant during both halves of the gating cycle. The substrate (terminal 7) can either be left floating or returned to a negative voltage, but it cannot be returned to ground. The characteristics of the shunt gate are as follows:

Gating frequency (f_g) — 1 to 100 kHz
Gating voltage (V_g) — 0.8 to 1.2 Vrms
Signal frequency (f_s) — dc to 500 kHz (2 dB down)
Signal voltage (V_s) — 0 to 1 Vrms

The frequency range of this circuit can be extended by application of a reverse bias to the substrate. The amount of gating voltage V_g present at the output as a function of the amplitude and frequency of V_g is shown in Table II.



T_1 — Technitrol No. 8511666 or equiv.

Fig.8 —Shunt gate using the CA3019.

TABLE II. GATING CHARACTERISTICS OF SHUNT GATE SHOWN IN FIG.8

Frequency of V_g kHz	*Amplitude of V_g volts*	*Present at the Amount of V_g Output mvs*
1	0.8	0.2
1	1.0	0.5
1	1.2	1.3
10	0.8	2.0
10	1.0	4.7
10	1.2	8.7
50	0.8	11.0
50	1.0	24.0
50	1.2	40.0

Series-Shunt Gate

A series-shunt gate which utilizes all six diodes of the CA3019 is shown in Fig. 9 This configuration combines the good on-to-off impedance ratio of the shunt gate with the low-output pedestal of the series gate.

On the gating half-cycle during which the voltage at A is positive with respect to the voltage at B, there is no output because the shunt diodes are forward-biased and

the series diodes are reverse-biased. Any signal passing through the input diodes (D_4 and D_2) encounters a low shunt impedance to ground (D_5 and D_6) and a high impedance in series with the signal path to the load (D_3 and D_1). This arrangement assures a good on-to-off impedance ratio. When the voltages at A and B reverse, the conduction states of the shunt and series diodes reverse, and the signal passes through the gate to the load resistor R_L. Any pedestal at the output is a function of the resistor, transformer, and diode balance.

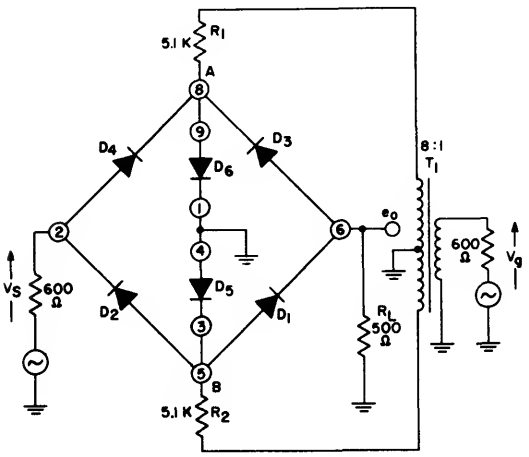


Fig.9 —Series-shunt gate using the CA3019.

The gate continues to operate successfully with resistors R_1 and R_2 shorted if the transformer center tap is removed from ground. In either case, no dc supply is required to bias the gate diodes.

Balanced Mixer

Fig. 10 illustrates the use of the CA3019 as a conventional balanced mixer. The load resistor across the output tuned circuit is selected to provide maximum power output. The conversion gain of the mixer for a 45-MHz input signal and a 55-MHz oscillator signal is shown in Fig. 11. The input impedance at point A is approximately 600-ohms for a 0.6-volt-rms oscillator drive.

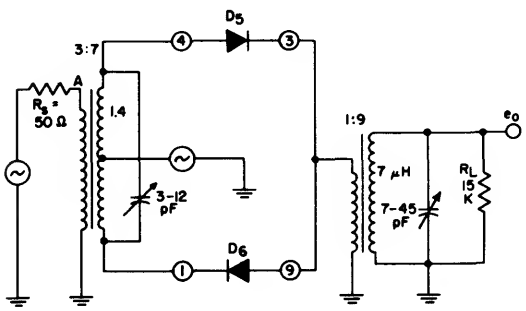


Fig.10 —Balanced mixer using the CA3019.

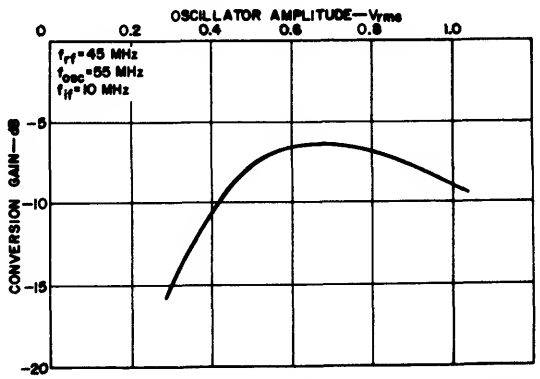


Fig.11 —Conversion gain as a function of oscillator amplitude for the balanced mixer of Fig.10.

The CA3019 mixer shown in Fig. 12 is essentially a balanced mixer with two additional diodes (D_3 and D_4) added to form a half-wave carrier switch. The additional diodes permit both legs of the circuit ($D_1 - D_2$ and $D_3 - D_4$) to function throughout the ac cycle. As compared with a conventional balanced mixer, shown in Fig.10, this circuit effectively doubles the desired output voltage

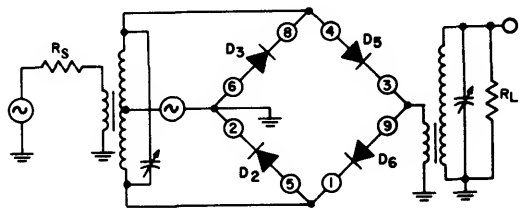


Fig.12—Balanced mixer with half-wave carrier switch using the CA3019.

and reduces the output voltage at the oscillator frequency by half. However, the capacitances associated with the integrated diodes prevent this circuit configuration from realizing the improvement in conversion gain at frequencies above 20 MHz.

Ring Modulator

The use of the CA3019 as a ring modulator is shown in Fig. 13. If a perfectly balanced arrangement were used, carrier current of equal magnitude and opposite direction would flow in each half of the center-tapped transformer T_2. Thus, the effect of the carrier current in transformer T_2 would be cancelled, and the carrier frequency would not appear in the output. However, the ring modulator of Fig. 13 is not exactly balanced because diodes ($D_1 + D_2$) and ($D_3 + D_4$) are actually two diodes in

parallel, while diodes (D_5) and (D_6) are individual diodes. Nevertheless, this circuit attenuates the carrier in the output as well as an arrangement that uses both individual diodes in two CA3019 circuits.

As the carrier passes through half of its cycle, diodes ($D_1 + D_2$) and (D_6) conduct, and diodes ($D_3 + D_4$) and (D5) do not conduct. When the carrier passes through the other half of its cycle, the previously nonconducting diodes conduct, and vice versa. As a result, the output amplitude, is alternately switched from plus to minus at the carrier frequency. The signal-frequency component of the output waveform is thus symmetrical about the zero axis and is not present in the output. Therefore, the ring modulator suppresses both the carrier frequency and the signal frequency so that the output theoretically contains only the upper and lower sidebands. For single-sideband transmission, one of these sidebands can be eliminated by selective filtering. The performance of the CA3019 as a ring modulator is shown in Table III.

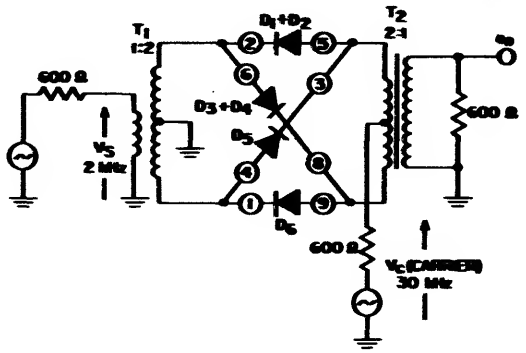


Fig.13 —Ring modulator using the CA3019.

TABLE III. PERFORMANCE CHARACTERISTICS OF RING MODULATION OF FIG.13

		For a given $V_s + V_c$, e_o in millivolts			
Output Freq. KHz	V_s rms	300	350	450	500
	V_c rms	600	500	350	300
28 or 32	Upper or Lower Sidebands	86	97	83	91
2	Sig. Freq.	0.042	0.02	0.015	0.020
30	Carrier Freq.	* 1.3 (−37db)	* 0.88 (−41db)	* 0.67 (−42db)	* 0.62 (−43db)
26 or 34	Higher Order Sidebands	0.018	0.016	0.036	0.043
24 or 36		0.021	0.054	0.047	5.0

* db below the desired upper and lower sidebands

ICAN-5337

Application Of The RCA-CA3028A and CA3028B Integrated-Circuit RF Amplifiers In The HF and VHF Ranges

by. H.M. Kleinman

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers. Each circuit also contains a constant-current transistor and suitable biasing resistors. The circuits are primarily intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in the following applications:

- RF Amplifier
- Autodyne Converter
- IF Amplifier
- Limiter

In addition to the applications listed above, the CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers. The CA3028B, which features tight control of operating current, input offset voltage, and input bias and offset current, is recommended for those applications in which balance and operating conditions are important.

Useful information concerning operation of the CA3028A and CA3028B in mixers, oscillators, balanced modulators, and similar circuits may be found in ICAN-5022, "Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers." Biasing considerations for the CA3028A and CA3028B differ from the types discussed in ICAN-5022; however, dynamic performance is quite similar to that of the CA3005 and CA3006. ICAN-5022 contains circuits that illustrate operation from dual supplies which, when available, can simplify the biasing of the CA3028A or CA3028B.

Both the CA3028A and CA3028B are supplied in an 8-terminal TO-5 package which assures minimum interlead capacitance and consequently excellent stability in high-frequency circuits. The spacing of the leads on the hermetically sealed package permits installation of the integrated circuits on printed circuit boards by wave-soldering techniques.

Circuit Description

The circuit diagram and terminal connections for the CA3028A and CA3028B are shown in Fig.1. The circuit is basically a single-stage differential amplifier composed of transistors Q_1 and Q_2 driven from a constant-current source Q_3. A single-ended input may be connected to terminal 1 or terminal 5, or push-pull inputs to terminals 1 and 5. Each of these terminals must be provided with a biasing network. Care must be taken to insure that the bias voltages on terminals 1 and 5 are nearly equal when balanced operation is desired. This can only be achieved in practice by using a single voltage divider as shown in Fig.2(a). Bias is first established on the base of one transistor, in this case Q_1, through terminal 1. The base of the second transistor, Q_2 in Fig.2(a), is then connected to the first through a low-valued dc impedance. In Fig.2(a), the inductive winding of the input transformer provides the

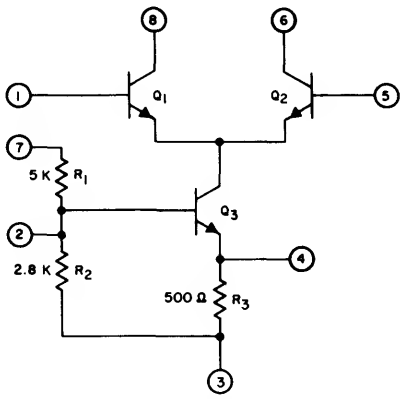


Fig.1 - Schematic diagram and terminal connections for the CA3028A and CA3028B integrated circuits.

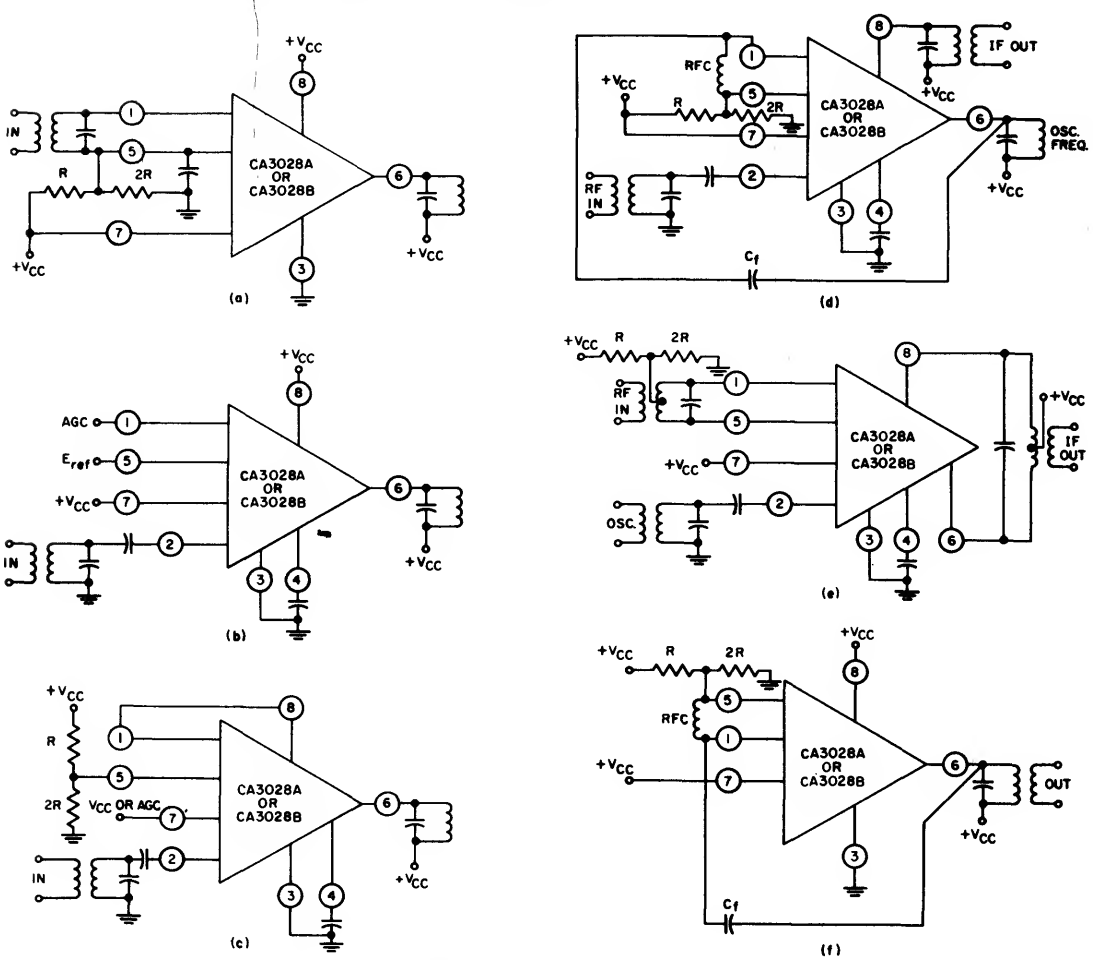


Fig.2 - Connections for the CA3028A and CA3028B for use as (a) a balanced differential amplifier with a controlled constant-current-source drive and agc capability; (b) a cascode amplifier with a constant-impedance agc capability; (c) a cascode amplifier with conventional agc capability; (d) a converter; (e) a mixer; (f) an oscillator.

low-resistance path. An rf choke or low-valued resistor may be used in place of transformer coupling, but caution must be exercised because even as little as 100 ohms may cause serious unbalance in some applications. A single-ended output may be taken from terminal 6 or terminal 8, or push-pull outputs from terminals 6 and 8. In systems with a single power supply of up to 12 volts, terminal 7 is connected to the highest positive potential for maximum gain. Other operating points can be selected by application of a varying bias voltage (agc) to Q_3.

The circuit diagrams in Fig.2 illustrate the flexibility of the CA3028A and CA3028B. Terminal connections are shown for a differential amplifier driven from a controlled constant-current source that has agc capability; a cascode amplifier with constant-impedance or conventional agc capability; a converter; a mixer; and an oscillator. The cascode mode of operation is recommended for applications that require higher gain. The differential mode is preferred when good limiting is required.

Operating Modes

The CA3028A and CA3028B integrated-circuit rf amplifiers can be operated in either the differential mode or the cascode mode. Applications using the differential mode are distinguished by high input impedance, good gain-control characteristics, large input-signal-handling capability, and good limiting.

For ease of design of systems using the CA3028A and CA3028B, admittance or "y" parameters are shown in Fig.3 for the differential mode and in Fig.4 for the cascode mode. It should be noted that the y parameters of the more complex differential and cascode amplifier stages differ from those of simple common-emitter transistor stages.

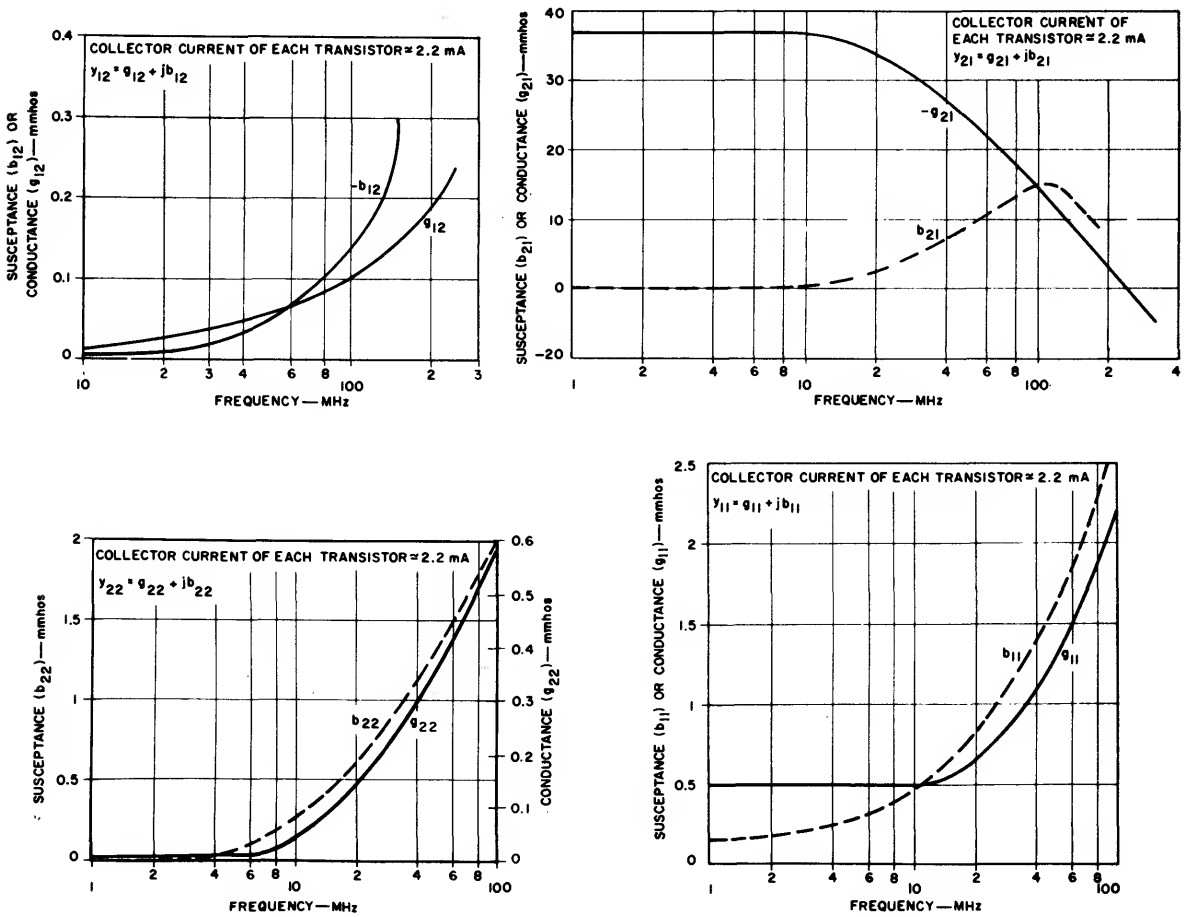
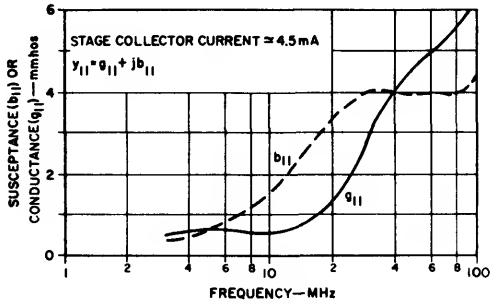
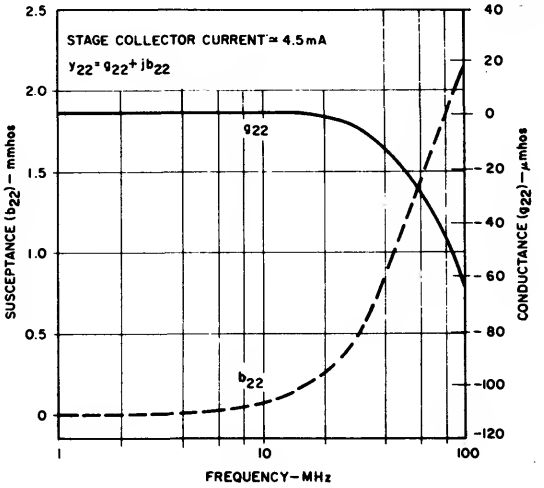
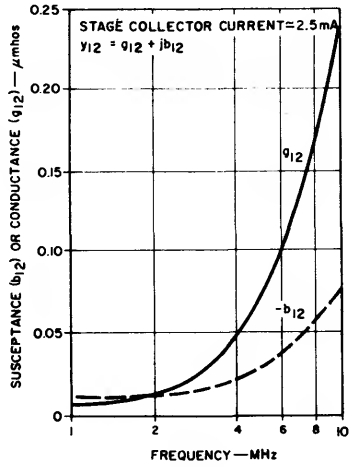
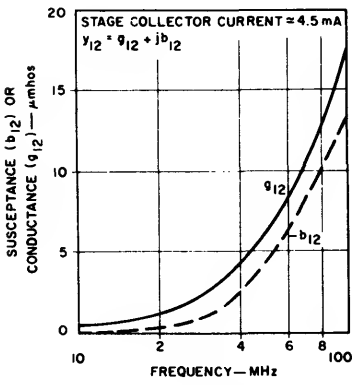


Fig.3 - Y parameters of the CA3028A and CA3028B in the differential-amplifier connection.









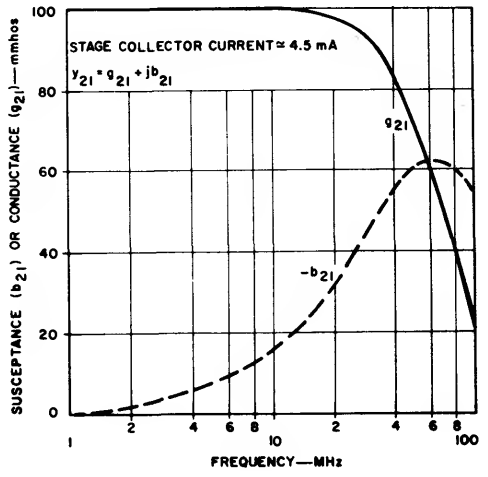


Fig.4 - Y parameters of the CA3028A and CA3028B in the cascode connection.

For quick reference, values for input and output parallel RC networks and transconductance values are listed in Table I for the differential amplifier and in Table II for the cascode amplifier.

Although the reverse transfer admittance y_{12} of the CA3028A or CA3028B is low for either cascode or differential operation, circuit-layout-induced instability can occur in high-gain amplifiers. Circuit layout is of paramount importance in both modes because undesirable coupling admittances can be much greater than the CA3028A or CA3028B admittances. Attention to layout and shielding is imperative if proper advantage is to be taken of the low feedback of the CA3028A and CA3028B.

Table I Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuits in the Differential Amplifier.

Frequency	Input Parallel RC Network		Output Parallel RC Network		Transconductance
(MHz)	R_{in} (ohms)	C_{in} (pF)	R_{out} (ohms)	C_{out} (pF)	g_m (millimhos)
10.7	1800	8	2.2×10^4	4	35
100	500	4.5	1.8×10^3	4	15

Table II Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuit Cascode Amplifier.

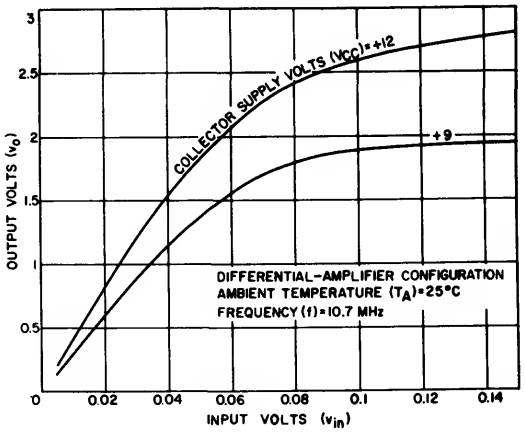
Frequency	Input Parallel RC Network		Output Parallel RC Network		Transconductance
(MHz)	R_{in} (ohms)	C_{in} (pF)	R_{out} (ohms)	C_{out} (pF)	g_m (millimhos)
10.7	900	22	-1.67×10^6	3.1	100
100	170	6.3	-5×10^5	3.5	14

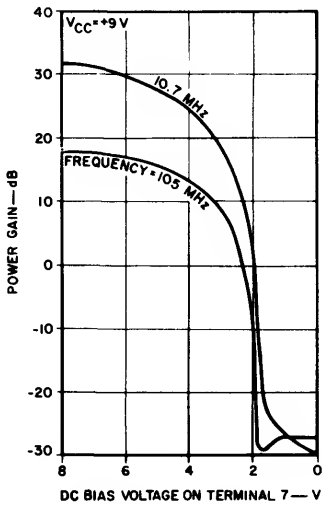
Differential Amplifier

The differential amplifier shown in Fig.2(a) is designed for operation at 10.7 MHz and 100 MHz. Because the amplifier consists essentially of a common-collector stage driving a common-base stage, the input admittance y_{11}, the output admittance y_{22}, and the forward transfer admittance y_{21} are decreased by a factor of two. The reverse transfer admittance y_{12} is typically 140 times lower than that of a single common-emitter transistor at 10.7 MHz, and 10 times lower at 100 MHz. As a result, the CA3028A and CA3028B can be aligned easily in if strips without need for neutralization.

The transfer characteristic in Fig.5(a) shows the excellent limiting capabilities of the CA3028A and CA3028B differential amplifiers. This limiting performance is achieved because the constant-current transistor Q_3 limits the circuit operating current so that the collectors of the differential-pair transistors Q_1 and Q_2 do not saturate. Table III shows the maximum permissible load resistances for non-saturating operation when single supply voltages of 9 and 12 volts are used.

When linear operation over a wide input-voltage range is imperative, agc voltage may be applied to the constant-current source Q_3 at terminal 7. Gain-control





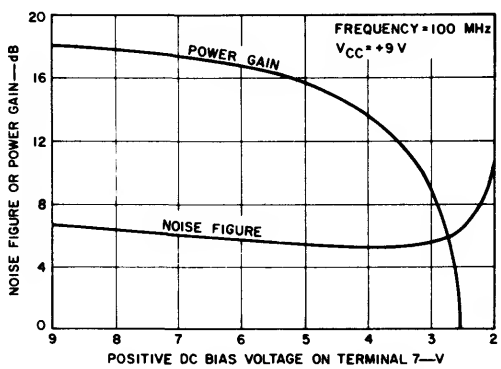


Fig.5 - Characteristics of the CA3028A and CA3028B in the differential-amplifier connection: (a) 10.7-MHz transfer characteristics; (b) agc capabilities; (c) power gain as a function of noise figure.

Table III Maximum Load Resistance Permissible for Non-Saturating Operation with +9 and +12 volt Single-Supply Voltages

V_{CC} (volts)	$I_{C1} + I_{C2}$ (milliamperes)	Maximum Tuned Load (ohms)	Maximum Resistive Load (ohms)
+9	5.0	3.6 K	1.8 K
+12	6.8	3.5 K	1.7 K

$R_L = V_{CC}/I_{C1} + I_{C2}$ Resistive Load

$R_L = 2\ V_{CC}/I_{C1} + I_{C2}$ Tuned Load

capabilities are -60 dB at 10.7 MHz and -46 dB at 100 MHz, as shown in Fig.5(b). Fig.5(c) shows curves of power gain and noise figure as a function of agc voltage. The combination of an optimum noise figure of 5.5 dB and a power gain of 15 dB at 100 MHz makes this circuit suitable for use as an rf amplifier in the commercial FM band.

Cascode Amplifier

When the CA3028A or CA3028B is used in the cascode configuration for rf-amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_{11} is essentially that of a common-emitter stage, and the forward transfer admittance y_{21} is that of a common-emitter stage times the common-base alpha. Because of the high-impedance drive source for the common-base stage, the output admittance y_{22} is quite low at low frequencies (0.6 μmho). The reverse transfer admittance y_{12} for the cascode circuit is 900 times less than that for a single-stage common-emitter at 10.7 MHz, and 35 times less at 100 MHz. As in the differential amplifier, ease in tuning is obtained without need for neutralization.

The transfer characteristic in Fig.6 shows the suitability of the cascode configuration for agc take-off for FM front-end controls.

Applications

The typical applications described below illustrate the use of the CA3028A and CA3028B integrated-circuit rf amplifiers in both the differential and the cascode modes.

10.7-MHz Cascode IF Amplifier. Fig.7 shows an FM if strip in which the CA3028A or CA3028B is used in a high-gain, high-performance cascode configuration in conjunction with a CA3012 integrated-circuit wide-band amplifier. The CA3012 is used in the last stage because of the high gain of 74 dB input to the 400-ohm-load ratio-detector transformer T_4. An input of approximately 400 microvolts is required at the base of the

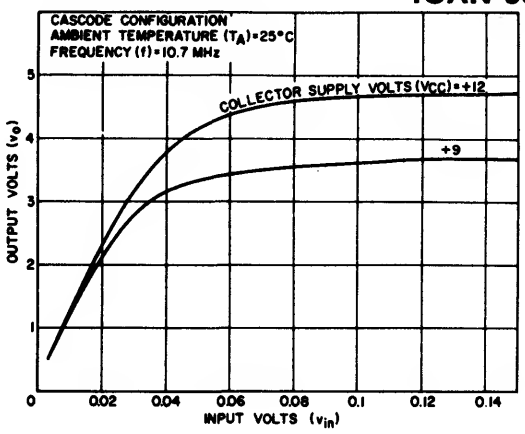


Fig.6 - 10.7-MHz transfer characteristics of the CA3028A and CA3028B in the cascode connection.

CA3012 for -3 dB below full limiting. An impedance-transfer device and filter must be connected between the CA3012 base (terminal 1) and the output of the CA3028A or CA3028B (terminal 6). The insertion loss of this filter should be kept near 6 dB (1:2 ratio of loaded to unloaded Q) so that all possible gain can be realized up to the CA3012 base. In addition to this insertion loss, a voltage step-down loss of 5.8 dB in the interstage filter is unavoidable. Therefore, the total voltage loss is approximately 9 to 14 dB, and an output of 1500 to 2000 microvolts must be available from the CA3028A or CA3028B to provide the required 400-microvolt input to the CA3012.

The voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{100 \times 10^{-3}}{0.33 \times 10^{-3}} = 300 = 49\ dB$$

This calculation indicated a sensitivity of 6.6 microvolts at the CA3028A or CA3028B base (terminal 2). This value cannot be realized, however, because the CA3012 limits on noise peaks so that the gain figure is reduced.

A sensitivity of 7.5 microvolts was realized in the design shown in Fig.7. The filter approach with high-gain integrated-circuit chips differs from that for single, cascaded transistor stages in that lumped selectivity is required rather than distributed selectivity.

Special care must be exercised when second-channel attenuation in the order of 45 dB is required. Selectivity is then proportioned as follows:

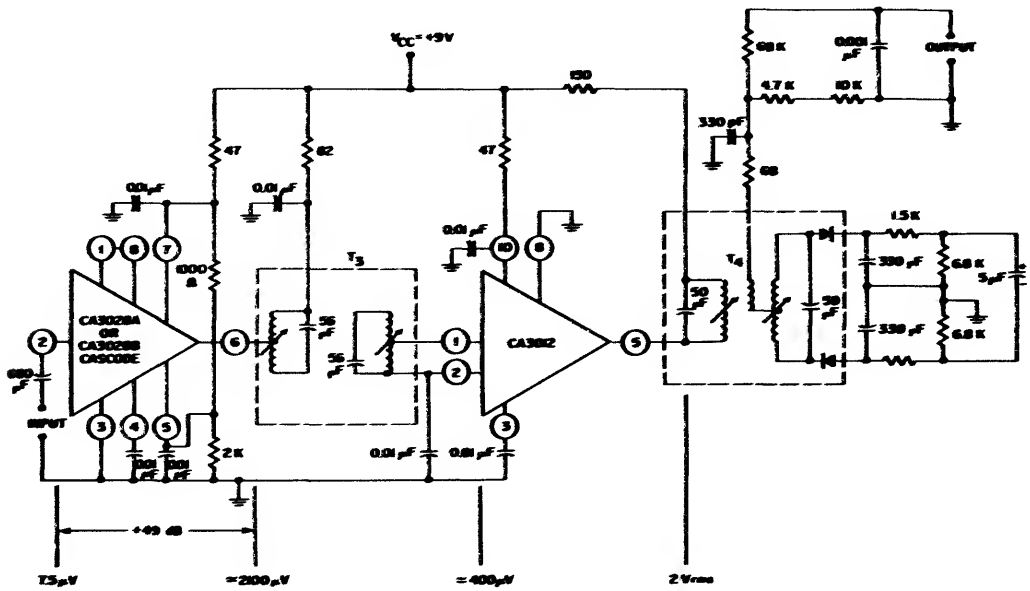
Interstage filter: double-tuned 220 kHz at -3 dB; coefficient of critical coupling, 0.7; voltage loss, 8 dB

Converter filter: triple-tuned, 220 kHz at -3 dB; coefficient of critical coupling, 0.8; voltage loss, about 28 dB

Because of input limiting in the CA3012, the interstage filter exhibits a somewhat wider bandwidth than the 220 kHz indicated. Therefore, a coefficient of critical coupling near 0.8 is realized, which is optimum for minimum deviation from constant time delay. The triple-tuned converter filter alone provides second-channel attenuation of 30 to 33 dB, while the interstage filter contributes 8 to 10 dB. The filters described meet requirements of both performance and economy.

10.7-MHz IF Strip Using Two CA3028A or CA3028B Circuits. The 10.7-MHz if strip shown in Fig.8 uses two CA3028A or CA3028B integrated circuits to provide less over-all gain than the circuit of Fig.7. The first integrated circuit is connected as a cascode amplifier and yields voltage gain of 50 dB; the second integrated circuit is connected as a differential amplifier and yields voltage gain of 42 dB.

When a practical interstage transformer having a voltage insertion loss of 9 dB is used, over-all gain is



T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

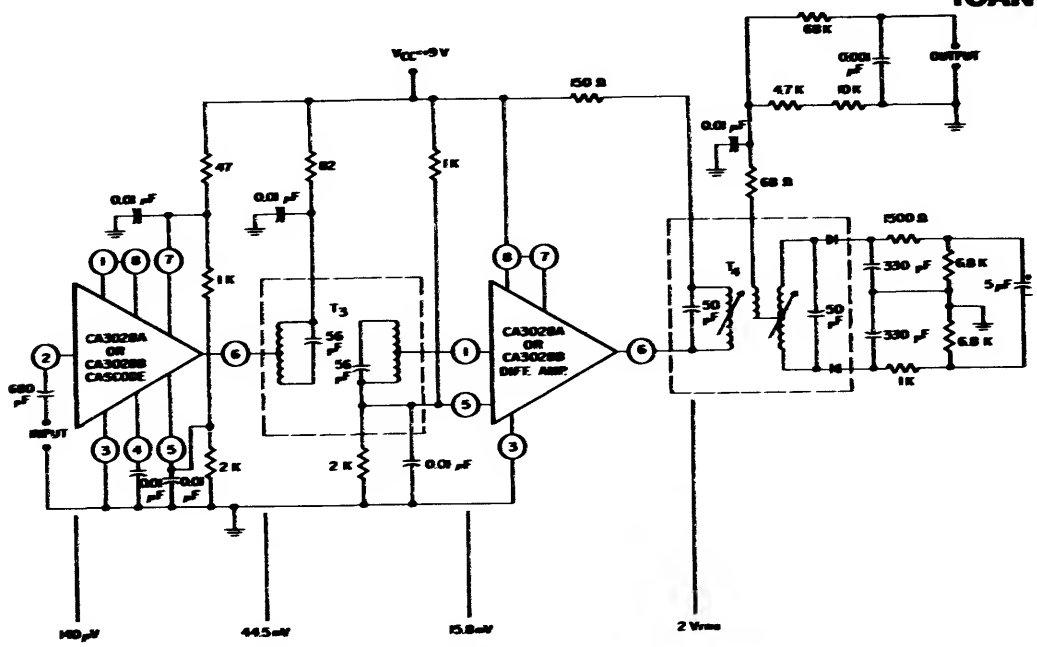
Audio Output: 155 mV rms for 7.5 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.7 - 10.7-MHz if amplifier using a CA3028A or CA3028B in the cascode mode.

The large collector swing that can be obtained in cascode operation of the CA3028A or CA3028B makes it desirable to take the agc voltage from the collector or "hot" end of the if transformer for front-end gain control. The cascode stage then operates primarily in its linear region, and excellent selectivity (40 dB) is maintained even for large signal inputs of approximately 0.4 volt. Front-end gain reduction is between 40 and 50 dB.

83 dB and the sensitivity at the base of the first integrated circuit is 140 microvolts. A less sophisticated converter filter (double-tuned) could be employed at the expense of about 26 dB of second-channel attenuation. If the voltage insertion loss of the converter filter is assumed to be 18 dB and the front-end voltage gain (antenna to mixer collector) is 50 dB, this receiver would have an IHFM* sensitivity of approximately 8 microvolts.

* Institute of High-Fidelity Manufacturers.



T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

Audio Output: 155 mV rms for 140 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.8 - 10.7-MHz if strip using two CA3028A or CA3028B integrated circuits.

10.7-MHz Differential-Amplifier IF Strip. Fig.9 shows a 10.7-MHz medium-gain if strip consisting of a CA3028A or CA3028B connected as a differential amplifier and a CA3012 wide-band amplifier. As in the circuit shown in Fig.7, an input of approximately 1500 microvolts is required to the interstage filter. The differential-mode voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

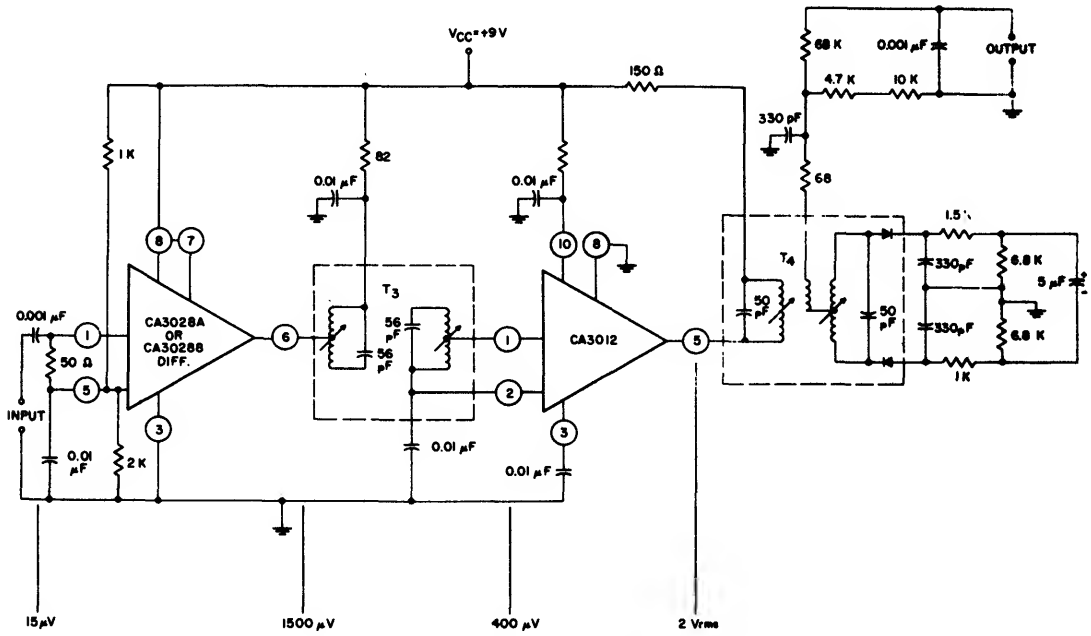
$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{35 \times 10^{-3}}{0.38 \times 10^{-3}} = 92.5 = 39.3 \text{ dB}$$

This voltage gain requires that an input of approximately 15 microvolts be available at the base of the CA3028A or CA3028B differential amplifier.

Even if a triple-tuned filter having a voltage insertion loss of 28 dB is used in a low-gain front end, a receiver having an IHFM sensitivity of 5 microvolts results. If 26 dB second-channel attenuation is permissible, a 3-microvolt-sensitivity IHFM receiver can be realized.

88-MHz-to-108-MHz FM Front End. Fig.10 illustrates the use of the CA3028A or CA3028B as an rf amplifier and a converter in an 88-to-108-MHz FM front end. For best noise performance, the differential mode is used and the base of the constant-current source Q_3 is biased for a power gain of 15 dB. The rf amplifier input circuit is adjusted for an insertion loss of 2 dB to keep the noise figure of the front end low. Because the insertion loss of the input transformer adds directly to the integrated-circuit noise figure of 5.5 dB, the noise figure for the front end alone is 7.5 dB, as compared to noise figures of about 6 dB for commercial FM tuners.

Although a single-tuned circuit is shown between the collector of the rf-amplifier stage and the base of the converter stage, a double-tuned circuit is preferred to reduce spurious response of the converter. If the double-tuned circuit is critically coupled for the same 3-dB bandwidth as the single-tuned circuit, the insertion loss remains the same.



T_3: Interstage transformer TRW #22486 or equiv.

T_4: Ratio detector TRW #22516 or equiv.

Audio output: 155 mV *rms for* 15 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig.9 - 10.7-MHz if strip using a CA3028A or CA3028B in the differential mode.

The collector of the rf stage is tapped down on the interstage coil at approximately 1500 ohms, and the base of the converter stage at 150 ohms. RF voltage gain is computed as follows:

Antenna to base	0 dB
Base to collector	22 dB
Voltage insertion loss of interstage coil	-13 dB
Net rf voltage gain	9 dB

If an if converter transformer having an impedance of 10,000 ohms is used, the calculated voltage conversion gain is

$$VG_c = \frac{-y_{21}}{y_{22} + y_L} = 112 = 41.3 \text{ dB}$$

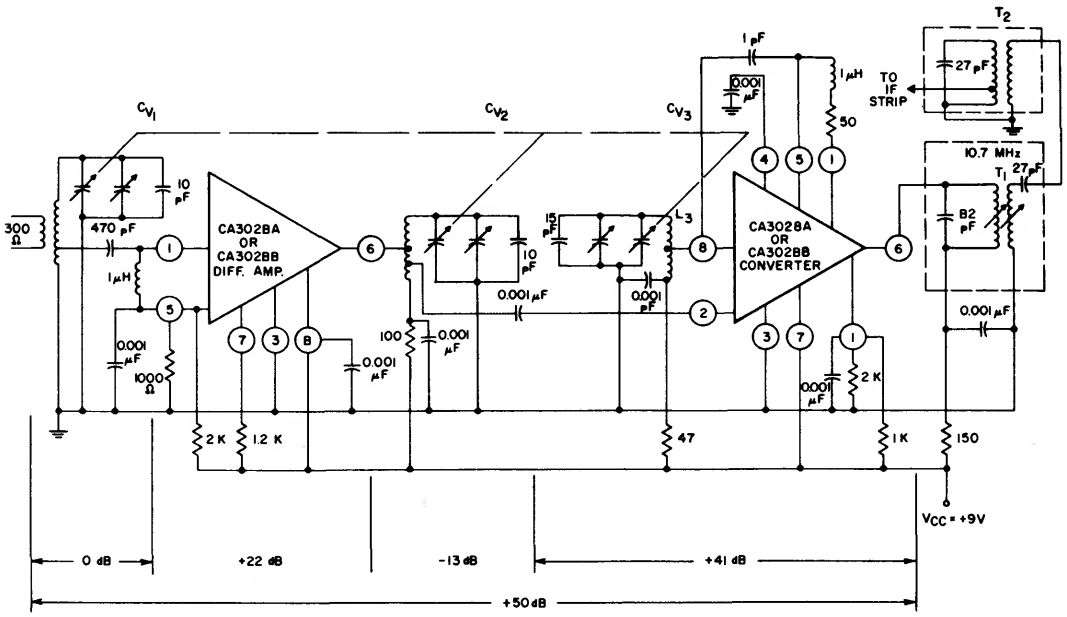
Measured gain into the collector of the converter is 42 dB. The measured voltage gain of the rf amplifier and converter into a 10,000-ohm load is 52 dB; calculated gain is 50 dB When the converter is tuned for the commercial FM band (88 to 108 MHz), the following parameters apply:

Input resistance R_{in}	170	ohms
Input capacitance C_{in}	6.3	pF
Output resistance R_{out}	80K	ohms
Output capacitance C_{out}	3.5	pF
Conversion transconductance	13	mmhos

The rf amplifier and converter shown in Fig.10 were combined with the if amplifier shown in Fig.7, and the following performance data were measured at 100 MHz:

30-dB (S + N)/N IHFM Sensitivity	3 μV
Image Rejection	46 dB

Receiver noise figure is the limiting factor that permits a sensitivity of only 3 microvolts to be realized.



L_1: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 1-3/4 T; primary — 2 turns #30 SE.

L_2: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 6 2-1/4 T, A 3/4 T.

$C_{V1\text{-}2}$: variable $\Delta C \approx 15$ pF

T_1: Mixer transformer TRW #22484 or equiv.

T_2: Input transformer TRW #22485 or equiv.

L_3: 3-1/2 T #18 tinned copper wire; winding length 5/16" on 9/32" form.

$C_{V1\text{-}3}$: variable, $\Delta C \approx 15$ pF.

Fig. 10 - 88-MHz-to-108-MHz FM front end.

ICAN-5380

Integrated-Circuit Frequency-Modulation IF Amplifiers

by H.C. Kiehn and R.L. Sanquini

Silicon monolithic integrated circuits that use a differential-amplifier configuration have certain design features which make them more attractive than discrete-component circuits for FM if-amplifier applications. These features include better performance, small size, light weight, and more potential circuit functions per dollar of cost.

The Differential Amplifier

The heart of integrated-circuit FM if amplifiers is the differential amplifier, which is probably the best simple configuration available today for symmetrical limiting over a wide input-voltage range. Each half of the differential amplifier is alternately cut off on positive and negative half-cycles of the input signal.

As shown in Fig.1, the total current through the circuit I_T is relatively constant. A current equal to $I_T/2$ flows through each transistor at balance (quiescent condition). When the base voltage V_{B1} is made

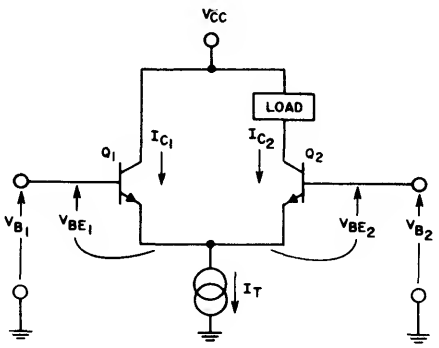


Fig.1 - Basic differential-amplifier configuration.

This material was presented at the IEEE Second Annual Semiconductor-Device Clinic on Linear Integrated Circuits in New York City, March 24, 1967.

more positive than V_{B2}, however, the collector current I_{C1} increases and I_{C2} decreases. The value of I_{C1} becomes equal to the total current I_T when the following condition exists:

$$V_{B1} - V_{B2} - V_{BE1} \geq V_{BE2} \text{ (threshold)}$$

The transistor Q_1 is then full on, and Q_2 is then cut off. Similarly, when V_{B1} is made more negative than V_{B2}, the value of I_{C2} becomes equal to I_T; Q_1 is then cut off and Q_2 is full on. When the worst-case value of I_T is known, the maximum load impedance for symmetrical limiting is selected so that collector saturation does not occur, as follows:

$$\text{Resistive Load: } R_L = V_{CC}/I_T$$

$$\text{Tuned Load: } R_L = 2\,V_{CC}/I_T$$

Under these conditions, symmetrical limiting is obtained without spurious phase modulation.

The transfer characteristics for a typical differential amplifier shown in Fig.2 illustrate the excellent

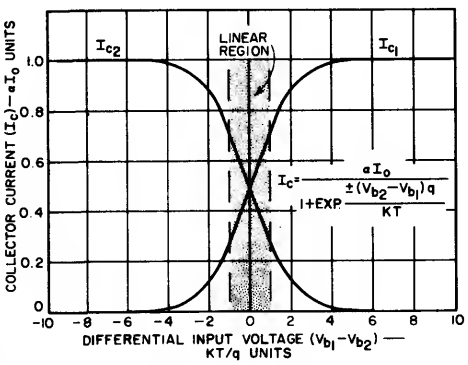


Fig.2 - Transfer characteristics of basic differential-amplifier circuit.

limiting characteristics. Further increases in input voltage ($V_{B1} - V_{B2}$) produce no change in collector current above 4KT/q units of input signal.

There are two basic approaches to the design of integrated-circuit FM if-amplifier stages using differential amplifiers: (1) lumped-filter FM if amplifiers using high-gain multi-stage integrated-circuit packages, or (2) individually tuned FM if amplifiers using single-stage integrated-circuit packages. This paper discusses the performance obtained with these approaches and outlines their merits and limitations.

Evolution of High-Gain Selective Building Blocks

The tuned rf amplifiers used in early broadcast receivers soon exhibited a point of diminishing returns with regard to gain and selectivity improvements. With the advent of the superheterodyne principle, the intermediate-frequency amplifier became the first building block that had fixed-frequency tuning, relatively high gain, and good selectivity as a result of its operation at a frequency lower than the signal frequency.

Because of its demands for high gain, phase linear amplification, and good symmetrical amplitude limiting, and because of the numerous FCC station allocations, FM broadcasting is now facing the dilemma of providing selectivity with good phase response. That is, receiver selectivity must be maintained for large signal inputs without deterioration of phase response. (A discussion of the practical solution of this problem is beyond the scope of this paper.) Successive limiting from the last stage back to the first stage can no longer be tolerated.

High-Gain-Per-Package Differential Integrated-Circuit IF Strips

Fig.3 shows the schematic diagram of a high-gain integrated circuit, the CA3012, which can be used in an if-amplifier strip to drive a ratio detector. The CA3012 wideband amplifier, designed for use in FM broadcast or communications receivers, is basically an if amplifier-limiter intended for use with external FM detectors. It consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of an emitter-coupled amplifier and an emitter-follower. The operating conditions are selected so that the dc voltage at the

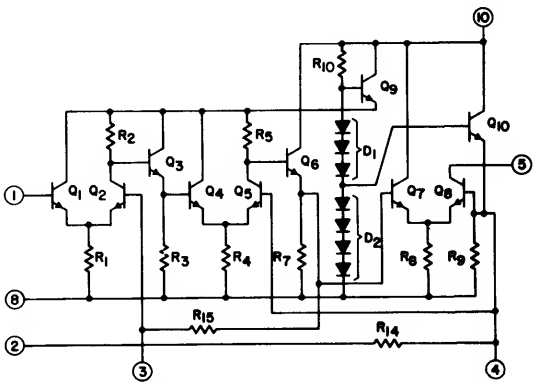


Fig.3 - Schematic diagram of CA3012 integrated-circuit wideband amplifier.

output of each stage is identical to that at the input of the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor. As a result,

the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to the base-to-emitter voltage V_{BE} plus the common base potential. The potential at the output of the emitter-follower, therefore, is the same as the common base potential.

At an operating point 3 dB down from the knee of the transfer curve, therefore, the CA3012 requires an input between 400 and 600 microvolts, depending on the ratio-detector design. Fig.4 shows the use of two CA3012 units in a 10.7-MHz if-amplifier strip. A double-tuned filter that has a voltage insertion loss of 8 dB is located between the two CA3012 units to provide a filter input of approximately 1000 microvolts (at terminal 5 of the first CA3012). For an if-strip sensitivity of 4 microvolts, a gain of 48 dB is required. However, if the CA3012 used has a load impedance of 1200 ohms, the available gain is 65 dB, or approximately 17 dB more than required. The extra gain is not wasted, but drives the second CA3012 harder, causing it to limit so that its gain is reduced by approximately 17 dB.

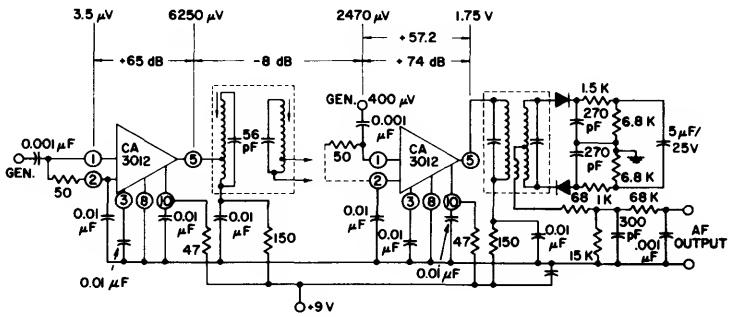


Fig.4 - 10.7-MHz if-amplifier strip using CA3012 integrated circuit.

Fig.5 shows the selectivity of the double-tuned interstage filter. The 3-dB bandwidth is 200 kHz at an input of 10 microvolts and 240 kHz at inputs from 500 microvolts to 0.5 volt. The coefficient of critical coupling is approximately 0.5 at 10 microvolts and increases to 1.0 but still maintains good phase response. The double-tuned filter should be coupled capacitance-aiding to avoid a nearly in-phase over-all relationship. Otherwise, bypassing of terminal 10 and the ratio-detector primary becomes critical and over-all stability is impaired.

The connection of the FM front end to the integrated-circuit if strip must provide good selectivity and good phase response. A double-tuned filter is not suitable from the standpoint of selectivity. An actual IHFM* receiver selectivity between 35 and 40 dB is practical and does not impose too much burden on alignment. Because IHFM selectivity includes other factors than passband, a combined filter design that provides second-channel attenuation between 52 and 60 dB becomes imperative.

Investigation of various types of inductance-capacitance filters indicates the use of a triple-tuned type to form the major lumped selectivity of the FM receiver. Fig.6 shows the response curve and two configurations for such a filter. Economy and ease of alignment are the major features in this approach.

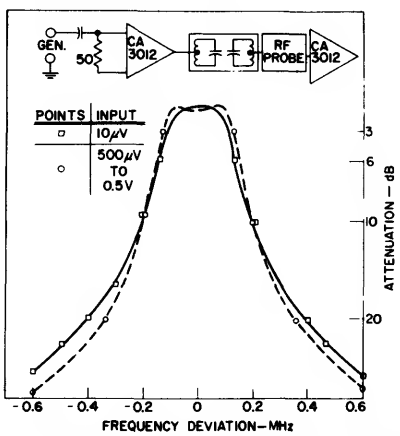


Fig.5 - Selectivity curve for double-tuned interstage filter.

The triple-tuned filter, which is located between the mixer and the first integrated circuit, may have a voltage insertion loss of 33 dB, depending on the desired gain distribution. The power insertion loss of the filter, which is between 12 and 17 dB, is the loss that contributes to if noise. If the primary impedance is reduced to provide a lower voltage insertion loss, the front-end gain is decreased by a corresponding amount. Stability criteria must be the deciding factor in impedance and gain distribution.

* Institute of High-Fidelity Manufacturers.

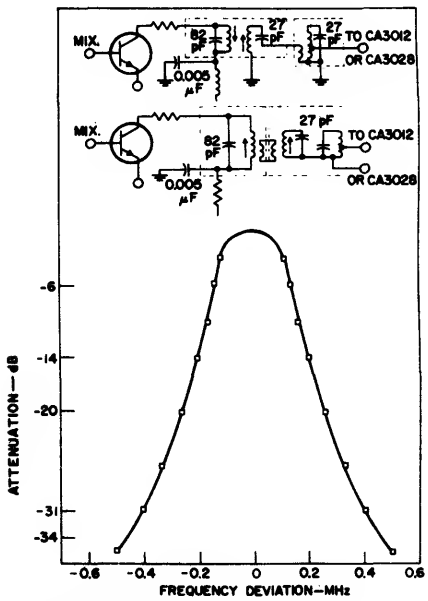


Fig.6 - Configurations and response curve for triple-tuned interstage filter.

Most FM front ends come equipped with a double-tuned 10.7-MHz if transformer in which a secondary high-impedance winding is brought out capacitively unterminated and non-polarized with respect to ground. This configuration does not lend itself readily to optimum skirt selectivity (form factor) when connected with an additional single-tuned transformer to form a triple-tuned filter. Most effective use of the existing front-end filter is accomplished by the addition of another double-tuned filter, such as those shown in Fig.7. Either

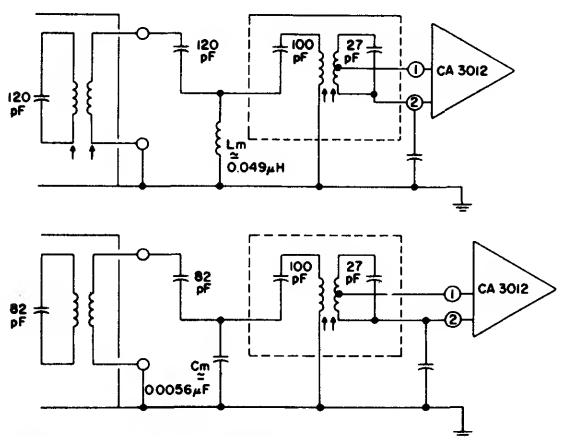


Fig.7 - Configurations of two quadruple-tuned interstage filters.

bottom inductance or capacitance coupling can be used. Voltage insertion losses from 18 dB to 26 dB can be expected. Fig.8 shows the response curve obtained

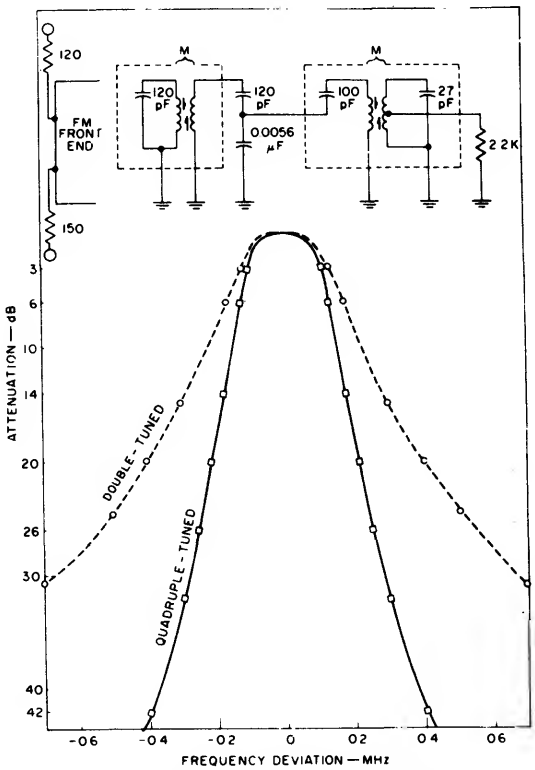


Fig.8 - Response curve obtained with quadruple-tuned filter.

with a quadruple-tuned interstage filter. The per-cent coupling between filters and the coupling mode must be determined on the basis of over-all stability and performance.

It may be appropriate to consider briefly the noise associated with high-insertion-loss filters. Over-all receiver noise F is calculated as follows:

$$F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2}$$

where F_1, F_2, and F_3 are the noise figures of the first (rf), second (mixer), and third (if) stages, respectively; and G_1 and G_2 are the power gains of the first and second stages. If a value of 27 dB is assumed for the if noise figure F_3 (filter plus integrated circuit), 10 dB for the mixer noise figure, and 30 dB for mixer power gain, the effect of if noise on mixer noise is determined as follows:

$$F_2' = F_2 + \frac{F_3-1}{G_2} = 10 + \frac{27-1}{30} = 10.87 \text{ dB}$$

If the rf stage is assumed to have a power gain of 15 dB and a noise figure of 5 dB, total receiver noise is then determined as follows:

$$F = F_1 + \frac{F_2 - 1}{G_1} = 5 + \frac{10.87 - 1}{15} = 5.66 \text{ dB}$$

These calculations show that the power gain of the rf-amplifier stage overrides both if noise and mixer noise. A minimum power gain of 10 dB is advisable.

The use of a tuning capacitance of 82 picofarads in the collector circuit of the mixer stage provides a loaded primary impedance of approximately 10,000 ohms and eliminates the need for a tap. The 27-picofarad tuning capacitances that comprise the other poles of this filter could be reduced to obtain more favorable loaded-to-unloaded-Q ratios without use of additional resistor loading. The choice of 27 picofarads was based primarily on circuit stability considerations.

Fig.9 shows one type of complete integrated-circuit if strip, and Fig.10 shows the accompanying voltage gains and impedances. Values are given for two levels of mixer output impedance. All other impedance levels shown have exhibited good stability. Over-all performance of the circuit is illustrated in Fig.11.

Capture ratio, which was measured at various levels, varies from 5 dB at 2 microvolts to 1.2 dB above 500 microvolts. With careful adjustment, values as low as 0.8 dB can be obtained. The selectivity curve for the integrated circuit if strip is shown in Fig.12. Over-all selectivity for a given ratio detector and the if strip is shown in Fig.13. Some distributed-selectivity receivers have very little second-channel selectivity at an antenna input of 2000 microvolts. The points marked in Fig.13 show such selectivity for several antenna input levels.

Fig.14 shows an if strip that combines high gain per package and the single-stage-per-package approach. CA3012 and CA3028 integrated circuits are used in a differential-mode connection. An if sensitivity of 15 microvolts can be obtained with this if strip.

If discrete circuits are directly replaced by single differential integrated-circuit amplifiers, a minimum of if transformer and printed-circuit-board redesign is required. Values of voltage gain and impedance are indicated on the block diagram in Fig.15. All three double-tuned transformers are made symmetrical with respect to primary and secondary windings and taps.

Because the single- or double-tuned circuit used between the mixer and the if strip has inherently less

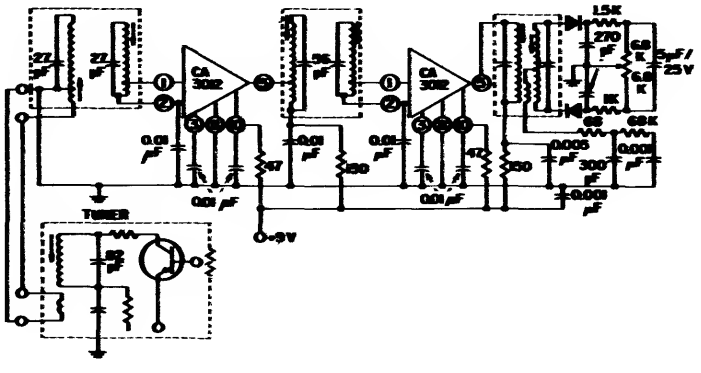


Fig.9 - Complete 10.7-MHz if-amplifier strip using two CA3012 integrated circuits.

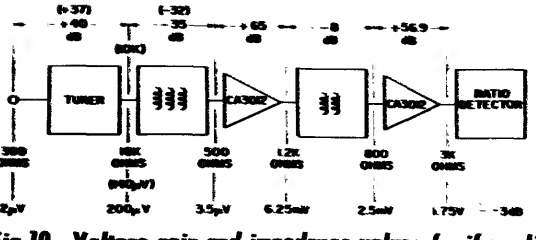


Fig.10 - Voltage gain and impedance values for if-amplifier strip of Fig.7.

insertion loss than a triple-tuned input filter, the input required is 20 instead of 3.5 microvolts. All three double-tuned if transformers have an insertion loss of 6 dB and a 3-dB bandwidth of 280 to 300 kHz. The ratio-detector primary impedance dictates the stage gain of 36 dB for the last integrated circuit. Each of the remaining three stages has a gain of 21.5 dB, for the total required gain of 100 dB. The impedance required for the desired stage gain was calculated to be 660 ohms for both the primary and secondary windings of the if transformers.

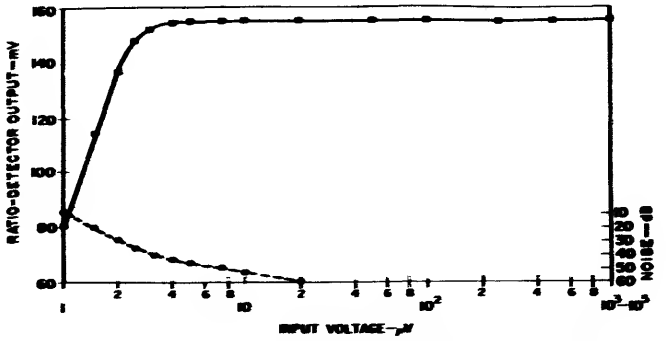


Fig.11 - Performance curves for if-amplifier strip of Fig.7.

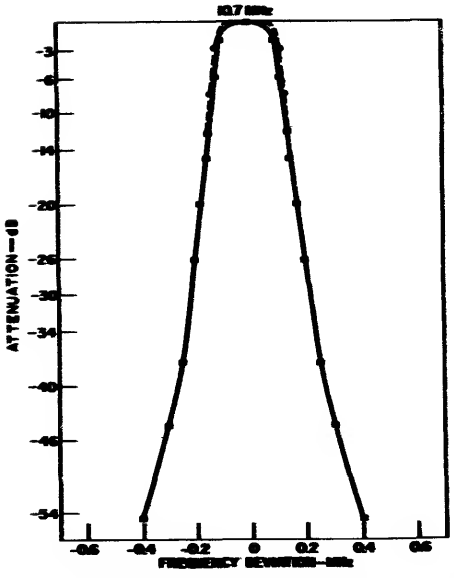


Fig.12 - Selectivity curve for if-amplifier strip of Fig.7.

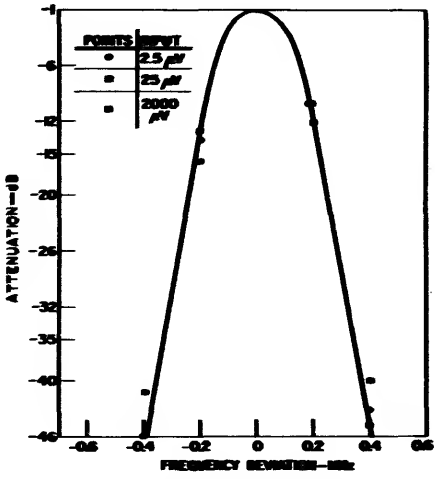


Fig.13 - Measured over-all selectivity curve for if-amplifier strip of Fig.7 and a given ratio detector.

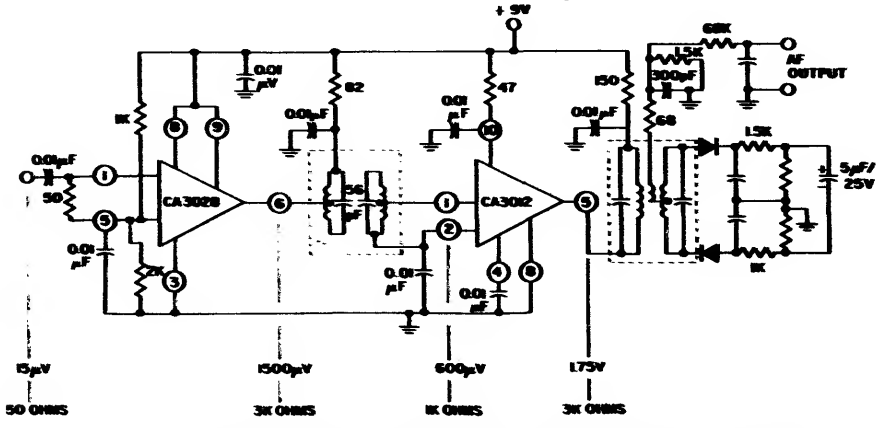


Fig.14 - IF-amplifier strip using CA3028 and CA3012 integrated circuits.

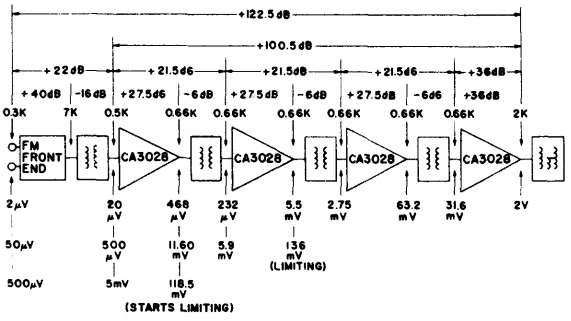


Fig.15 - Voltage gain and impedance values for if-amplifier strip of Fig.12.

With inputs from 20 to 200 microvolts, second-channel selectivity as high as 52 to 59 dB can be attained for three double-tuned and four double-tuned filters, respectively, for a 3-dB bandwidth of 196 kHz. For higher inputs, the same deterioration of selectivity occurs as that experienced with discrete circuits, as shown in Fig.16.

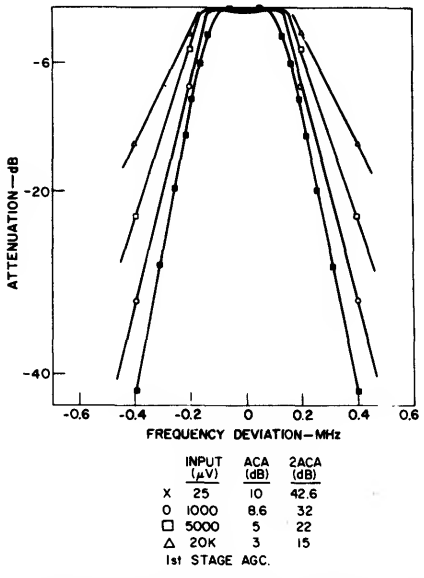


Fig.16 - Selectivity curves for discrete-component if strip using six double-tuned filters.

Several receivers incorporating the if strips shown have been field-tested in areas of 200-kHz station separation, where a weak station was sandwiched between two strong stations. The weak station was received without interference, as compared to the performance of other high-quality FM receivers fabricated with discrete-component if circuits, where lack of selectivity marred reception.

Conclusions

The preceding discussion has shown that the simplest approach to the use of integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

This approach, however, is not the best for cost performance in the long run. The single stage of gain is most difficult to justify economically when a single transistor stage is replaced with a single integrated-circuit package. The boundary condition for such an approach is that ultimately the cost of fabricating a package containing three transistors and three resistors (a typical complement for a differential-amplifier stage) must be the same as that of the one transistor the stage replaces.

Approaches to FM if stages which use the high-gain-per-package concept achieve the excellent AM rejection of differential amplifiers, as well as superior adjacent-channel attenuation, because more gain is inserted between the selectivity elements. From a performance point of view, this approach is superior to both discrete-stage and individually tuned integrated-circuit if strips.

From the point of view of cost, this approach has better possibilities because two packages are equivalent to four single stages of gain (four integrated-circuit packages). This approach results in maximum utilization of present-day monolithic integrated-circuit technology, and is closer to the optimum FM if amplifier shown in Fig.17.

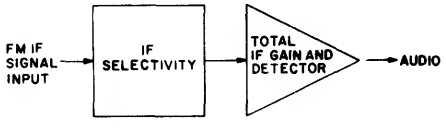


Fig.17 - Optimum FM if-amplifier configuration.

Application Of The RCA CA3020 and CA3020A Integrated-Circuit Multi-Purpose Wide-Band Power Amplifiers

by W.M. Austin and H.M. Kleinman

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has a lower voltage rating and must not be used in applications which require voltages on the output transistors greater than 18 volts. The integrated circuit protects the output transistor by limiting the drive to the output stages. The drive-limited current capability of the CA3020 is less than that of the CA3020A, but peak currents in excess of 150 milliamperes are an assured characteristic of the CA3020.

The RCA CA3020 and CA3020A integrated circuits are multi-purpose, multi-function power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz.

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has more limited voltage- and current-handling capability and must not be used in applications which require voltage swings on the output transistors greater than 18 volts or peak currents in excess of 150 milliamperes.

The CA3020 and CA3020A are designed to operate from a single supply voltage which may be as low as +3 volts. The maximum supply voltage is dictated by the type of circuit operation. For transformer-loaded class B amplifier service, the maximum supply voltages are +9 and +12 volts for the CA3020 and the CA3020A, respectively. When operated as a class B amplifier, either circuit can deliver a typical output of 150 milliwatts from a +3-volt supply or 400 milliwatts from a +6-volt supply. At +9 volts, the idling dissipation can be as low as 190 milliwatts, and either circuit can deliver an output of 550 milliwatts. An output of slightly more than 1 watt is available from the CA3020A when a +12-volt supply is used.

CIRCUIT DESCRIPTION AND OPERATION

Fig. 1 shows the schematic diagram of the CA3020 and CA3020A, and indicates the five functional blocks into

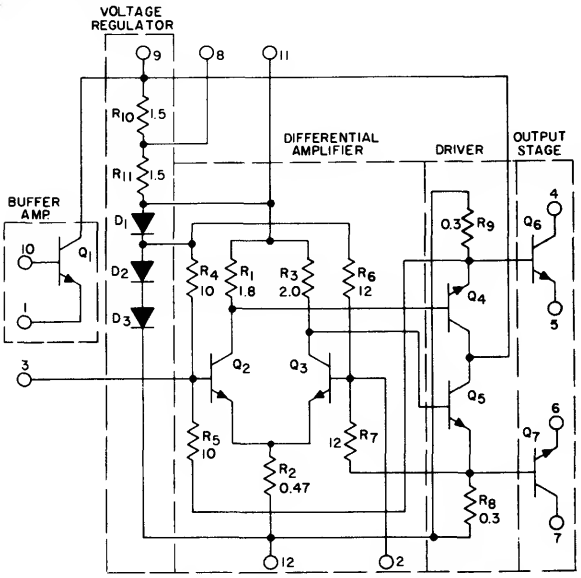


Fig. 1—Schematic diagram of CA3020 and CA3020A integrated-circuit amplifiers.

which the circuit can be divided for understanding of its operation. Fig. 2 shows the relationship of these blocks in block-diagram form.

A key to the operation of the circuit is the voltage regulator consisting of diodes D_1, D_2, and D_3 and resistors R_{10} and R_{11}. The three diodes are designed to provide accurately controlled voltages to the differential amplifier so that the proper idling current for class B operation is established in the output stage. The characteristics of these monolithic diodes closely match those of the driver and output stages so that proper bias voltages are applied over the entire military temperature range of −55 to +125°C. The close thermal coupling of the circuit assures against thermal runaway within the prescribed temperature and dissipation ratings of the devices.

The differential amplifier operates in a class A mode to supply the power gain and phase inversion required for the push-pull class B driver and output stages. In normal operation, an ac signal is capacitively coupled to terminal

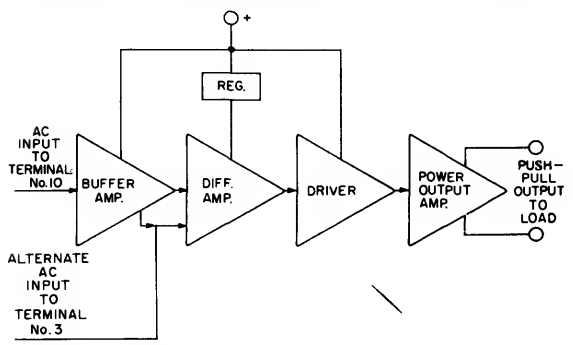


Fig. 2—Functional block diagram of the CA3020 and CA3020A.

3, and terminal 2 is grounded through a suitable capacitor. When the signal becomes positive, transistor Q_2 is turned on and its collector voltage changes in a negative direction. The same current flows out of the emitter of Q_2 and tends to flow to ground through resistor R_2. However, the impedance of R_2 is high compared to the input impedance of the emitter of Q_3, and an alternate path is available to ground through the emitter-to-base junction of transistor Q_3 and then through the bypass capacitor from terminal 2 to ground. Because this path has a much lower impedance than R_2, most of the current takes this alternate route. The signal current flowing into the emitter of Q_3 reduces the magnitude of that current and, because the collector current is nearly equal to the emitter current, the collector current in Q_3 drops and the collector voltage rises. Thus, a positive signal on terminal 3 causes a negative ac voltage on the collector of transistor Q_2 and a positive ac voltage on transistor Q_3, and provides the out-of-phase signals required to drive the succeeding stages. It should be noted that the differential amplifier is not balanced; resistor R_3 is ten per cent greater than R_1. This unbalance is deliberately introduced to compensate for the fact that all of the current in the emitter of Q_2 does not flow into Q_3. Use of a larger load resistor for transistor Q_3 compensates for the lower current so that the voltage swings on the two collectors have nearly the same magnitude.

The driver stages (transistors Q_4 and Q_5) are emitter-follower amplifiers which shift the voltage level between the collectors of the differential-amplifier transistors and the bases of the output transistors and provide the drive current required by the output transistors.

The power transistors (Q_6 and Q_7) are large, high-current devices capable of delivering peak currents greater than 0.25 ampere. The emitters are made available to facilitate various modes of operation or to permit the inclusion of emitter resistors for more complete stabilization of the idling current of the amplifier. Inclusion of such resistors also reduces distortion by introducing negative feedback, but reduces the power-output capability by limiting the available drive.

Inclusion of emitter resistors between terminals 5 and 6 and ground also enhances the effectiveness of the internal dc feedback supplied to the bases of transistors Q_2 and Q_3 through resistors R_5 and R_7. Any increase in the idling current in either output transistor is reflected as an increased voltage at its base. This change is coupled to the input through the appropriate resistor to correct for the increased current.

A later section of this Note describes how stable class A operation of the output stages may be obtained.

OPERATING CHARACTERISTICS

Supply Voltages and Derating. The CA3020 operates with any supply voltage between +3 and +9 volts. The CA3020A can also be operated with supply voltages up to +12 volts with inductive loads or +25 volts with resistive loads. Fig. 3 shows the permissible dissipation rating of the CA3020 and CA3020A as a function of case

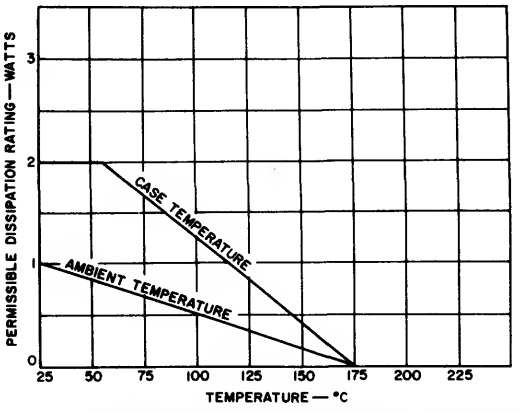


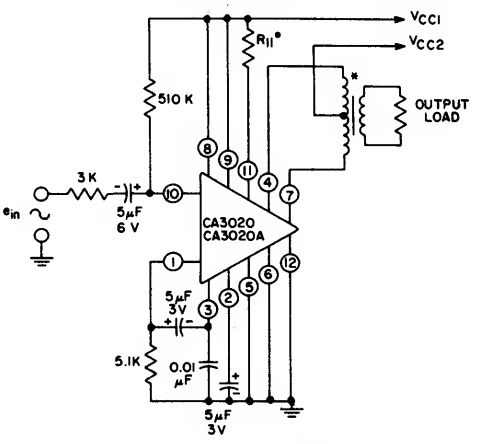
Fig. 3—Dissipation rating of the CA3020 and CA3020A as a function of case and ambient temperatures.

and ambient temperatures. At supply voltages from +6 to +12 volts, a heat sink may be required for maximum power-output capability. The worst-case dissipation $P_{d_{max}}$ as a function of power output can be calculated as follows:

$$P_{d_{max}} = (V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}) + (V_{CC_2}{}^2/(R_{CC})$$

where V_{CC_1} and V_{CC_2} are the supply voltages to the differential-amplifier and output-amplifier stages, respectively; I_{CC_1} and I_{CC_2} are the corresponding idling currents; and R_{CC} is the collector-to-collector load resistance of the output transformer. This equation is preferred to the conventional formula for the dissipation of a class B output transistor (i.e., 0.84 times the maximum power output) because the $P_{d_{max}}$ equation accounts for the device standby power and device variability.

Basic Class B Amplifier. Fig. 4 shows a typical audio-amplifier circuit in which the CA3020 or CA3020A can provide a power output of 0.5 or 1 watt, respectively. Table I shows performance data for both types in this amplifier. The circuit can be used at all voltage and power-output levels applicable to the CA3020 and CA3020A.



* Better Coil and Transformer DF108A, Thordarson TR-192, or equivalent.
• see text and tables.

Fig. 4—Basic class B audio amplifier circuit using the CA3020 or CA3020A.

The emitter-follower stage at the input of the amplifier in Fig. 4 is used as a buffer amplifier to provide a high input impedance. Although many variations of biasing may

Table 1 — Typical Performance of CA3020 and CA3020A in Circuit of Fig. 4*

Characteristic	CA3020	CA3020A	
Power Supply — V_{CC_1}	9	9	V
V_{CC_2}	9	12	V
Zero-Signal Idling Current — I_{CC_1}	15	15	mA
I_{CC_2}	24	24	mA
Maximum-Signal Current — I_{CC_1}	16	16.6	mA
I_{CC_2}	125	140	mA
Maximum Power Output at 10% THD	550	1000	mW
Sensitivity	35	45	mV
Power Gain	75	75	dB
Input Resistance	55	55	kΩ
Efficiency	45	55	%
Signal-to-Noise Ratio	70	66	dB
% Total Harmonic Distortion at 150 mW	3.1	3.3	%
Test Signal	1000 Hz/600Ω generator		
Equivalent Collector-to-Collector Load	130	200	Ω
Idling-Current Adjust Resistor (R_{11})	1000	1000	Ω

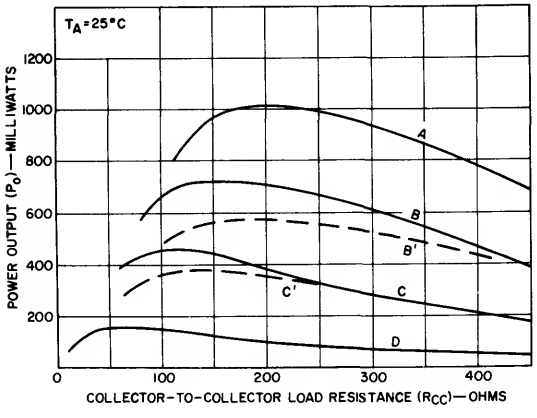
* Integrated circuit mounted on a heat sink, Wakefield 209 Alum. or equiv.

be applied to this stage, the method shown is efficient and economical. The output of the buffer stage is applied to terminal 3 of the differential amplifier for proper balance of the push-pull drive to the output stages. Terminals 2 and 3 must be bypassed for approximately 1000 ohms at the desired low-frequency roll-off point.

At low power levels, the cross-over distortion of the class B amplifier can be high if the idling current is low. For low cross-over distortion, the idling current should be approximately 12 to 24 milliamperes, depending on the efficiency, idling dissipation, and distortion requirements of the particular application. The idling current may be increased by connection of a jumper between terminals 8 and 9. If higher levels of operating idling current are desired, a resistor (R_{11}) may be used to increase the regulated voltage at terminal 11 by a slight amount with additional current injection from the power supply V_{CC_1}.

In some applications, it may be desirable to use the input transistor Q_1 of the CA3020 or CA3020A for other purposes than the basic buffer amplifier shown in Fig. 4. In such cases, the input ac signal can be applied directly to terminal 3.

The extended frequency range of the CA3020 and CA3020A requires that a high-frequency ac bypass capacitor be used at the input terminal 3. Otherwise, oscillation could occur at the stray resonant frequencies of the external components, particularly those of the transformers. Lead inductance may be sufficient to cause oscillation if long power-supply leads are not properly ac bypassed at the CA3020 or CA3020A common ground point. Even the bypassing shown may be insufficient unless good high-frequency construction practices are followed.

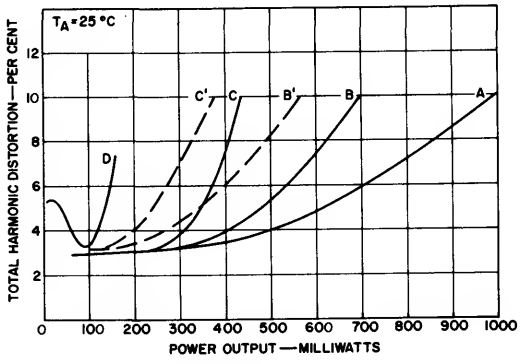


CURVE CA3020	CURVE CA3020A	IDLING CURRENT (mA) I_{CC1}	IDLING CURRENT (mA) I_{CC2}	POWER-SUPPLY VOLTAGE (V) V_{CC1}	POWER-SUPPLY VOLTAGE (V) V_{CC2}	R_{11} (OHMS)
-	A	9	10	9	12	00
B'	B	9	10	9	9	00
C'	C	7	6	6	6	00
-	D	8	8	3	3	220

Fig. 5—Power output of the CA3020 and CA3020A as a function of collector-to-collector load resistance R_{CC}.

Fig. 5 shows typical power output of the CA3020A at supply voltages of +3, +6, +9, and +12 volts, and of the CA3020 at +6 and +9 volts, as measured in the basic class B amplifier circuit of Fig. 4. The CA3020A has higher power output for all voltage-supply conditions because of its higher peak-output-current capability.

Fig. 6 shows total harmonic distortion (THD) as a function of power output for each of the voltage conditions shown in Fig. 5. The values of the collector-to-collector load resistance (R_{CC}) and the idling-current adjust resistor (R_{11}) shown in the figure are given merely as a fixed reference; they are not necessarily optimum values. Higher idling-current drain may be desired for low cross-over distortion, or a higher value of R_{CC} may be used for better sensitivity with less power-output capability. Because the maximum power output occurs at the same conditions of peak-current limitations, the sensitivities at maximum power output for the curves of Figs. 5 and 6 are approximately the same. Increasing the idling-current drain by reducing the value of the resistor R_{11} also improves the sensitivity.



CURVE CA3020	CURVE CA3020A	IDLING CURRENT (mA)		POWER-SUPPLY VOLTAGE (V)		R_{CC} (OHMS)	R_{11} (OHMS)
-	A	15	24	9	12	200	1000
B'	B	15	24	9	9	150	1000
C	C	12	14	6	6	100	1000
-	D	9	9	3	3	50	220

Fig. 6—Total harmonic distortion of the CA3020 or CA3020A as a function of power output.

Fig. 7 illustrates the improvement in cross-over distortion at low power levels. Distortion at 100 milliwatts is shown as a function of idling current I_{CC_2} (output stages only). There is a small improvement in total harmonic distortion for a large increase in idling current as the current level exceeds 15 milliamperes.

APPLICATIONS

Audio Amplifiers. The circuit shown in Fig. 4 may be used as a highly efficient class B audio power-output circuit in such applications as communications systems, AM or FM radios, tape recorders, phonographs, intercom sets, and linear mixers. Fig. 8 shows a modification of this

circuit which may be used as a transformerless audio amplifier in any of these applications or in other portable instruments. The features of this circuit are a power-output capability of 310 milliwatts for an input of 45 millivolts, and a high input impedance of 50,000 ohms. The idling-current drain of the circuit is 24 milliamperes. The curves of Fig. 5 may be used to determine the value of the center-tapped resistive load required for a specified power-output level (the indicated load resistance is divided by two).

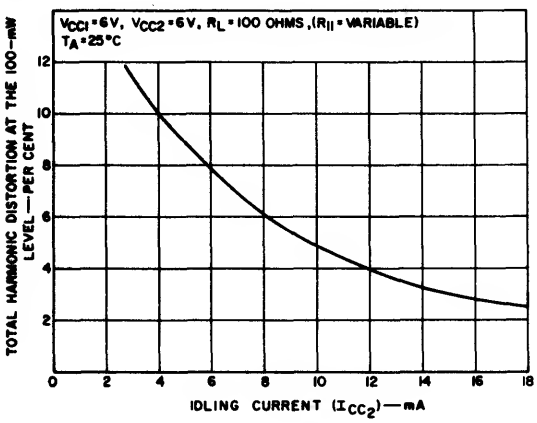


Fig. 7—Total harmonic distortion as a function of idling current for a supply voltage of 6 volts and an output of 100 milliwatts.

The CA3020 or CA3020A provides several advantages when used as a sound output stage or as a preamplifier-driver in communications equipment because each type is a compact and low-power-drain circuit. The squelching requirement in such applications is simple and economical.

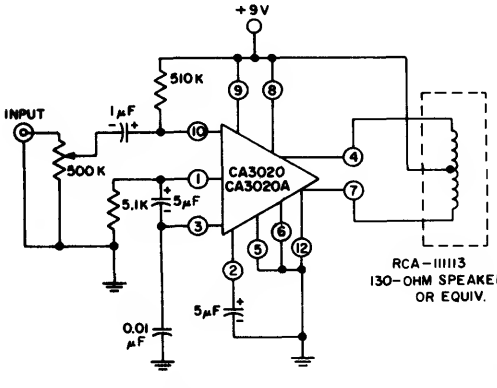


Fig. 8—310-milliwatt audio amplifier without transformers.

Fig. 9 shows a practical method of providing squelch to the CA3020 or CA3020A. When the squelch switching transistor Q_s is in the "on" state, the CA3020 or CA3020A

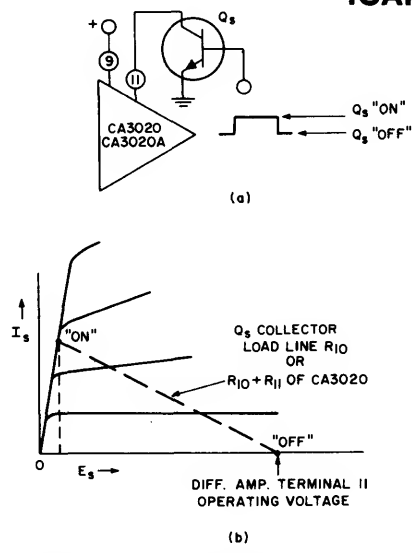


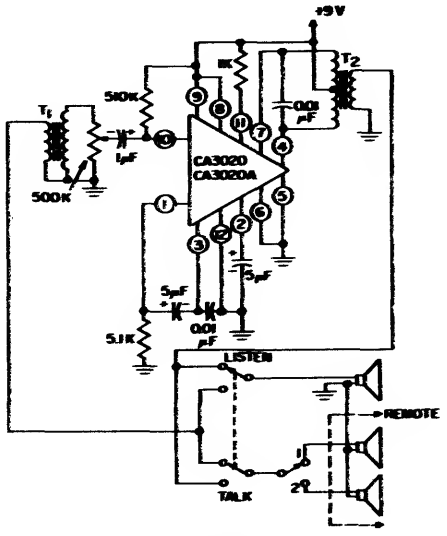
Fig. 9—Method of applying squelch to the CA3020 or CA3020A to save idling dissipation.

is "off" and draws only fractional idling dissipation. The only current that flows is that of the buffer-amplifier transistor Q_1 in the integrated circuit and the saturating current drain of Q_s. For a circuit similar to that of Fig. 8, the squelched condition requires an idling current of approximately 7 milliamperes, as compared to a normal idling-current drain of 24 milliamperes.

In applications requiring high gain and impedance matching, the CA3020 or CA3020A can be adapted for use without complex circuit modifications. Detectors having low signal outputs or high impedances can be easily matched to the input of the CA3020 or CA3020A buffer amplifier. The typical integrated-circuit input impedance of 55,000 ohms may be too low for crystal output devices such as phonograph pickups, but the sensitivity may be sacrificed to impedance-match at the input while still providing adequate drive to the CA3020 or CA3020A. Both types may be used in tape recorders as high-gain amplifiers, bias oscillators, or record and playback amplifiers. The availability of two input terminals permits the use of the CA3020 or CA3020A as a linear mixer, and thus adds to its flexibility in systems that require adaptation to multiple functions, such as communications equipment and tape recorders.

Fig. 10 illustrates the use of the audio amplifier shown in Fig. 4 in an intercom in which a listen-talk position switch controls two or more remote positions. Only the speakers, the switch, and the input transformer are added to the basic audio amplifier circuit. A suitable power supply for the intercom could be a 9-volt battery used intermittently rather than continuously.

Wide-Band Amplifiers. A major general-purpose application of the CA3020 and CA3020A is to provide high gain and wide-band amplification. The CA3020 and CA3020A



T_1: Primary 4 ohms, Secondary 25,000 ohms; Stancor A4744 or equiv.

T_2: Better Coil and Transformer DF1084, Thordarson TR-192, or equiv.

Speakers: 4 ohms

Fig. 10—Intercom using CA3020 or CA3020A.

have typically flat gain-bandwidth response to 8 MHz. Although the circuits are normally biased for class B operation, only the output stages operate in this mode. If proper dc bias conditions are applied, the output stages may be operated as linear class A amplifiers.

Fig. 11 shows the recommended method for achieving an economical and stable class A bias. The differential-amplifier portion of the CA3020A is placed at a potential

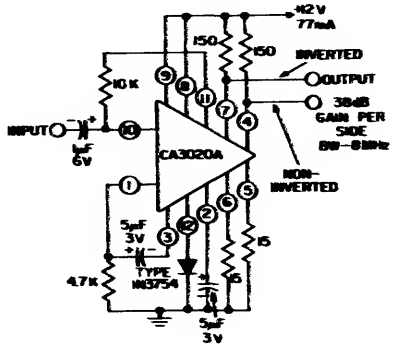


Fig. 11—Wide-band video amplifier illustrating economical and stable class A bias of CA3020A.

above ground equal to the base-to-emitter voltage V_{be} of the integrated-circuit transistors (0.5 to 0.7 volt). In this condition, the output stages have an emitter-current bias approximately equal to the base-to-emitter voltage divided by the emitter-to-ground resistance. The circuit in Fig. 11 is a wide-band video amplifier that provides a gain of 38 dB at each of the push-pull outputs, or 44 dB in a balanced-output connection. The 3-dB bandwidth of the circuit is 30 Hz to 8 MHz. Higher gain-bandwidth performance can be achieved if the diode-to-ground voltage drop at terminal 12 is reduced. The lower voltage drop permits the use of a higher ratio of output-stage collector-to-emitter resistors without departure from the desired portion of the class A load line. It is important to note that the temperature coefficient of the terminal-12-to-ground reference element should be sufficiently low to prevent a large change in the current of the output stages.

The same method for achieving class A bias is used in the large-signal-swing output amplifier shown in Fig. 12.

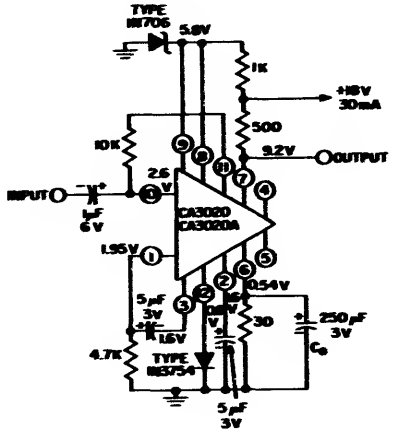


Fig. 12—Large-signal-swing output amplifier using CA3020 or CA3020A.

Either the CA3020 or the CA3020A may be used in this circuit with power supplies below +18 volts; the CA3020A can also be used with B+ voltages up to 25 volts with non-inductive loads. The circuit of Fig. 12 provides a gain of 60 dB and a bandwidth of 3.2 MHz if the output transistor Q_7 has a bypassed emitter resistor. With an unbypassed output emitter resistor, the gain is 40 dB and the bandwidth is 8 MHz. The output stage can deliver a 5-volt-rms signal when a supply of +18 volts is used. For better performance in this type of circuit, the input signal is coupled from the buffer amplifier Q_1 to the input terminal 3 of the differential amplifier. This arrangement provides higher gain because the collector resistor of the differential-amplifier transistor Q_2 is larger than that of Q_2. (This difference results from a requirement of differential drive balance that is not used in this circuit.) In addition, the terminals of the unused output transistor Q_6 help to form an isolating shield between the input at terminal 3 and the output at terminal 7. This cascade of amplifiers has a single phase inversion at the output for much better stability than could be achieved if terminal 4 were used as the output and terminal 3 as the input.

Fig. 13 illustrates the use of the CA3020 or CA3020A as a class A linear amplifier. This circuit features a very

low output impedance and may be used as a line-driver amplifier for wide-band applications up to 8 MHz. The circuit requires a 0.12-volt peak-to-peak input for a single-ended output of 1 volt or a balanced peak-to-peak output of 2 volts from a 3-ohm output impedance at each emitter. The input impedance is specified as 7800 ohms, but is primarily a function of the external 10,000-ohm resistor that provides bias to Q_1 from the regulating terminal 11.

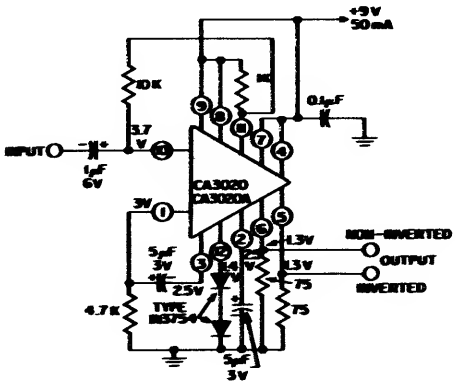


Fig. 13—Class A linear amplifier using CA3020 or CA3020A.

Fig. 14 illustrates the practical use of the CA3020 or CA3020A as a tuned amplifier. This circuit uses dc biasing similar to that shown previously, and has a gain of 70 dB at a frequency of 160 kHz. The CA3020 or CA3020A can be used as a tuned rf amplifier or oscillator at frequencies well beyond the 8-MHz bandwidth of the basic circuit.

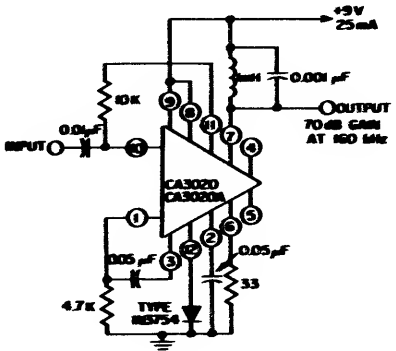
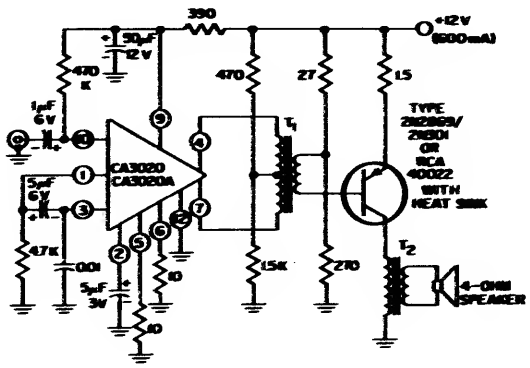


Fig. 14—160-kHz tuned amplifier using the CA3020 or CA3020A.

Driver Amplifiers. The high power-gain and power-output capabilities of the CA3020 and CA3020A make these integrated circuits highly suitable for use as drivers for higher-power stages. In most applications, the full power-output capability of the circuit is not required, and large emitter resistors may be used in the output stage to reduce distortion. The CA3020 and CA3020A can drive any transformer-coupled load within their respective ratings. Several examples of typical applications are given below.

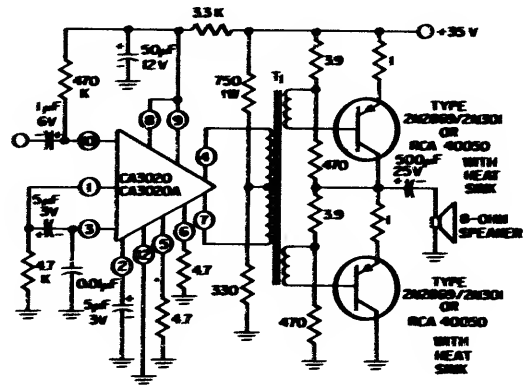
Fig. 15 illustrates the use of the CA3020 or CA3020A to drive a germanium power-output transistor to a 2.5-watt level. Because the integrated circuit is required to deliver a maximum power output of less than 50 milliwatts, an unbypassed emitter resistor can be used in the output stage to reduce distortion. Sensitivity for an output of 2.5 watts is 3 millivolts; this figure can be improved at a slight increase in distortion by reduction of the 4.7-ohm resistors between terminals 5 and 6 and ground.



T_1: primary impedance, 10,000 ohms; center-tapped at 160 ohms; primary direct current, 2 milliamperes; Thordarson TR-287 (entire secondary), or equiv.

T_2: primary impedance, 20 ohms; primary direct current, 0.6 ampere; secondary, 4 ohms; Thordarson TR-304, Stancor TP62, or equiv.

Fig. 15—2.5-watt class A audio amplifier using the CA3020 or CA3020A as a driver amplifier.



T_1: primary impedance, 4,000 ohms; center-tapped; secondary impedance, 600 ohms; center-tapped, split; Thordarson TR-454 or equivalent.

Fig. 16—10-watt single-ended class B audio amplifier using the CA3020 or CA3020A as a driver amplifier.

Because so little of the power-output capability of the CA3020 or CA3020A is used, higher-power class B stages can easily be accommodated by selection of suitable output transistors and appropriate transformers.

Fig. 16 shows a medium-power class B audio amplifier in which the CA3020 or CA3020A is used as a driver. The output stage uses a pair of TO-3-type germanium output transistors which must be mounted on a heat sink for reliable operation. Idling current for the entire system is 70 milliamperes from the 35-volt supply. Sensitivity is 10 millivolts for an output of 10 watts.

Motor Controller and Servo Amplifier. The CA3020 or CA3020A may be used as a 40-to-400-Hz motor controller and servo amplifier, as shown in Fig. 17.

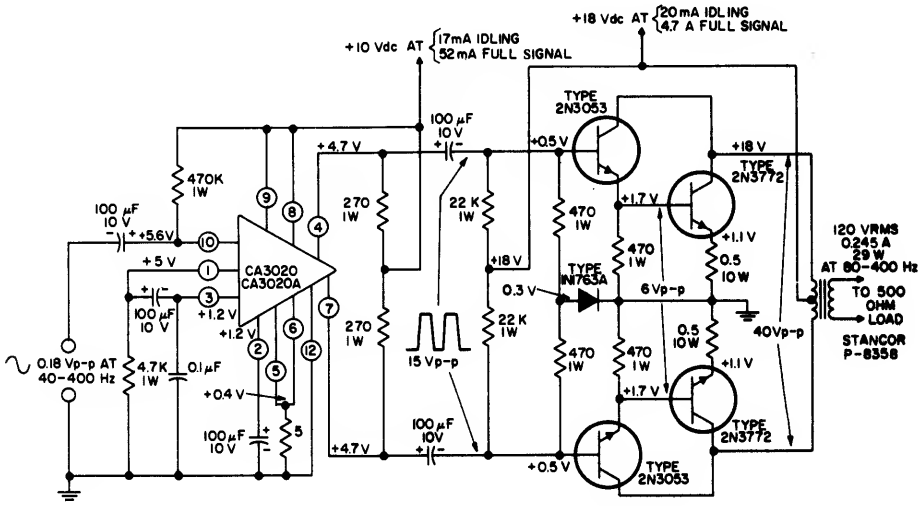


Fig. 17—Motor controller and servo amplifier using CA3020 or CA3020A.

Some Applications of A Programmable Power Switch/Amplifier

by L. R. Campbell and H. A. Wittlinger

The RCA-CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

Class A instrumentations and power amplifiers

Class A driver-amplifier for complementary power transistors

Wide-frequency-range power multivibrators

Current- or voltage-controlled oscillators

Comparators (threshold detectors)

Voltage regulators

Analog timers (long time delays)

Alarm systems

Motor-speed controllers

Thyristor-firing circuits

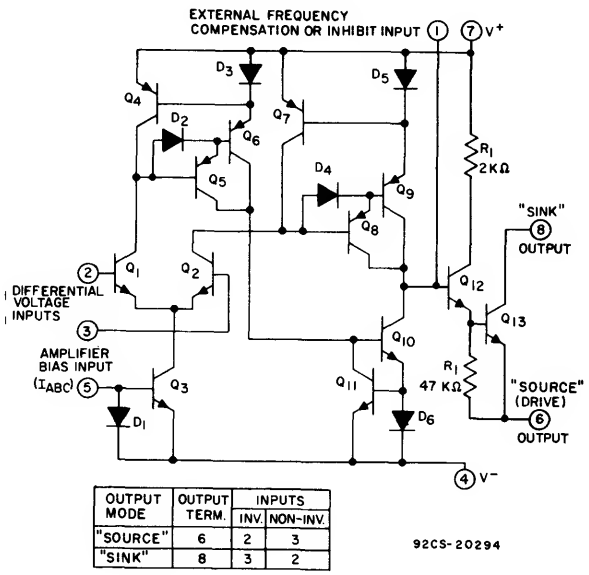
Battery-charger regulator circuits

Ground-fault-interrupter circuits

Circuit Description

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic IC's dissipate only a few microwatts when quiescent, they have a high current-output capability (100 milliamperes average, 300 milliamperes peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44 volts.

Fig. 1 shows a schematic diagram of the CA3094. The portion of the circuit preceding transistors Q_{12} and Q_{13} is the preamplifier section and is generically similar to that of the RCA-CA3080 Operational Transconductance Amplifier (OTA).[1,2] The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current (I_{ABC}) terminal (No. 5 in Fig. 1) to control circuit sensitivity. Response of the amplifier is essentially linear as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in many applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a single-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darlington-connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.



OUTPUT MODE	OUTPUT TERM.	INPUTS	
		INV.	NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1—CA3094 circuit schematic diagram.

The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as

shown below; other electrical characteristics are identical.

Package Options	Maximum Voltage Rating
CA3094S; CA3094T	24 V
CA3094AS; CA3094AT	36 V
CA3094BS; CA3094BT	44 V

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8-lead dual-in-line configuration (0.1" pin spacing). The suffix "T" indicates circuits packaged in 8-lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout this Note.

Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance (g_m R_L), feedback is not needed to obtain predictable open-loop gain performance. Fig. 2 shows the CA3094 in this basic type of circuit.

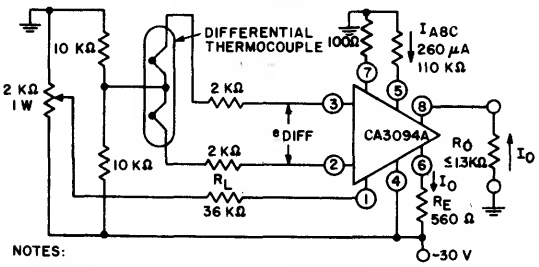


Fig.2—Open-loop instrumentation amplifier with differential input and single-ended output.

The gain of the preamplifier section (to terminal No. 1) is g_m R_L = (5 x 10^{-3}) (36 x 10^3) = 180. The transconductance g_m is a function of the current into terminal No. 5, I_{ABC}, the amplifier-bias-current. In this circuit an I_{ABC} of 260 microamperes results in a g_m of 5 millimhos. The operating point of the output stage is controlled by the 2-kilohm potentiometer. With no differential input signal (e_{diff} = 0), this potentiometer is adjusted to obtain a quiescent output current I_O of 12 milliamperes. This output current is established by the 560-ohm emitter resistor, R_E, as follows:

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

Under the conditions described, an input swing e_{diff} of ±26 millivolts produces a variation in the output current I_O of ±8.35 milliamperes. The nominal quiescent output voltage is 12 milliamperes times 560 ohms or 6.7 volts. This output level drifts approximately −4 millivolts, or −0.0595 per cent, for each °C change in temperature. Output drift is caused by temperature-induced variations in the base-emitter voltage of the two output transistors, Q_{12} and Q_{13}.

Fig. 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Fig. 4 shows a single-supply

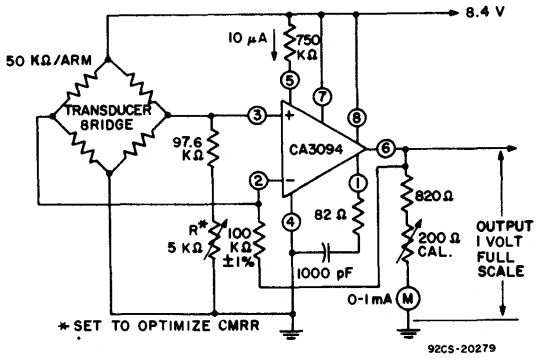


Fig.3—Single-supply differential-bridge amplifier.

amplifier for thermocouple signals. The RC networks* connected between terminals 1 and 4 in Figs. 3 and 4 provide compensation to assure stable operation.

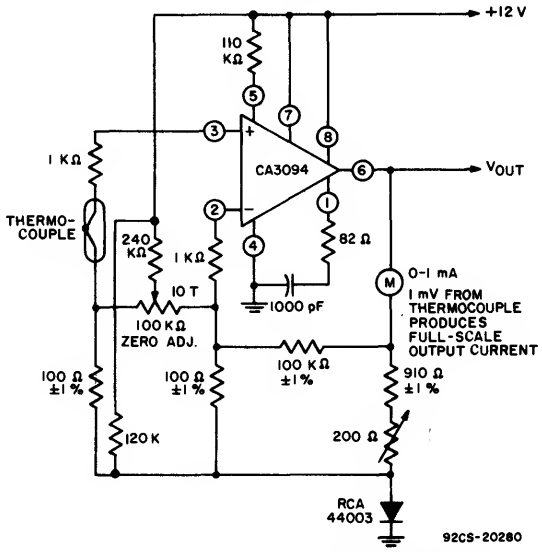


Fig.4—Single-supply amplifier for thermocouple signals.

Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100 milliamperes (300 milliamperes peak), the premium devices

*The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2 \text{ MHz}.$$

(CA3094B) can operate at supply voltages up to 44 volts, and the TO-5 package can dissipate power up to 1.6 watts when equipped with a suitable heat sink that limits the case temperature to 55°C.

Fig. 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280 milliwatts to a 350-ohm resistive load. This circuit has a voltage gain of 60 dB and a

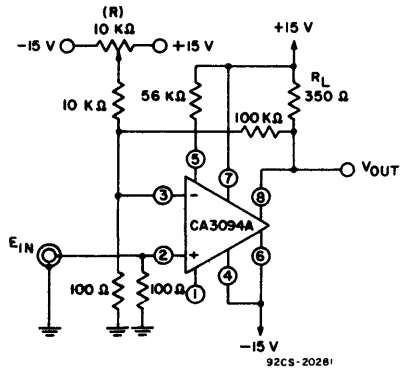


Fig.5—Class-A amplifier — 280-mW capability into a resistive load.

3-dB bandwidth of about 50 kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

The circuit of Fig. 6 illustrates the use of the CA3094 in a class A power-amplifier circuit driving a transformer-coupled load. With dual power supplies of +7.5 volts and −7.5 volts, a

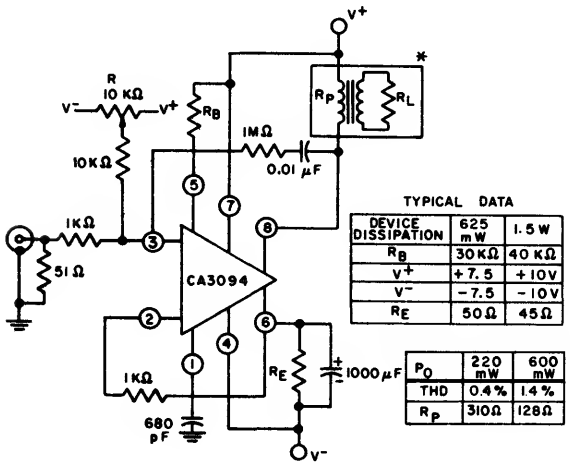


Fig.6—Class-A amplifier with transformer-coupled load.

base resistor R_B of 30 kilohms, and an emitter resistor R_E of 50 ohms, CA3094 dissipation is typically 625 milliwatts. With supplies of +10 volts and −10 volts, R_B of 40 kilohms, and R_E of 45 ohms, the dissipation is 1.5 watts. Total harmonic distortion is 0.4 per cent at a power-output level of 220 milliwatts with a reflected load resistance R_P of 310 ohms, and is 1.4 per cent for an output of 600 milliwatts with an R_P of 128 ohms. The setting of potentiometer R establishes the quiescent operating point for class A operation. The 1-kilohm resistor connected between terminals 6 and 2 provides dc feedback to stabilize the collector current of the output transistor. The ac gain is established by the ratio of the 1-megohm resistor connected between terminals 8 and 3 and the 1-kilohm resistor connected to terminal 3. Phase compensation is provided by the 680-picofarad capacitor connected to terminal 1.

Class A Driver-Amplifier for Complementary Power Transistors

The CA3094 configuration and characteristics are ideal for driving complementary power-output transistors;[3] a typical circuit is shown in Fig. 7. This circuit can provide 12 watts of audio power output into an 8-ohm load with intermodulation distortion (IMD) of 0.2 per cent when 60-Hz and 2-kHz signals are mixed in a 4:1 ratio. Intermodulation distortion is shown as a function of power output in Fig. 8.

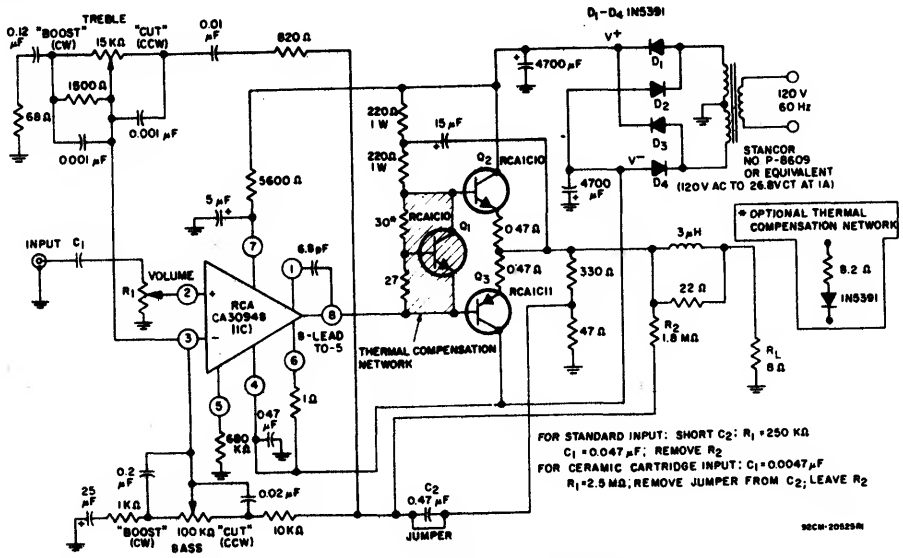
The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. The tone controls in the circuit of Fig. 7 are part of the feedback network connected from the amplifier output (junction of the 330- and 47-ohm resistors driven by the emitters of Q_2 and Q_3) to terminal 3 of the CA3094. Fig. 9 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls incorporated in the feedback network results in excellent signal-to-noise ratio. Hum and noise are typically 700 microvolts (83 dB down) at the output.

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 dB and 100 dB, respectively. An amplifier with 40-dB gain and 90-dB power-supply rejection would require a 31-millivolt power-supply ripple to produce one millivolt of hum at the output. Therefore, no filtering is required other than that provided by the energy-storage capacitors at the output of the rectifier system shown in Fig. 7.

For applications in which the operating temperature range is limited (e.g., consumer service) the thermal compensation network (shaded area) can be replaced by a more economical configuration consisting of a resistor-diode combination (8.2 ohms and 1N5391) as shown in Fig. 7.

Power Multivibrators (Astable and Monostable)

The CA3094 is suitable for use in power multivibrators because its high-current output transistor can drive low-impedance circuits while the input circuitry and the frequency-determining elements are operating at micropower levels. A typical example of an astable multivibrator using the CA3094 with a



For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9	

Fig.7—12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

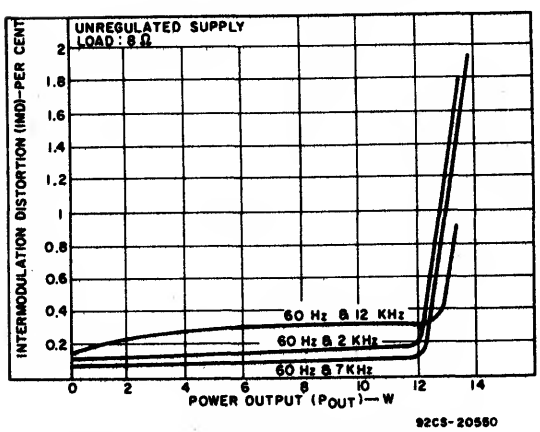


Fig.8—Intermodulation distortion vs. power output.

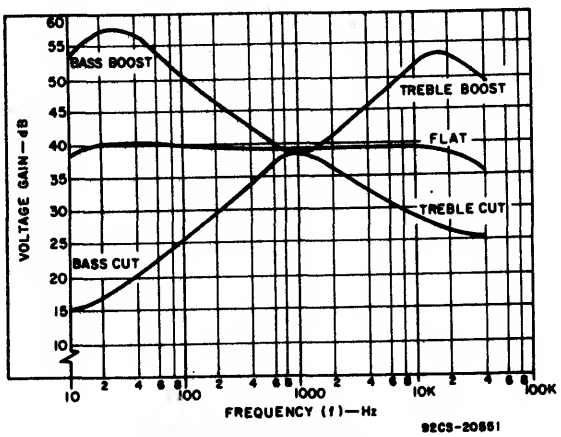


Fig.9—Voltage gain vs. frequency.

dual power supply is shown in Fig. 10. The output frequency f_{OUT} is determined as follows:

$$f_{OUT} = \frac{1}{2RC\ln[(2R1/R2) + 1]}$$

If R2 is equal to 3.08 R1, then f_{OUT} is simply the reciprocal of RC.

Fig. 11 is a single-supply astable multivibrator circuit which illustrates the use of the CA3094 for flashing an incandescent lamp. With the component values shown, this circuit produces one flash per second with a 25-per-cent "on"-time while delivering output current in excess of 100 milliamperes. During

the 75-per-cent "off"-time it idles with micropower consumption. The flashing rate can be maintained within ±2 per cent of the nominal value over a battery voltage range from 6 to 15 volts and a temperature excursion from 0 to 70°C. The CA3094 series of circuits can supply peak-power output in excess of 10 watts when used in this type of circuit. The frequency of oscillation f_{OSC} is determined by the resistor ratios, as follows:

$$f_{OSC} = \frac{1}{2RC\ln[(2R_1/R_2)+1]}$$

where

$$R1 = \frac{R_A R_B}{R_A + R_B}$$

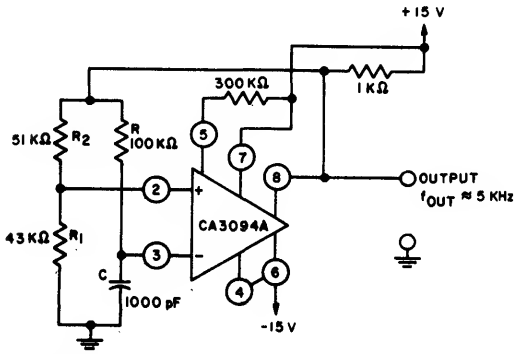
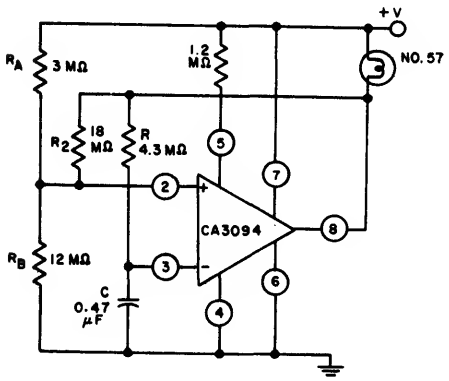


Fig. 10—Astable multivibrator using dual supply.



FEATURES

- 1 FLASH/SEC. $f_{OSC} = \frac{1}{2RC\ln[(2R_1/R_2+1)]}$ WHERE $R_1 = \frac{R_A R_B}{R_A+R_B}$
- 25 % DUTY CYCLE
- FREQUENCY INDEPENDENT OF V+ FROM 6-15 V DC

92CS-20293

Fig. 11—Astable multivibrator using single supply.

Provisions can easily be made in the circuit of Fig. 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown in Fig. 12 incorporates a potentiometer Rp for varying the width of pulses generated by the astable multivibrator to drive a light-emitting diode (LED).

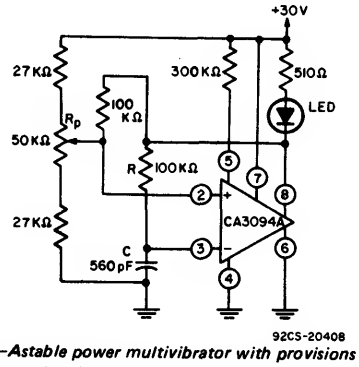


Fig. 12—Astable power multivibrator with provisions for varying duty cycle.

Fig. 13 shows a circuit incorporating independent controls (R_{ON} and R_{OFF}) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100-kilohm resistor R in Fig. 12.

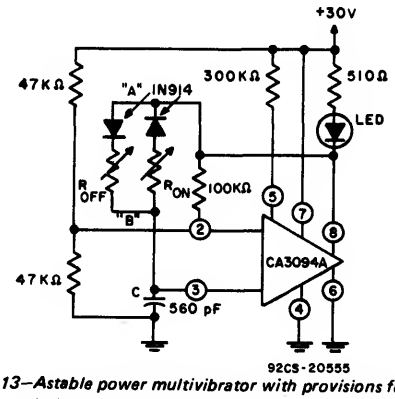


Fig. 13—Astable power multivibrator with provisions for independent control of LED "on-off" periods.

The CA3094 is also suitable for use in monostable multivibrators, as shown in Fig. 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger-pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

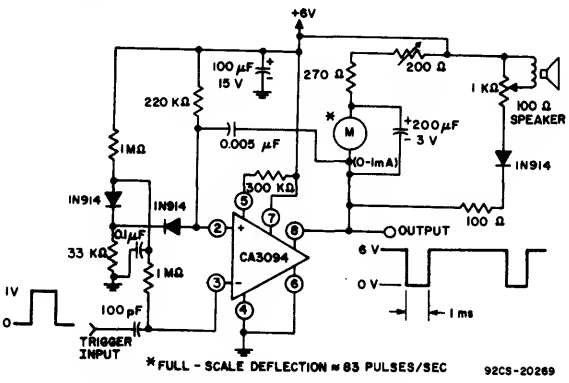


Fig. 14—Power monostable multivibrator.

Current- or Voltage-Controlled Oscillators

Because the transconductance of the CA3094 varies linearly as a function of the amplifier bias current (I_{ABC}) supplied to terminal 5, the design of a current- or voltage-controlled oscillator is straightforward, as shown in Fig. 15. Fig. 16 and 17 show oscillator frequency as a function of I_{ABC} for a current-controlled oscillator for two different values of capacitor C in Fig. 15. The addition of an appropri-

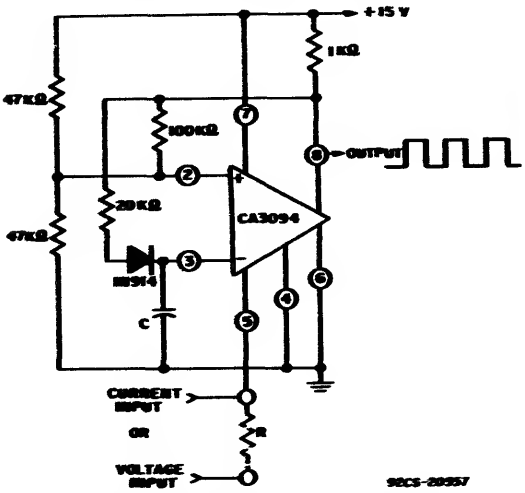


Fig. 15—Current- or voltage-controlled oscillator.

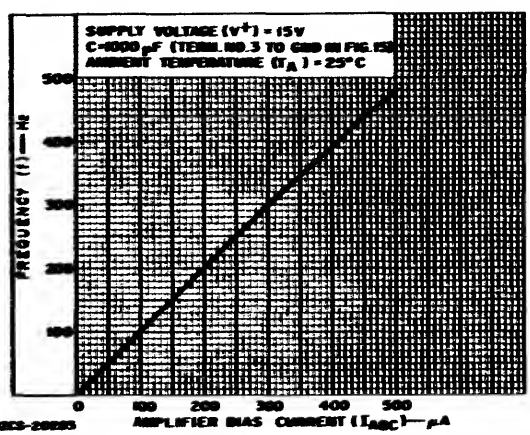


Fig. 16—Frequency as a function of I_{ABC} for C=1000 pF for circuit in Fig. 15.

ate resistor (R) in series with terminal 5 in Fig. 15 converts the circuit into a voltage-controlled oscillator. Linearity with respect to either current or voltage control is within 1 per cent over the middle half of the characteristics. However, variation in the symmetry of the output pulses as a function of frequency is an inherent characteristic of the circuit in Fig. 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type of distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase-locked discriminator circuits.

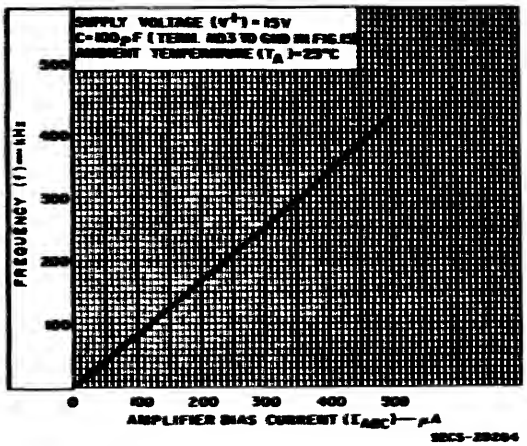


Fig. 17—Frequency as a function of I_{ABC} for C=100 pF for circuit in Fig. 15.

Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA3094, as shown by the circuits in Fig. 18. The circuit of Fig. 18(a) is arranged for dual-supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply-voltage rail (it is assumed that there is negligible resistive loading on the output ter-

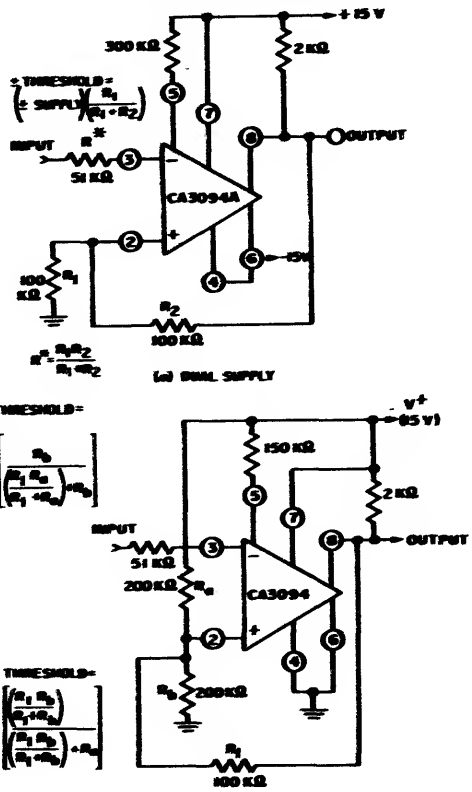


Fig. 18—Comparators (threshold detectors) — dual- and single-supply types.

minal). An input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Fig. 18(b), connected for single-supply operation, functions similarly.

Fig. 19 shows a dual-limit threshold detector circuit in which the high-level limit is established by potentiometer R1

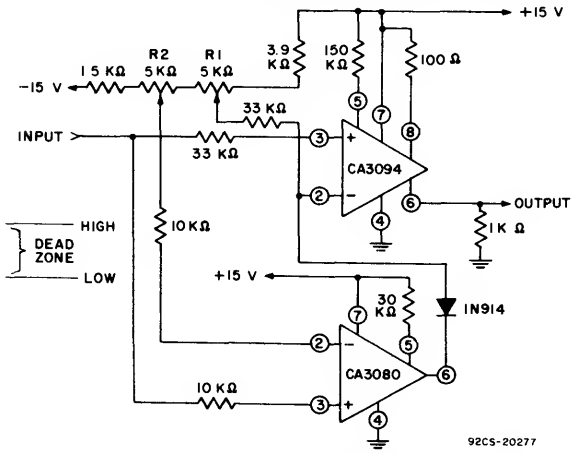


Fig. 19—Dual-limit threshold detector.

and the low-level limit is set by potentiometer R2 to actuate the CA3080 low-limit detector.[1,2] A positive output signal is delivered by the CA3094 whenever the input signal exceeds either the high-limit or the low-limit values established by the appropriate potentiometer settings. This output voltage is approximately 12 volts with the circuit shown.

The high current-handling capability of the CA3094 makes it useful in Schmitt power-trigger circuits such as that shown in Fig. 20. In this circuit, a relay coil is switched whenever the

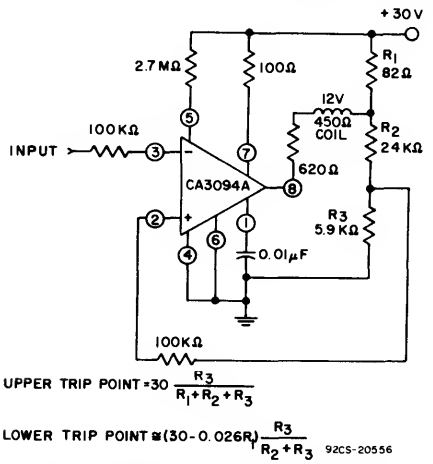


Fig. 20—Precision Schmitt power-trigger circuit.

input signal traverses a prescribed upper or lower trip point, as defined by the following expressions:

$$\text{Upper Trip Point} = 30\left(\frac{R3}{R1 + R2 + R3}\right)$$

$$\text{Lower Trip Point} \cong (30 - 0.026R1)\frac{R3}{R2 + R3}$$

The circuit is applicable, for example, to automatic ranging. With the values shown in Fig. 20, the relay coil is energized when the input exceeds approximately 5.9 volts and remains energized until the input signal drops below approximately 5.5 volts.

Power-Supply Regulators

The CA3094 is an ideal companion device to the CA3085 series regulator circuits[4] in dual-voltage tracking regulators that handle currents up to 100 milliamperes. In the circuit of Fig. 21, the magnitude of the regulated positive voltage provided by the CA3085A is adjusted by potentiometer R. A sample of this positive regulated voltage supplies the power for the CA3094A negative regulator and also supplies a refer-

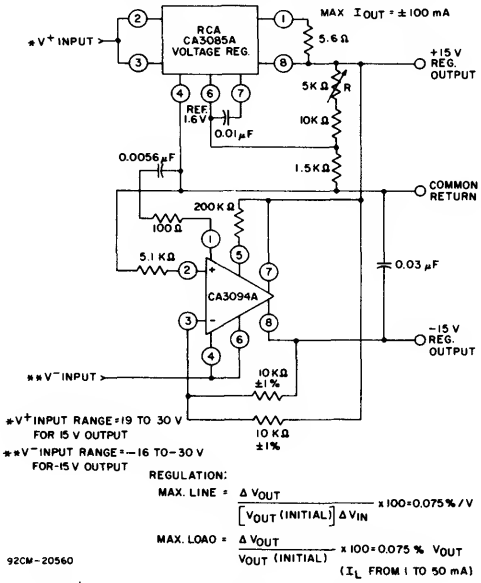


Fig. 21—Dual-voltage tracking regulator.

ence voltage to its terminal 3 to provide tracking. This circuit provides a maximum line regulation equal to 0.075 per cent per volt of input voltage change and a maximum load regula- of 0.075 per cent of the output voltage.

Fig. 22 shows a regulated high-voltage supply similar to the type used to supply power for Geiger-Mueller tubes. The CA3094, used as an oscillator, drives a step-up transformer which develops suitable high voltages for rectification in the RCA-44007 diode network. A sample of the regulated output voltage is fed to the CA3080A operational transconductance amplifier through the 198-megohm and 910-kilohm divider to control the pulse repetition rate of the CA3094. Adjustment of potentiometer R determines the magnitude of the regulated output voltage. Regulation of the desired output voltage is maintained within one per cent despite load-current variations of 5 to 26 microamperes. The dc-to-dc conversion efficiency is about 48 per cent.

Timers

The programmability feature inherent in the CA3094 (and operational transconductance amplifiers in general) simplifies the design of presettable timers such as the one shown in

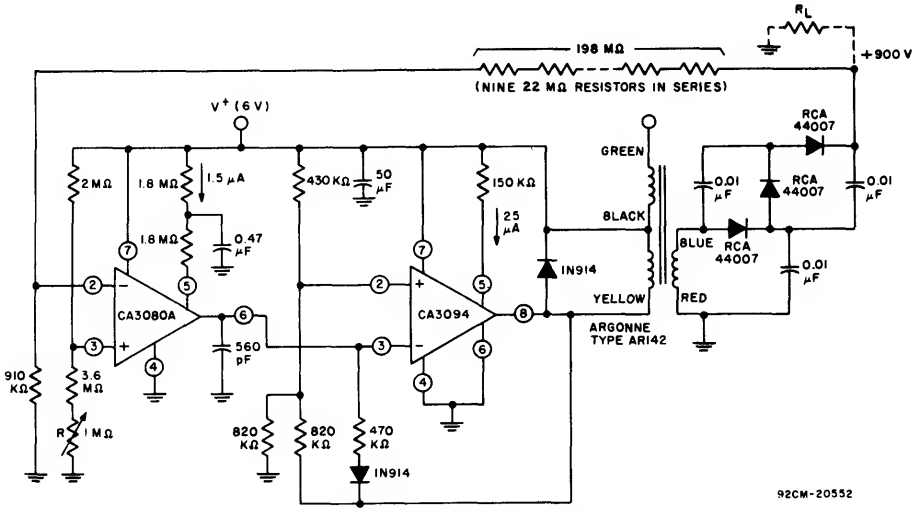


Fig.22—Regulated high-voltage supply.

Fig. 23. Long timing intervals (e.g., up to 4 hours) are achieved by discharging a timing capacitor C_1 into the signal-input terminal (e.g., No. 3) of the CA3094. This discharge current is controlled precisely by the magnitude of the amplifier bias current I_{ABC} programmed into terminal 5 through a resistor selected by switch S2. Operation of the circuit is initiated by charging capacitor C_1 through the momentary closing of switch S_1. Capacitor C_1 starts discharging and continues discharging until voltage E_1 is less than voltage E_2. The differential input transistors in the CA3094 then change state, and terminal 2 draws sufficient current to reverse the polarity of

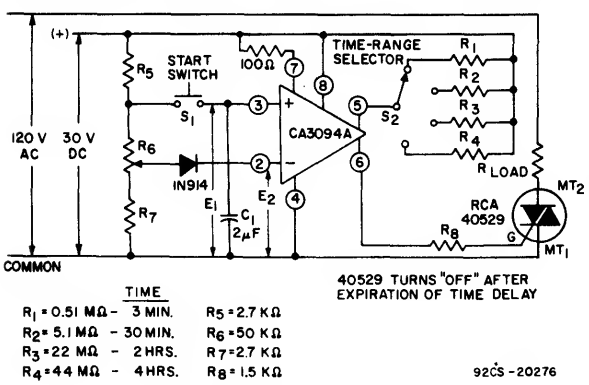


Fig.23—Presettable analog timer.

the output voltage (terminal 6). Thus, the CA3094 not only has provision for readily presetting the time delay, but also provides significant output current to drive control devices such as thyristors. Resistor R_5 limits the initial charging current for C_1. Resistor R_7 establishes a minimum voltage of at least 1 volt at terminal 2 to insure operation within the common-mode-input range of the device. The diode limits the maximum differential input voltage to 5 volts. Gross changes in time-range selection are made with switch S2, and vernier trimming adjustments are made with potentiometer R_6.

In some timer applications, such as that shown in Fig. 24, a meter readout of the elapsed time is desirable. This circuit uses the CA3094 and the CA3083 transistor array[5] to control the meter and a load-switching triac. The timing cycle starts with the momentary closing of the start switch to charge capacitor C_1 to an initial voltage determined by the 50-kilohm vernier timing adjustment. During the timing cycle, capacitor C_1 is discharged by the input bias current at terminal 3, which is a function of the resistor value R_1 chosen by the time-range selection switch. During the timing cycle the output of the CA3094, which is also the collector voltage of Q_1, is "high". The base drive for Q_1 is supplied from the positive supply through a 91-kilohm resistor. The emitter of Q_1, through the 75-ohm resistor, supplies gate-trigger current to the triac. Diode-connected transistors Q_4 and Q_5 are connected so that transistor Q_1 acts as a constant-current source to drive the triac. As capacitor C_1 discharges, the CA3094 output voltage at terminal 6 decreases until it becomes less than the V_{CEsat} of Q_1. At this point the flow of drive current to the triac ceases and the timing cycle is ended. The 20-kilohm resistor between terminals 2 and 6 of the CA3094 is a feedback resistor. Diode-connected transistors Q_2 and Q_3 and their associated networks serve to compensate for nonlinearities in the discharge-circuit network by bleeding corrective current into the 20-kilohm feedback resistor. Thus, current flow in the meter is essentially linear with respect to the timing period. The time periods as a function of R_1 are indicated on the Time-Range Selection Switch in Fig. 24.

Alarm Circuit

Fig. 25 shows an alarm circuit utilizing two "sensor" lines. In the "no-alarm" state, the potential at terminal 2 is lower than the potential at terminal 3, and terminal 5 (I_{ABC}) is driven with sufficient current through resistor R_5 to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the output goes "low" and activates some type of alarm system.

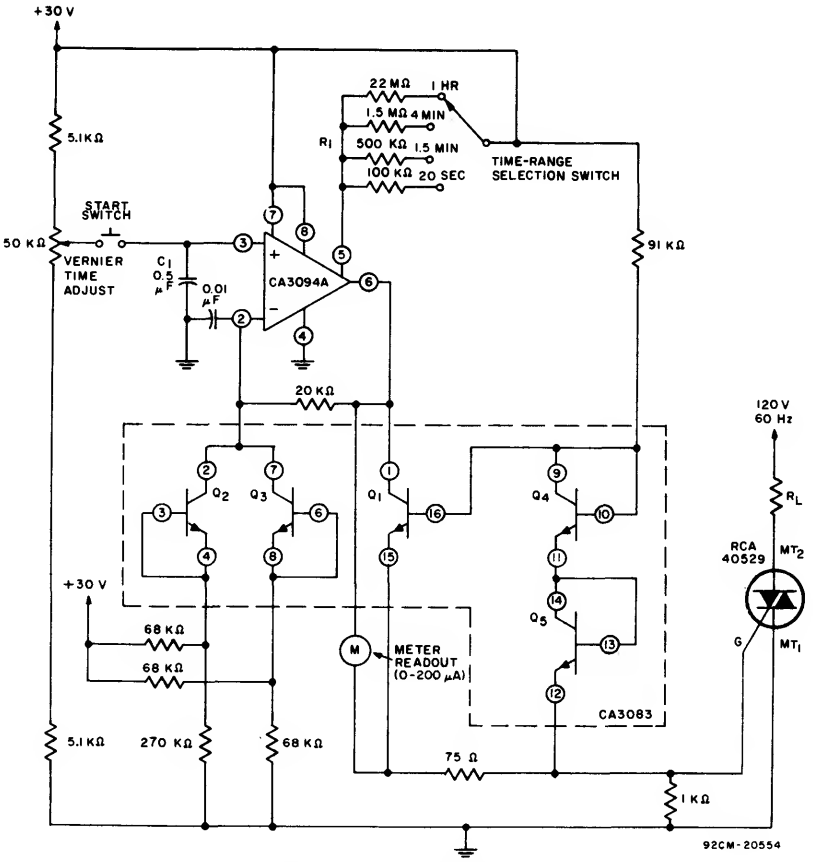


Fig.24—Presettable timer with linear readout.

The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

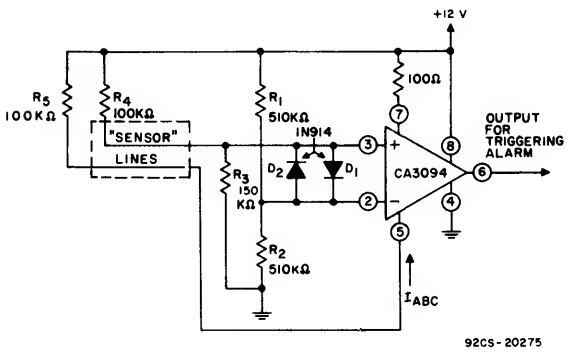


Fig.25—Alarm system.

Motor-Speed Controller System

Fig. 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuitry associated with rectifiers D_1 and D_2 comprises a full-wave rectifier which develops a train of half-sinusoid voltage pulses to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half-cycle) the SCR is conductive.

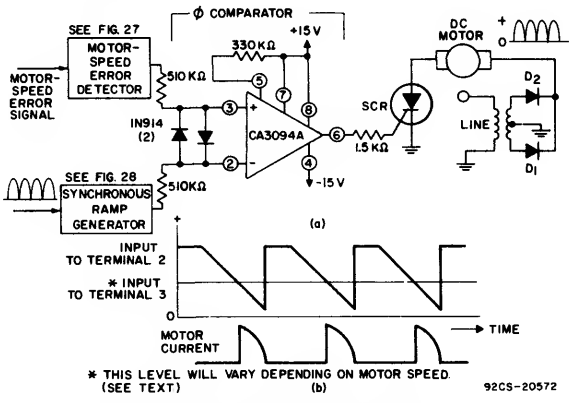


Fig.26—Motor-speed controller system.

The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Fig. 27. This dc voltage is compared to that of a fixed-amplitude ramp wave generated synchronously with the ac-line-voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period

when the ramp potential is less than that of the error voltage on terminal 3. The motor-current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Motor-speed accuracy of ±1 per cent is easily obtained with this system.

Motor-Speed Error Detector. Fig. 27(a) shows a motor-speed error detector suitable for use with the circuit of Fig. 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage E_1 is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Fig. 27(b) also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error-correction response time.

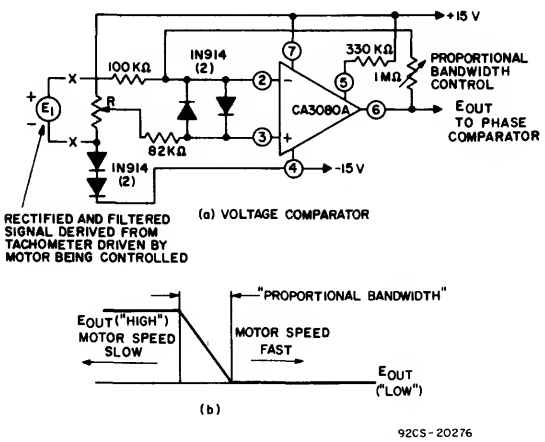


Fig. 27—Motor speed error detector.

Synchronous Ramp Generator. Fig. 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor-controller circuit of Fig. 26. Terminal 3 is biased at approximately +2.7 volts (above the negative supply voltage). The input signal E_{IN} at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Fig. 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor C_1 in response to the synchronous toggling of E_{IN}. The charging current for C_1 is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors Q_{12} and Q_{13} in the CA3094 (Fig. 1) lose their base drive and become non-conductive. Under these conditions, C_1 discharges linearly through the external diode D_3 and the Q_{10}, D_6 path in the CA3094 to produce the ramp wave. The E_{out} signal is supplied to the phase comparator in Fig. 26.

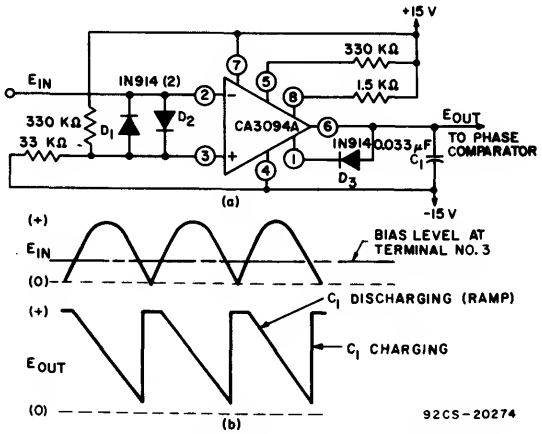


Fig.28—Synchronous ramp generator with input and output waveforms.

Thyristor Firing Circuits

Temperature Controller. In the temperature control system shown in Fig. 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive-temperature-coefficient) temperature sensor, two 75-kilohm resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC-type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5-kilohm resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power-supply-rejection and common-mode-rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power-supply ripple. The circuit of Fig. 29 is equally suitable for use with NTC (negative-temperature-coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back-to-back across the input terminals of the CA3094 protect the device against excessive differential input signals.

Thyristor Control from AC-Bridge Sensor. Fig. 30 shows a line-operated thyristor-firing circuit controlled by a CA3094 that operates from an ac-bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from dc. The CA3094 is inoperative when the high side of the ac line is negative because there is no I_{ABC} supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the ac line swings positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the 1N3193 diode to charge the 100-microfarad reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the ac line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

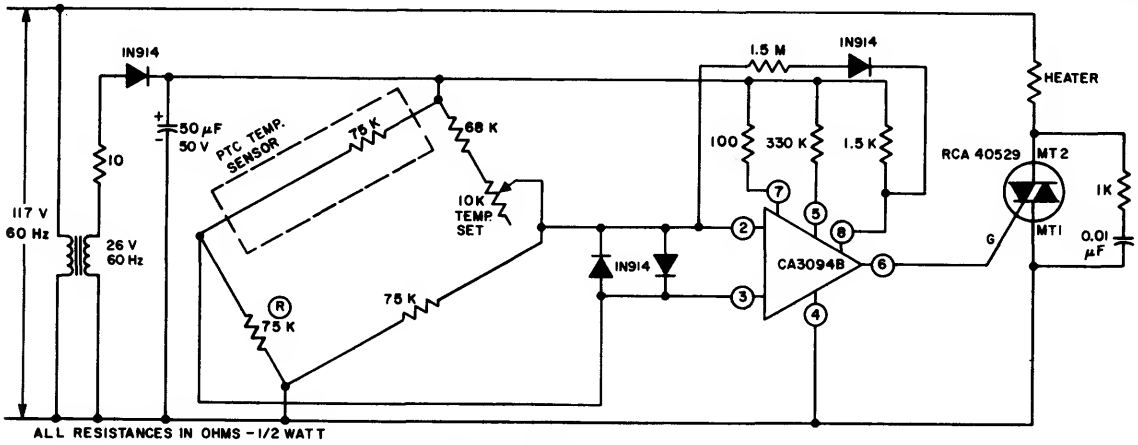


Fig.29—Temperature controller.

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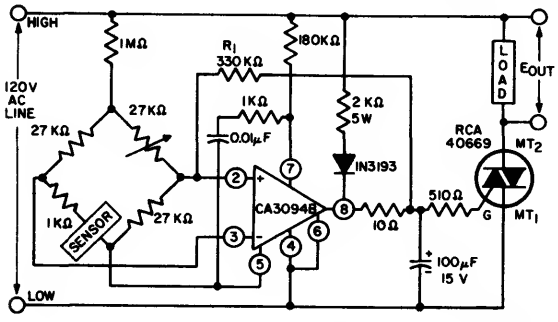

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Fig.30—Line-operated thyristor-firing circuit controlled by ac-bridge sensor.

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N3193 diode so that the triac gate cannot be triggered. Resistor R_1 supplies the hysteresis feedback to prevent rapid cycling between turn-on and turn-off.

Battery-Charger Regulator Circuit

The circuit for a battery-charger regulator circuit using the CA3094 is shown in Fig. 31. This circuit accurately limits the peak output voltage to 14 volts, as established by the zener diode connected across terminals 3 and 4. When the output voltage rises slightly above 14 volts, signal feedback through a 100-kilohm resistor to terminal 2 reduces the current drive supplied to the 2N3054 pass transistor from terminal 6 of the CA3094. An incandescent lamp serves as the indicator of charging-current flow. Adequate limiting provisions protect the circuit against damage under load-short conditions. The advantage of this circuit over certain other types of regulator circuits is that the reference voltage supply doesn't drain the battery when the power supply is disconnected. This feature is important in portable service applications, such as in a trailer where a battery is kept "on-charge" when the trailer is parked and power is provided from an ac line.

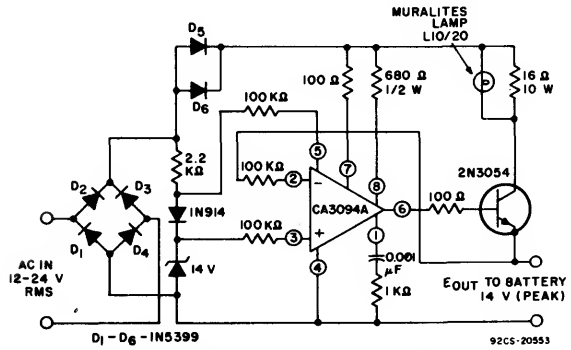

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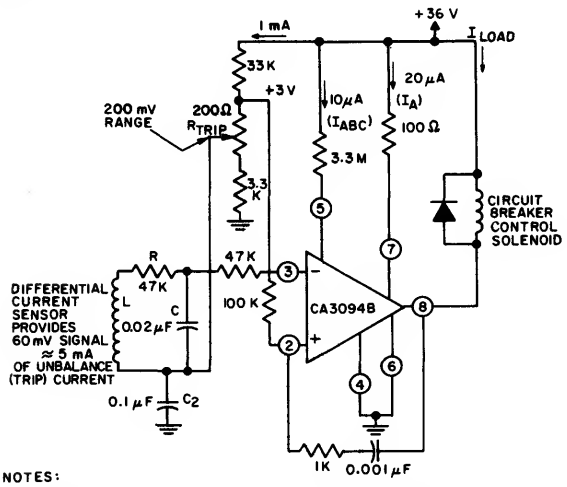
Fig.31—Battery-charger regulator circuit.

Ground-Fault Interrupters (GFI)

Ground-fault-interrupter systems are used to continuously monitor the balance of current between the high and neutral lines of power-distribution networks. Power is interrupted whenever the unbalance exceeds a preset value (e.g., 5 milliamperes). An unbalance of current can occur when, for example, defective insulation in the high side of the line permits leakage of current to an earth ground. GFI systems can be used to reduce the danger of electrocution from accidental contact with a "high" line because the unbalance caused by the leakage of current from the "high" line through a human body to ground results in an interruption of current flow.

The CA3094 is ideally suited for GFI applications because it can be operated from a single supply, has adequate sensitivity, and can drive a relay or thyristor directly to effect power interruption. Fig. 32 shows a typical GFI circuit. Vernier adjustment of the trip point is made by the R_{TRIP} potentiometer. When the differential current sensor supplies a signal that exceeds the selected trip-point voltage level (e.g., 60 millivolts), the CA3094 is toggled "on" and terminal 8 goes "low" to energize the circuit-breaker trip coil. Under quiescent conditions, the entire circuit consumes approximately 1 milliampere. The resistor R, connected to one leg of the current sensor, provides current limiting to protect the CA3094 against voltage spikes as large as 100 volts. Fig. 32 also shows the pertinent waveform for the GFI circuit.



NOTES:

1. ALL RESISTORS IN OHMS, 1/2 WATT, ±10%
2. RC SELECTED FOR 3db POINT AT 200 Hz
3. C_2=AC BY-PASS
4. OFFSET ADJ. INCLUDED IN R_{TRIP}
5. INPUT IMPEDANCE FROM 2 TO 3 EQUALS 800 K.
6. WITH NO INPUT SIGNAL TERMINAL 8 (OUTPUT) AT +36 VOLTS

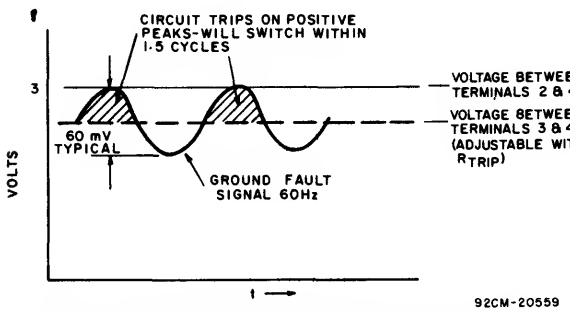


Fig.32–Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

Because hazards of severe electrical shock are a potential danger to the individual user in the event of malfunctions in GFI apparatus, it is mandatory that the highest standards of good engineering practice be employed in designing equipment for this service. Every consideration in design and application must be given to the potentially serious consequences of component malfunction in such equipment. Use of "reliability-through-redundancy" concepts and so-called "fail-safe" features is encouraged.

Acknowledgments

The authors thank A. Sheng and R. Baird for their assistance in designing some of the circuits described in this Note.

References

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2. Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers, RCA Application Note ICAN-6668.
3. L. Kaplan and H. A. Wittlinger, "An IC Operational-Transconductance-Amplifier (OTA) with Power Capability". Paper originally presented at the IEEE Chicago Spring Conference on Broadcast and TV Receivers, June 1972. Reprinted by the RCA Solid State Division as Publication No. ST-6077.
4. RCA Published Data for CA3085, File No. 491.
5. RCA Published Data for CA3083, File No. 481.

An IC Operational-Transconductance-Amplifier (OTA) With Power Capability

by L. Kaplan and H. Wittlinger

In 1969, RCA introduced the first triple operational-transconductance-amplifier or OTA. The wide acceptance of this new circuit concept prompted the development of the single, highly linear operational-transconductance-amplifier, the CA3080. Because of its extremely linear transconductance characteristics with respect to amplifier bias current, the CA3080 gained wide acceptance as a gain-control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current-carrying capability to 300 milliamperes, peak. This new device, the CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this paper describes only a few of the many consumer applications.

WHAT IS AN OTA?

The OTA, operational-transconductance-amplifier, concept is as basic as the transistor; once understood, it will broaden the designer's horizons to new boundaries and make realizable designs that were previously unobtainable. Fig. 1 shows an equivalent diagram of the OTA. The differential input circuit is the same as that found on many modern operational amplifiers. The remainder of the OTA is composed of current mirrors as shown in Fig. 2. The geometry of these mirrors is such that the current gain is unity. Thus, by highly degenerating the current mirrors, the output current is precisely defined by the differential-input amplifier. Fig. 3 shows the output-current transfer-characteristic of the amplifier. The shape of this characteristic remains

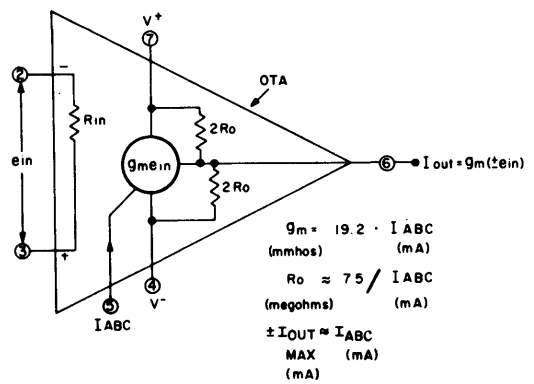

Fig. 1– Equivalent diagram of the OTA.

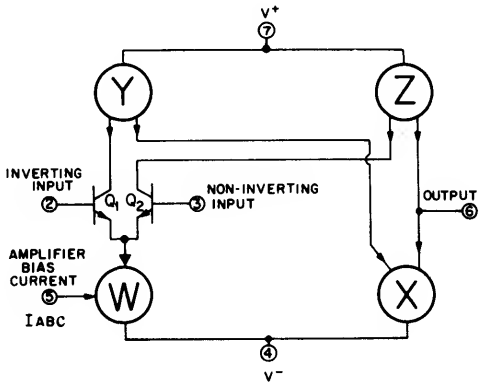

Fig. 2– Current mirrors W, X, Y, and Z used in the OTA.

constant and is independent of supply voltage. Only the maximum current is modified by the bias current.

The major controlling factor in the OTA is the input amplifier bias current I_{ABC}; as explained in Fig. 1, the total output current and gm are controlled by this current. In addition, the input bias current, input resistance, total supply current, and output resistance are all proportional to this

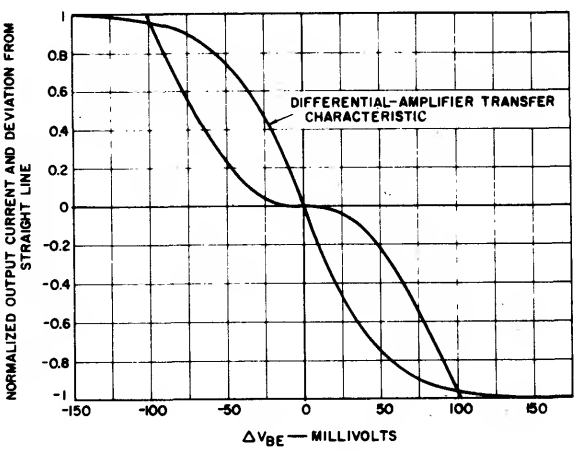

Fig. 3– The output-current transfer-characteristic of the OTA is the same as that of an idealized differential amplifier.

amplifier bias current. These factors provide the key to the performance of this most flexible device, an idealized differential amplifier, i.e., a circuit in which differential input to single-ended output conversion can be realized. With this knowledge of the basics of the OTA, it is possible to explore some of the applications of the device.

DC Gain Control

The methods of providing dc gain-control functions are numerous. Each has its advantage – simplicity, low cost, high level control, low distortion. Many manufacturers who have nothing better to offer propose the use of a four-quadrant multiplier. This is analogous to using an elephant to carry a twig. It may be elegant but it takes a lot to keep it going! When operated in the gain-control mode, one input of the standard transconductance multiplier is offset so that only one half of the differential input is used; thus, one-half of the multiplier is being thrown away.

The OTA, while providing excellent linear amplifier characteristics, does provide a simple means of gain control. For this application the OTA may be considered the realization of the ideal differential amplifier in which the full differential amplifier gm is converted to a single-ended output. Because the differential amplifier is ideal, its gm is directly proportional to the operating current of the differential-amplifier; in the OTA the maximum output current is equal to the amplifier bias current I_{ABC}. Thus, by varying the amplifier bias current, the amplifier gain may be varied: $A = Gm\ R_L$ where R_L is the output load resistance. Fig. 4 shows the basic configuration of the OTA dc gain-control circuit.[1]

As long as the differential input signal to the OTA remains under 50-millivolts peak-to-peak, the deviation from a linear transfer will remain under 5 percent. Of course, the total harmonic distortion will be considerably less than this value. Signal excursions beyond this point only result in an undesired "compressed" output. The reason for this compression can be seen in the transfer characteristic of the differential amplifier in Fig. 3. Also shown in Fig. 3 is a curve depicting the departure from a linear line of this transfer characteristic.

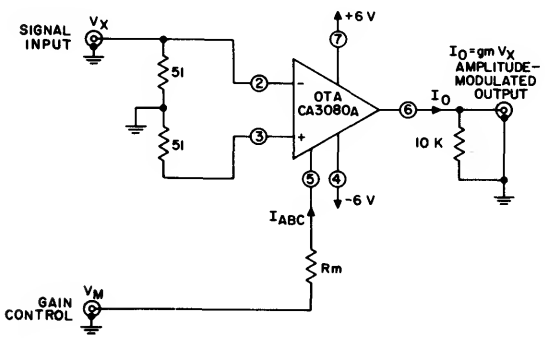

Fig. 4– Basic configuration of the OTA dc gain-control circuit.

The actual performance of the circuit shown in Fig. 4 is plotted in Fig. 5. Both signal-to-noise ratio and total harmonic distortion are shown as a function of signal input. Figs. 5(b) and (c) show how the signal-handling capability of the circuit is extended through the connection of diodes on

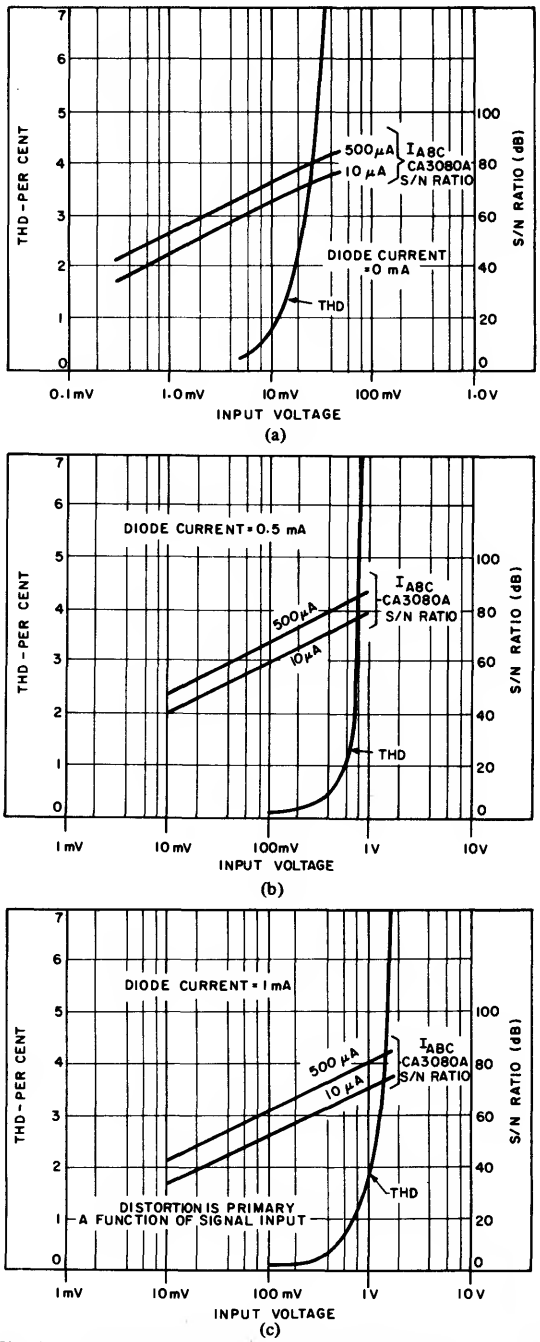

Fig. 5– Performance curves for the circuits of Figs. 4 and 6.

the input as shown in Fig. 6.[2] Fig. 7 shows total system gain as a function of amplifier bias current for several values of diode current. Fig. 8 shows an oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 4. The oscilloscope photograph of Fig. 9 was obtained with the circuit shown in Fig. 6. Note the improvement in

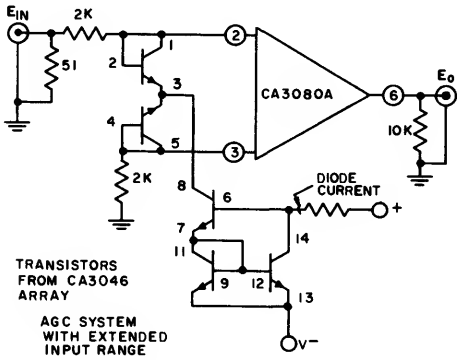

Fig. 6— A circuit showing how the signal-handling capability of the circuit of Fig. 4 can be extended through the connection of diodes on the input.

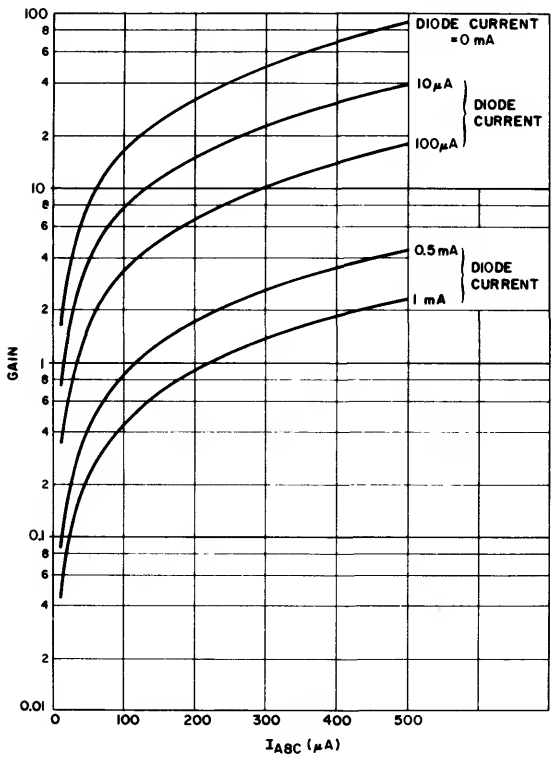

Fig. 7— Total system gain as a function of amplifier bias current for several values of diode current.

Fig. 8— Oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 4.

Fig. 9— Oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 6.

linearity of the transfer characteristic. Reduced input impedance does result from this shunt connection. Similar techniques could be used on the OTA output, but then the output signal would be reduced and the correction circuitry further removed from the source of non-linearity. It must be emphasized that the input circuitry is differential.

Simplified Differential-Input to Single-Ended Output Conversion

One of the more exacting configurations for operational amplifiers is the differential-to-single-ended conversion circuit. Fig. 10 shows some of the basic circuits that are usually employed. The ratios of the resistors must be precisely matched to assure the desired common-mode rejection. Fig. 11 shows another system using the CA3080 to obtain this conversion without the use of precision resistors. Differential input signals must be kept under ±26-millivolts for better than 5-percent non-linearity. The common-mode range is that of the CA3080 differential amplifier. In addition, the gain characteristic follows the standard differential-amplifier Gm-temperature coefficient of −0.3%/°C. Although the system of Fig. 11 does not provide the precise gain control obtained with the standard operational-amplifier approach, it does provide a good simple compromise suitable for many differential transducer-amplifier applications.

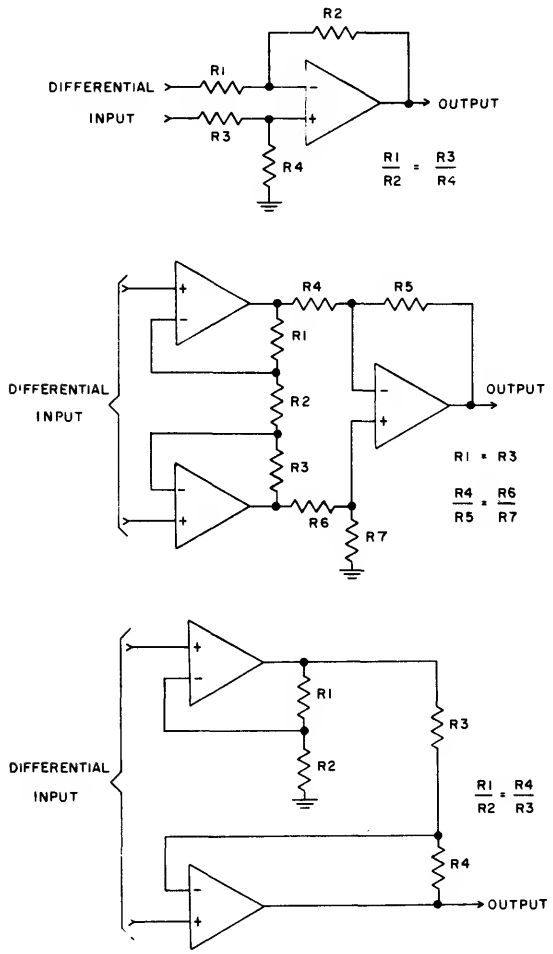

Fig. 10— Some typical differential-to-single-ended conversion circuits.

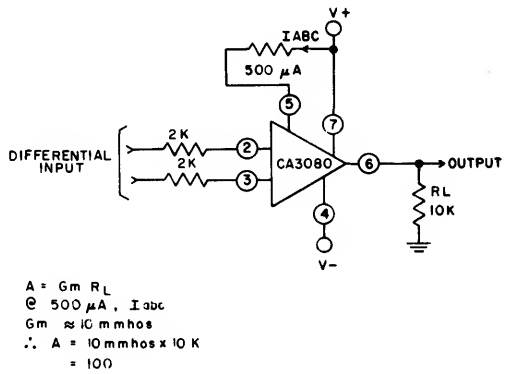

Fig. 11— A differential-to-single-ended conversion circuit without precision resistors.

THE CA3094

The RCA CA3094 offers a unique combination of characteristics that suit it ideally to use as a programmable gain block for audio power amplifiers. It is a transconductance amplifier in which gain and open-loop bandwidth can be controlled between wide limits. The device has a large reserve of output-current capability, and breakdown and power-dissipation ratings sufficiently high to allow it to drive a complementary pair of transistors. For example, a 12-watt power-amplifier stage (8-ohm load) can be driven with peak currents of 35 milliamperes (assuming a minimum output-transistor beta of 50) and supply voltages of ±18 volts. In this application, the RCA CA3094A is operated substantially below its supply-voltage rating of 44-volts max. and its dissipation rating of 1.6-watts max. Also in this application, a high value of open-loop gain suggests the possibility of precise adjustment of frequency-response characteristics by adjustment of impedances in the feedback networks.

Implicit Tone Controls

In addition to low distortion, the large amount of loop gain and flexibility of feedback arrangements available when using the CA3094 make it possible to incorporate the tone controls into the feedback network that surrounds the entire amplifier system. Consider the gain requirements of a phonograph playback system that uses a typical high-quality magnetic cartridge.[3] A desirable system gain would result in from 2 to 5 watts of output at a recorded velocity of 1 cm/s. Magnetic pickups have outputs typically ranging from 4 to 10 millivolts at 5 cm/s. To get the desired output, the total system needs about 72 dB of voltage gain at the reference frequency.

Fig. 12 is a block diagram of a system that uses a passive or "losser"-type of tone-control circuit that is inserted ahead of the gain control. Fig. 13 shows a system in which the tone controls are implicit in the feedback circuits of the power amplifier. Both systems assume the same noise input voltage at the equalizer and main-amplifier inputs. The feedback system shows a small improvement (3.8 dB) in signal-to-noise ratio at maximum gain but a dramatic improvement (20 dB) at the zero gain position. For purposes of comparison, the assumption is made that the tone controls are set "flat" in both cases.

Cost Advantages

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 and 100 dB, respectively. An amplifier with 40 dB of gain and 90 dB of power-supply rejection would require 316 millivolts of power-supply ripple to produce one millivolt of hum at the output. Thus, no further filtering is required other than that given by the energy-storage capacitor at the output of the rectifier system.

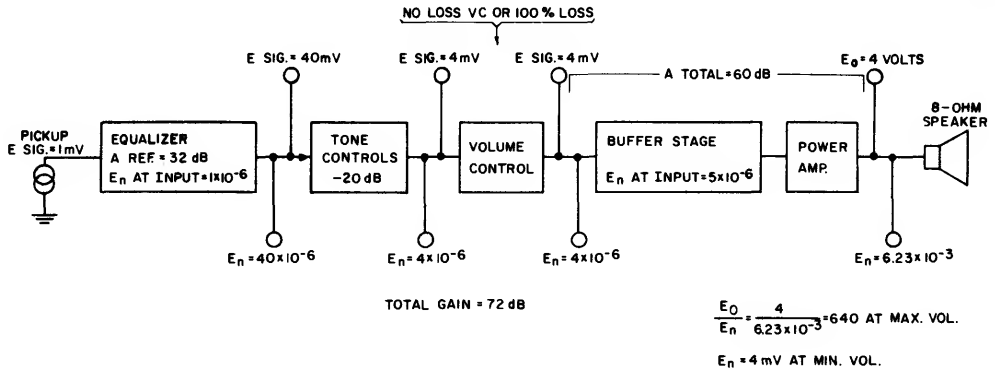

Fig. 12– Block diagram of a system using a "losser"-type tone-control circuit.

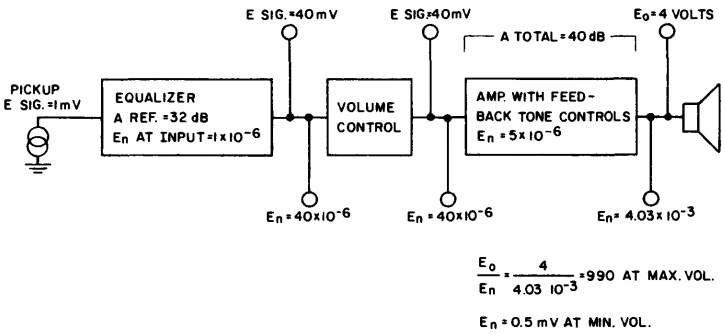

Fig. 13– A system in which tone controls are implicit in the feedback circuit of the power amplifier.

POWER AMPLIFIER USING THE CA3094

A complete power amplifier using the CA3094 and three additional transistors is shown schematically in Fig. 14. The amplifier is shown in a single-channel configuration, but power-supply values are designed to support a minimum of two channels. The output section comprises Q1 and Q2, complementary epitaxial units connected in the familiar "bootstrap" arrangement. Capacitor C3 provides added base drive for Q1 during positive excursions of the output. The circuit can be operated from a single power supply as well as from a split supply as shown in Fig. 15. The changes required for 14.4-volt operation with a 3.2-ohm speaker are also indicated in the diagram.

The amplifier may also be modified to accept input from ceramic phonograph cartridges. For standard inputs (equalizer preamplifiers, tuners, etc.) C1 is 0.047, R1 is 250 kilohms, and R2 and C2 are omitted. For ceramic-cartridge inputs, C1 is 0.0047, R1 is 2.5 megohms, and the jumper across C2 is removed.

Output Biasing

Instead of the usual two-diode arrangement for establishing idling currents in Q1 and Q2, a "V_{be} Multiplier", transistor Q3, is used. This method of biasing establishes the voltage between the base of Q1 and the base of Q2 at a constant multiple of the base-to-emitter voltage of a single transistor while maintaining a low variational impedance between its collector and emitter (see Appendix A). If transistor Q3 is mounted in intimate thermal contact with the output units, the operating temperature of the heat sink forces the V_{be} of Q3 up and down inversely with heat-sink temperature. The voltage bias between the bases of Q1 and Q2 varies inversely with heat-sink temperature and tends to keep the idling current in Q1 and Q2 constant.

A bias arrangement that can be accomplished at lower cost than those already described replaces the V_{be} multiplier with a 1N5391 diode in series with an 8.2-ohm resistor. This arrangement does not provide the degree of bias stability of the V_{be} multiplier, but is adequate for many applications.

Tone-Controls

The tone controls, the essential elements of the feedback system, are located in two sets of parallel paths. The bass network includes R3, R4, R5, C4, and C5. C6 blocks the dc from the feedback network so that the dc gain from input to the feedback takeoff point is unity. The residual dc-output-

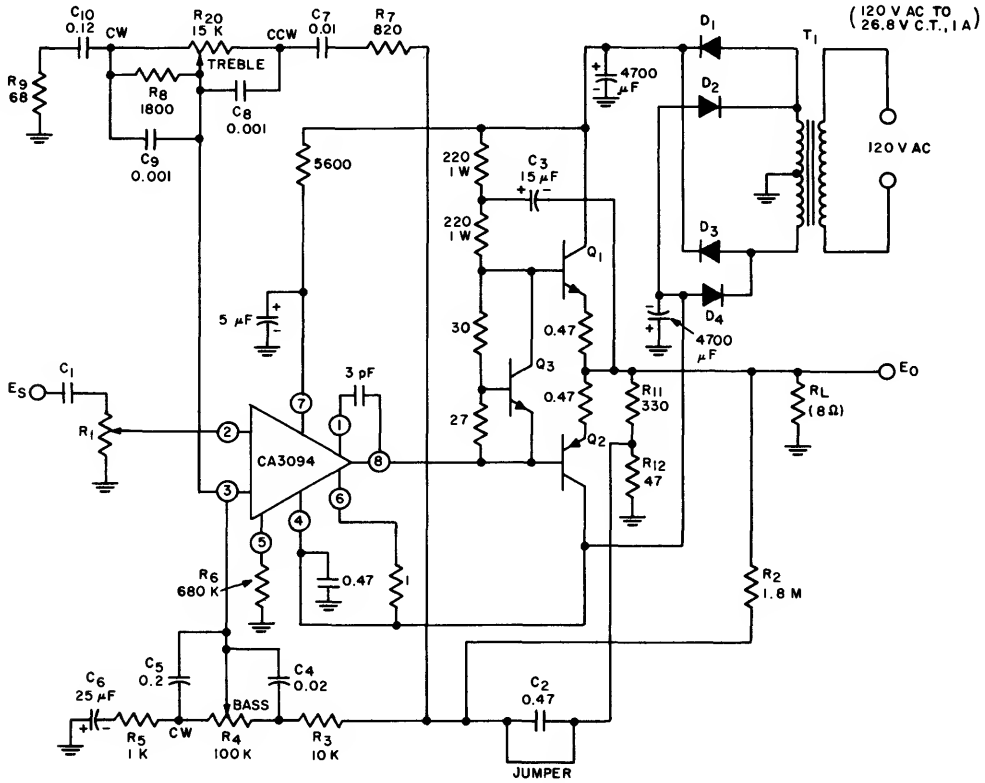

Fig. 14– A complete power amplifier using the CA3094 and three additional transistors.

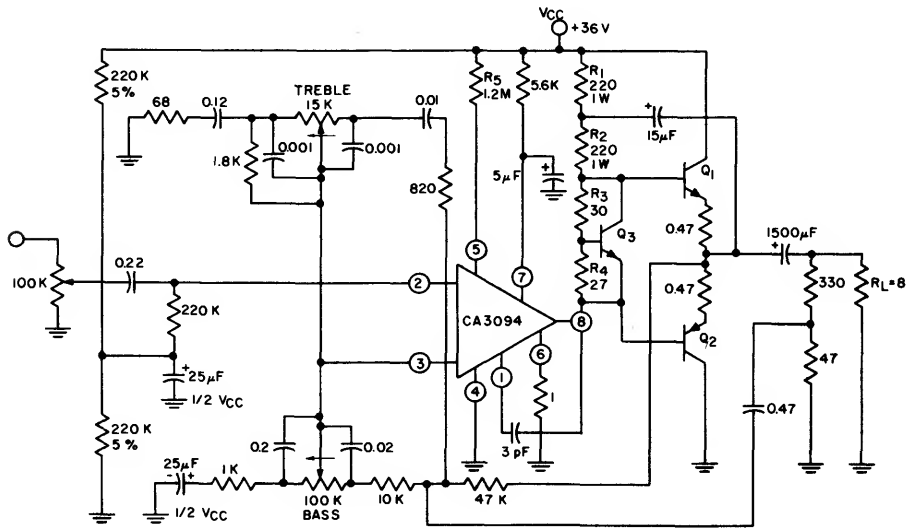

Fig. 15– A power amplifier operated from a single supply.

voltage at the speaker terminals is then $I_{ABC} R_1 \frac{R_{11} + R_{12}}{R_{12}}$ where R_1 is the source resistance. The input bias current is then $\frac{I_{ABC}}{2\beta} = -\frac{(V_{cc} - V_{be})}{2\beta R6}$. The treble network consists of R7, R8, R9, R10, C7, C8, C9, and C10. Resistors R7 and R9 limit the maximum available cut and boost, respectively. The boost limit is useful in curtailing heating due to finite turn-off time in the output units. The limit is also desirable when there are tape recorders nearby. The cut limit aids the stability of the amplifier by cutting the loop gain at higher frequencies where phase shifts become significant.

In cases in which absolute stability under all load conditions is required, it may be necessary to insert a small inductor in the output lead to isolate the circuit from capacitive loads. A 3-microhenry inductor (1 ampere) in parallel with a 22-ohm resistor is adequate. The derivation of circuit constants is shown in Appendix B. Curves of control action versus electrical rotation are also given.

Performance

Fig. 16 is a plot of the measured response of the complete amplifier at the extremes of tone-control rotation. A comparison of Fig. 16 with the computed curves of Fig. B4 (Appendix B) shows good agreement. The total harmonic distortion of the amplifier with an unregulated power supply is shown in Fig. 17; IM distortion is plotted in Fig. 18. Hum and noise are typically 700 microvolts at the output, or 83-dB down.

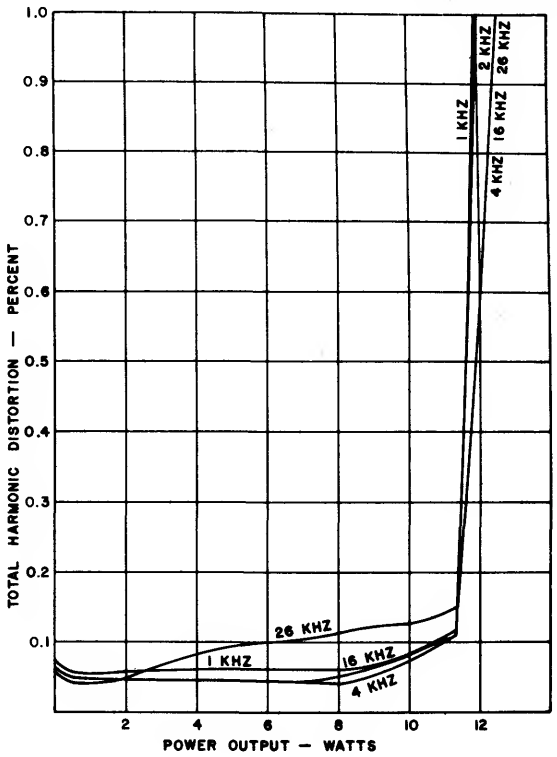

Fig. 17— Total harmonic distortion of the amplifier with an unregulated power supply.

COMPANION RIAA PREAMPLIFIER

Many available preamplifiers are capable of providing the drive for the power amplifier of Fig. 14. Yet the unique characteristics of the amplifier – its power supply, input impedance, and gain – make possible the design of an RIAA

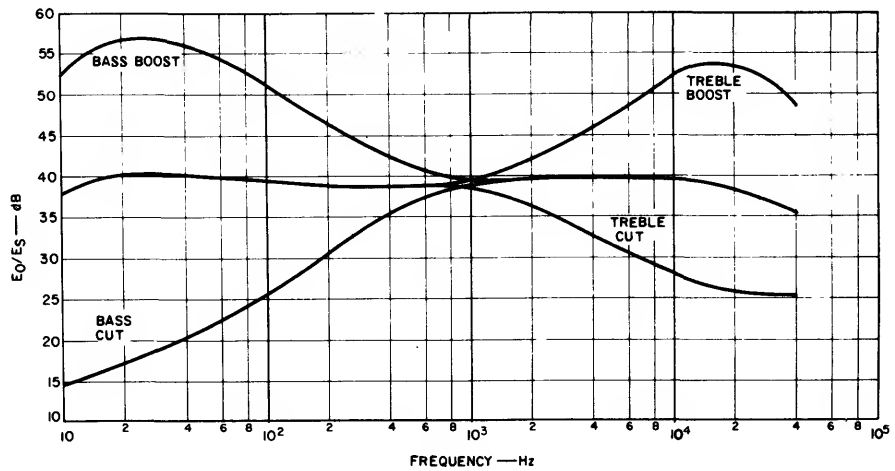

Fig. 16— The measured response of the amplifier at extremes of tone-control rotation.

preamplifier that can exploit these qualities. Since the input impedance of the amplifier is essentially equal to the value of the volume-control resistance (250 kilohms), the preamplifier need not have high output-current capability. Because the gain of the power amplifier is high (40 dB) the preamplifier gain only has to be approximately 30 dB at the reference frequency (1 kHz) to provide optimum system gain.

Fig. 19 shows the schematic diagram of a CA3080 preamplifier. The CA3080, a low-cost OTA, provides sufficient open-loop gain for all the bass boost necessary in RIAA compensation. For example, a gm of 10,000 micromhos with a load resistance of 250 kilohms provides an open-loop gain of 68 dB, thus allowing at least 18 dB of loop gain at the lowest frequency. The CA3080 can be operated from the same power supply as the main amplifier with only minimal decoupling because of the high power-supply rejection inherent in the device circuitry. In addition, the high voltage-swing capability at the output enables the CA3080 preamplifier to handle badly over-modulated (over-cut) recordings without overloading. The accuracy of equalization is within ±1 dB of the RIAA curve, and distortion is virtually unmeasurable by classical methods. Overload occurs at an output of 7.5 volts, which allows for undistorted inputs of up to 186 millivolts (260 millivolts peak).

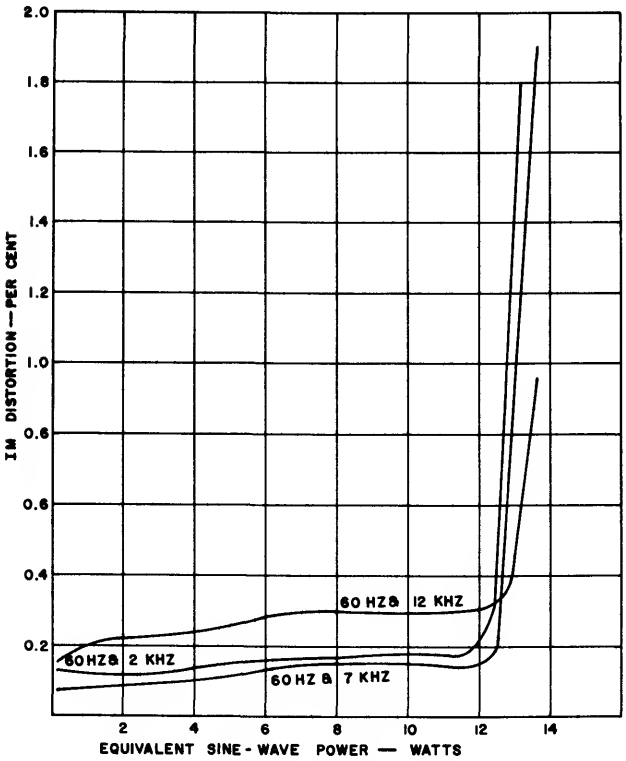

Fig. 18— IM distortion of the amplifier with an unregulated supply.

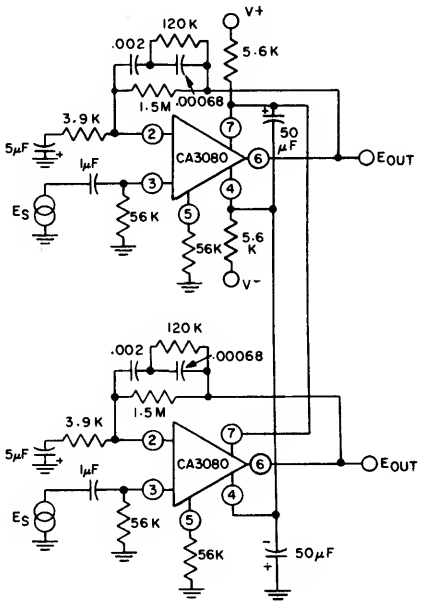

Fig. 19— A CA3080 preamplifier.

APPENDIX A – V_{be} MULTIPLIER

The equivalent circuit for the V_{be} multiplier is shown in Fig. A1. The voltage E_1 is given by:

$$E_1 = \frac{R1I}{\beta+1} + V_{be}\left[1 + \frac{R1}{R2\,(\beta+1)}\right] \qquad (A1)$$

The value of V_{be} is itself dependent on the emitter current of the transistor, which is, in turn, dependent on the input current I since:

$$I_e = I - \frac{V_{be}}{R2} \qquad (A2)$$

The derivative of Eq. A1 with respect to I yields the incremental impedance of the V_{be} multiplier:

$$\frac{dE_1}{dI} = Z = \frac{R1}{\beta+1} + \left[1 + \frac{BR1}{(\beta+1)\,R2}\right]\left[\frac{K_3R2}{R2I_e+K_3}\right] \qquad (A3)$$

where K_3 is a constant of the transistor Q1 and can be found from:

$$V_{be} = K_3 \ln I_e - K_2 \qquad (A4)$$

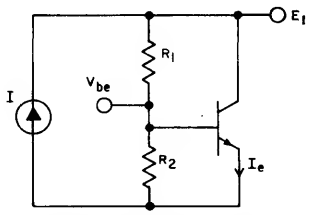

Fig. A1– Equivalent circuit for the V_{be} multiplier.

Eq. A4 is but another form of the diode equation:[4]

$$I_e = I_S\left(e^{\frac{qV_{be}}{KT}} - 1\right) \qquad (A5)$$

Using the values shown in Fig. 14 plus data on the 2N5494 (a typical transistor that could be used in the circuit), the dynamic impedance of the circuit at a total current of 40 milliamperes is found to be 4.6 ohms. In the actual design of the V_{be} multiplier, the value of IR2 must be greater than V_{be} or the transistor will never become forward biased.

APPENDIX B – TONE CONTROLS

Fig. B1 shows four operational-amplifier circuit configurations and the gain expressions for each. The asymptotic low-frequency gain is obtained by letting S approach zero in each case:

Bass Boost: $A_{Low} = \frac{R1+R2+R3}{R2}$

Bass Cut: $A_{Low} = \frac{R1+R2+R3}{R2+R3}$

Treble Boost: $A_{Low} = \frac{C1+C4}{C4}$

Treble Cut: $A_{Low} = \frac{C1+C4}{C4}$

The asymptotic high-frequency gain is obtained by letting S increase without limit in each expression:

Bass boost; $A_{High} = \frac{R1+R2}{R2}$

Bass cut: $A_{High} = \frac{R1+R2}{R2}$

Treble boost: $A_{High} = 1 + C1\left(\frac{C3+C4}{C3C4}\right)$

Treble cut: $A_{High} = \frac{C2 + \frac{C1C4}{C1+C4}}{C1+C2}$

Note that the expressions for high-frequency gain are identical for both bass circuits, while the expressions for low-frequency gain are identical for the treble circuits.

Fig. B2 shows cut and boost bass and treble controls that have the characteristics of the circuits of Fig. B1. The value R_{EFF} in the treble controls of Fig. B1 is derived from the parallel combination of R1 and R2 of Fig. B2 when the control is rotated to its maximum counterclockwise position. When the control is rotated to its maximum clockwise position, the value is equal to R1.

To compute the circuit constants, it is necessary to decide in advance the amounts of boost and cut desired. The gain expressions of Fig. B1 indicate that the slope of the amplitude versus frequency curve in each case will be 6 dB per octave (20 dB per decade). If the ratios of boosted and cut gain are set at 10, i.e.:

Bass circuit: $A_{Low(Boost)} = 10\,A_{Mid}$

$A_{Low\,(Cut)} = \frac{A_{Mid}}{10}$

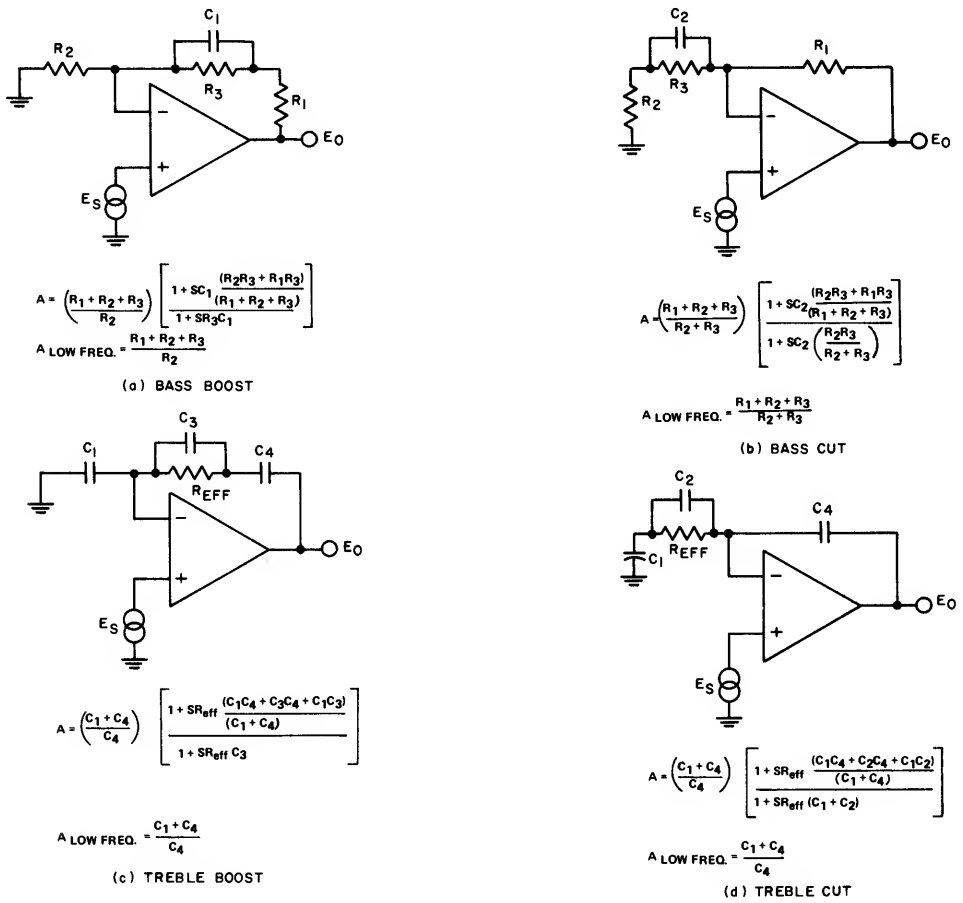

Fig. B1– Four operational-amplifier circuit configurations and the gain expressions for each.

Treble Circuit: $A_{High\ (Boost)} = 10\ A_{Mid}$

$$A_{High(Cut)} = \frac{10\ A_{Mid}}{10}$$

then the following relationships result:

Bass circuit: $R1 = 10\ R2$

$R3 = 99\ R2$

Treble circuit: $C1 = 10\ C4$

$$C2 = \frac{10\ C4}{99}$$

The unaffected portion of the gain (A high for the bass control and A low for the treble control) is 11 in each case.

To make the controls work symmetrically, the low- and high-frequency break points must be equal for both boost and cut.
Thus:

Bass Control: $$\frac{C1\ R3\ (R1+R2)}{R1+R2+R3} = \frac{C2\ R2R3}{R2+R3}$$

and $$C1\ R3 = \frac{C2\ R3\ (R1+R2)}{R1+R2+R3}$$

since $R3 \simeq R2+R3$, $\underline{C2 = 10C1}$

Treble Control: $$R1\ \frac{(C1C4+C3C4+C1C3)}{C1+C4}$$

$$= \frac{R1R2}{R1+R2}\ (C1+C2)$$

and $$R2C3 = \left(\frac{R1R2}{R1+R2}\right)\frac{(C1C4+C2C4+C1C2)}{(C1+C4)}$$

since $C1 \simeq 100C2$, $C2 = C3$ and $C1 = 10C4$, $\underline{R1 = 9R2}$

To make the controls work in the circuit of Fig. 14, breaks were set at 1000 Hz:

for the base control $$0.1C1R3 = \frac{1}{2\pi \times 1000}$$

and for the treble control $$R1C3 = \frac{1}{2\pi \times 1000}$$

Response and Control Rotation

In a practical design, it is desirable to make "flat" response correspond to the 50-percent rotation position of the control, and to have an aural sensation of smooth variation of response on either side of the mechanical center. It is easy to show that the "flat" position of the bass control occurs when the wiper arm is advanced to 91-percent of its total resistance. The amplitude response of the treble control is, however, never completely "flat"; a computer was used to generate response curves as controls were varied.

Fig. B3 is a plot of the response with bass and treble tone controls combined at various settings of both controls. The values shown are the practical ones used in the actual design. Fig. B4 shows the information of Fig. B3 replotted as a function of electrical rotation. The ideal taper for each control would be the complement of the 100-Hz plot for the bass control and the 10-kHz response for the treble control. The mechanical center should occur at the crossover point in each case.

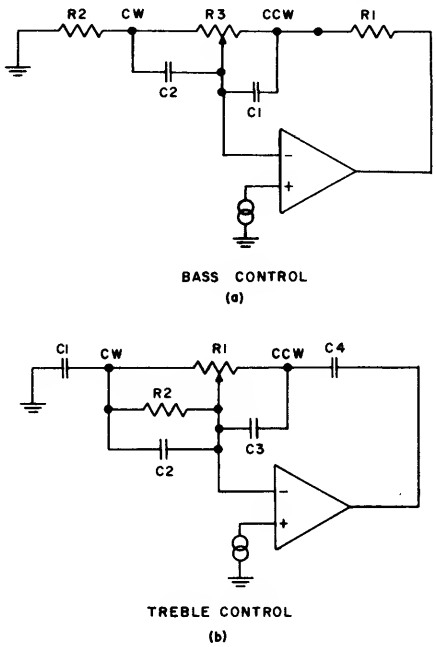

Fig. B2— Cut and boost bass and treble controls that have the characteristics of the circuits of Fig. B1.

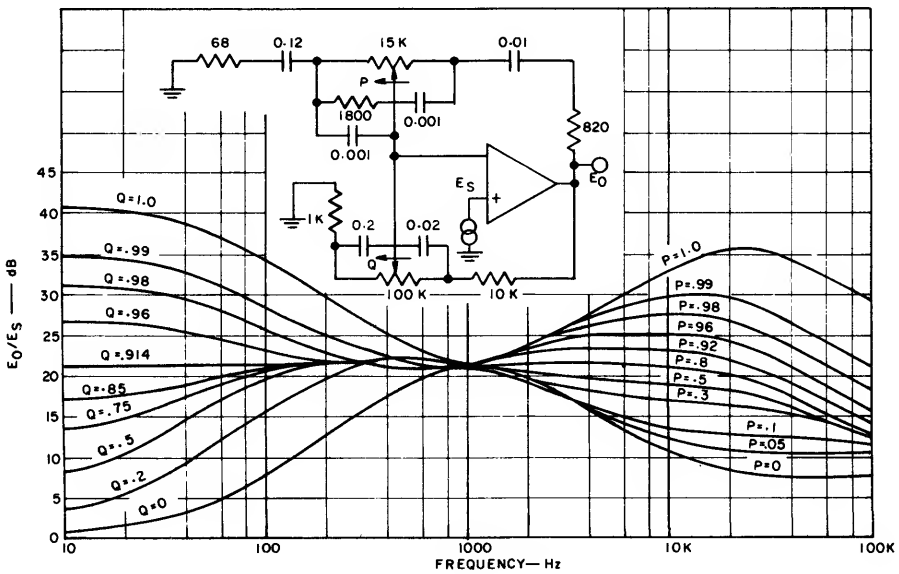

Fig. B3— A plot of the response of the circuit of Fig. 14 with bass and treble tone controls combined at various settings of both controls.

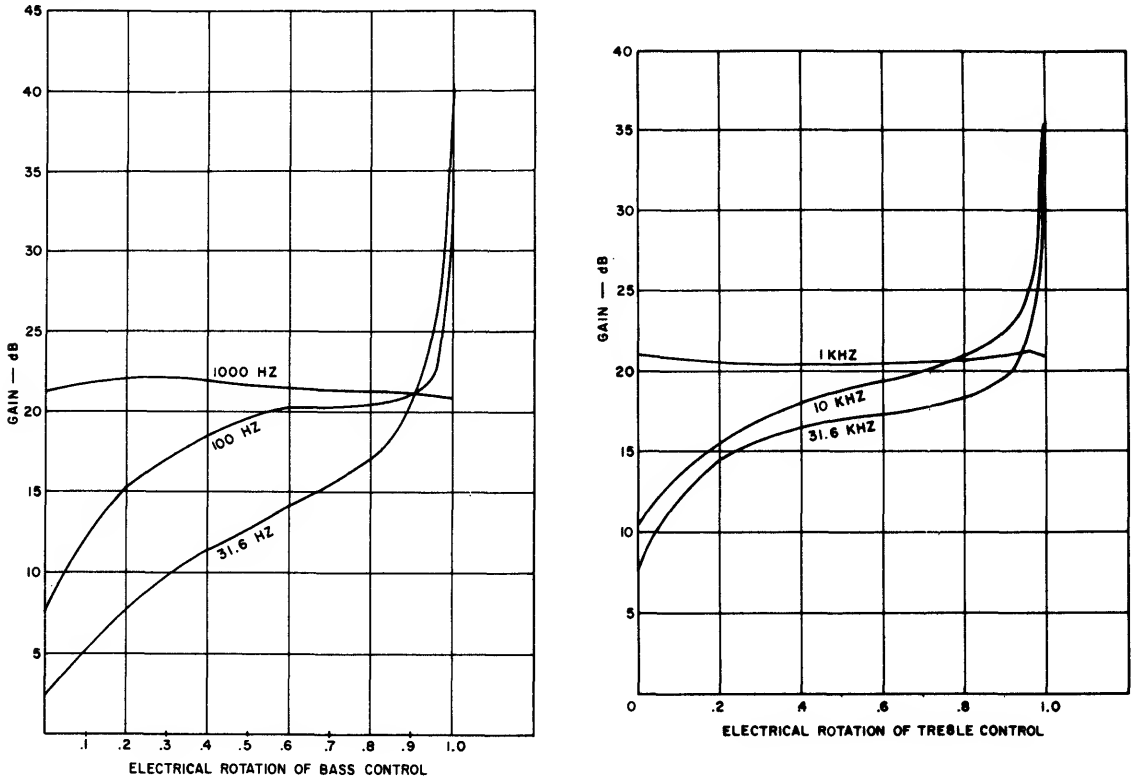

Fig. B4— The information of Fig. B3 plotted as a function of electrical rotation.

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1. "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers," H. A. Wittlinger, RCA Application Note ICAN-6668
2. "A New Wide-band Amplifier Technique," B. Gilbert, IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December, 1968.
3. "Trackability," James A. Kogar, *Audio*, December 1966
4. *RCA Linear Integrated Circuits Manual*, RCA Technical Series IC-42

*RCA publications available through RCA Solid State Division, Box 3200, Somerville, N.J., 08876.

Applications of the CA3085-Series Monolithic IC Voltage Regulators

by A.C.N. Sheng and L.R. Avery

The RCA-CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100 milliamperes over the temperature range from -55°C to +125°C. They are supplied in 8-lead TO-5 type packages; their characteristics and ratings are given in RCA Data File No. 491. The following tabulation shows some key characteristics and salient differences between devices in the CA3085 Series.

Type	$V_{IN}(V_I)$ Range V	$V_{OUT}(V_O)$ Range V	Max. $I_{OUT}(I_O)$ mA	Max. Load Regulation % V_O
CA3085	7.5-30	1.8-26	12*	0.1
CA3085A	7.5-40	1.7-36	100	0.15
CA3085B	7.5-50	1.7-46	100	0.15

*This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

In addition to these differences, the range of some specified performance parameters is more tightly controlled in the CA3085B than in the CA3085A, and more in the CA3085A than in the CA3085.

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting, A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

Circuit Description

The block diagram of the CA3085-series circuits is shown in Fig. 1. Fundamentally, the circuit consists of a frequency-compensated error-amplifier which compares an internally generated reference voltage with a sample of the output voltage and controls a series-pass amplifier to regulate the output. The starting circuit assures stable latch-in of the voltage-reference circuitry. The current-limiting portion of the circuit is an optional feature that protects the IC in the event of overload.

Terminal 5 provides a source of stable reference voltage for auxiliary use; a current of about 250 microamperes can be supplied to an external circuit without significantly disturbing reference-voltage stability. If necessary, filtering of the inherent noise of the reference-voltage circuit can be accomplished by connecting a suitable bypass capacitor between terminals 5 and 4.

Terminal 6 (the "inverting input" in accordance with operational-amplifier terminology) is the input through which a sample of the regulated output voltage is applied.

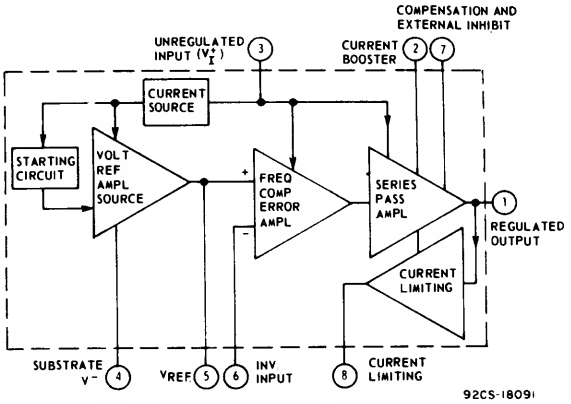


Fig. 1 - Block diagram of CA3085 series.

The collector of the series-pass output transistor is brought out separately at terminal 2 ("current booster") to provide base drive for an external p-n-p transistor; this approach is one method of regulating currents greater than 100 milliamperes.

Because the voltage regulator is essentially an operational amplifier having considerable feedback, frequency compensation is necessary in some circuits to prevent oscillations. Terminal 7 is provided for external frequency compensation; it can also be used to "inhibit" (strobe, squelch, pulse, key) the operation of the series-pass amplifier.

Brief Description of CA3085 Schematic Diagram

The schematic diagram of the CA3085-series circuits is shown in Fig. 2. The left-hand section includes the starting circuit, the voltage-reference circuit, and the constant-current circuit. The center section is basically an elementary operational amplifier which serves as the voltage-error amplifier. It controls the series-pass Darlington pair (Q13, Q14) shown in the right-hand section. When controlled by an appropriate external sensing network, transistor Q15 serves to provide protective current-limiting characteristics by diverting base drive from the series-pass circuit. For operation at the highest current levels, terminals 2 and 3 are tied together to eliminate the voltage drop which would otherwise be developed across resistor R5.

Voltage-Reference Circuits

The basic voltage-reference element used in the CA3085 is zener diode D3. It provides a nominal reference voltage of 5.5 volts and exhibits a positive temperature coefficient of approximately 2.5 millivolts/°C. If this reference voltage

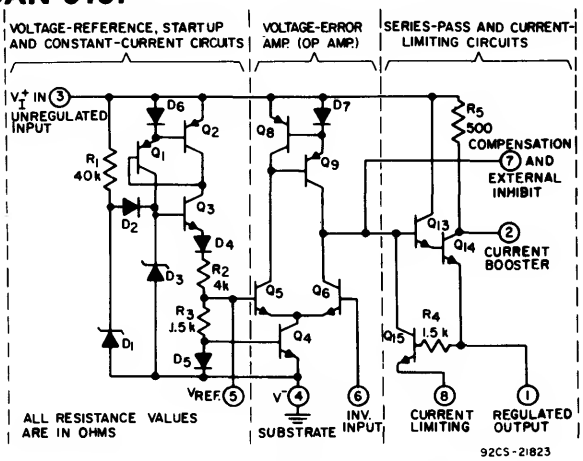


Fig. 2 - Schematic diagram of CA3085 series.

were used directly in conjunction with the error-amplifier (Q5, Q6, etc.), the IC would exhibit two major undesirable characteristics: (1) its performance with temperature variations would be poor, and (2) its use as a regulator would be restricted to circuits in which the minimum regulated output voltages are in excess of 5.5 volts. Consequently, it is necessary to provide means of compensating for the positive temperature coefficient of D3 and at the same time provide for obtaining a stable source of lower reference voltage. Both temperature compensation and the reduction of the reference voltage are accomplished by means of the series divider network consisting of the base-emitter junction of Q3, diode D4, resistors R2 and R3, and diode 5.

The voltage developed across D3 drives the divider network and a voltage of approximately 4 volts is developed between the cathode of D4 and the cathode of D5 (terminal 4). The current through this divider network is held nearly constant with temperature because of the combined temperature coefficients of the zener diode (D3), Q3 base-emitter junction, D4, D5, and the resistors R2 and R3. This constant current through the diode D5 and the resistor R3 produces a voltage drop between terminals 4 and 5 that results in the reference voltage (≈ 1.6 volts) having an effective temperature coefficient of about 0.0035 per cent/°C.

The reference diode D3 receives a current of approximately 620 microamperes from a constant-current circuit consisting of Q3 and the current-mirror* D6, Q1, and Q2. Current to start-up the constant-current source initially is provided by auxiliary zener diode D1 and R1. Diode D2 blocks current from the R1-D1 source after latch-in of the constant-current source establishes a stable reference potential, and thereby prevents modulation of the reference voltage by ripple voltage on the unregulated input voltage.

Voltage-Error Amplifier

Transistors Q5 and Q6 comprise the basic differential amplifier that is used as a voltage-error amplifier to compare the stable reference voltage applied at the base of Q5 with a sample of the regulator output voltage applied at terminal 6. The D5-Q4 combination is a current-mirror which maintains essentially constant-current flow to Q5 and Q6 despite variations in the unregulated input voltage. The Q8, Q9, and D7 network provides a "mirrored" active collector load for Q5 and Q6 and also provides a variable single-ended drive to the Q13 and Q14 series-pass transistors in accordance with the difference signal developed between the bases of Q5 and Q6. The open-loop gain of the error-amplifier is greater than 1000.

Series-Pass and Current-Limiting Circuits

In the normal mode of operation, or in the current-boost mode when terminals 2 and 3 are tied together, the Darlington pair Q13-Q14 performs the basic series-pass regulating function between the unregulated input voltage and the regulated output voltage at terminal 1. In the current-limiting mode transistor Q15 provides current-limiting to protect the CA3085 and/or limit the load current. To provide current-limiting protection, a resistor (e.g., 5 ohms) is connected between terminals 1 and 8; terminal 8 becomes the source of regulated output voltage. As the voltage drop across this resistor increases, base drive is supplied to transistor Q15 so that it becomes increasingly conductive and diverts base drive from the Q13-Q14 pass transistor to reduce output current accordingly. Resistor R4 is provided to protect Q15 against overdrive by limiting its base current under transient and load-short conditions.

Because the CA3085 regulator is essentially an op-amp having considerable feedback, frequency compensation may be required to prevent oscillations. Stability must also be maintained despite line and load transients, even during operation into reactive loads (e.g., filter capacitors). Provisions are included in the CA3085 so that a small-value capacitor may be connected between terminals 6 and 7 to compensate the regulator, when necessary, by "rolling-off" the amplifier frequency-response. Terminal 7 is also used to externally "inhibit" operation of the CA3085 by diverting base current supplied to Q13-Q14, thereby permitting the use of keying, strobing, programming, and/or auxiliary overload-protection circuits.

APPLICATIONS

A Simple Voltage Regulator

Fig. 3 shows the schematic diagram of a simple regulated power supply using the CA3085. The ac supply voltage is stepped down by T1, full-wave rectified by the diode bridge circuit, and smoothed by the large electrolytic capacitor C1 to provide unregulated dc to the CA3085 regulator circuit. Frequency compensation of the error-amplifier is provided by capacitor C2. Capacitor C3 bypasses residual noise in the reference-voltage source, and thus decreases the incremental noise-voltage in the regulator circuit output.

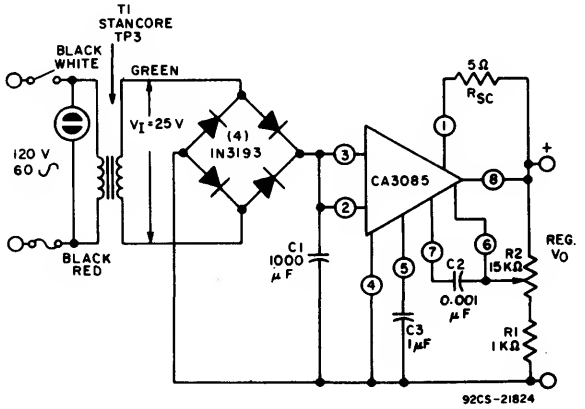


Fig. 3 - Basic power supply.

*The fundamentals of current-mirror theory are reviewed in the Appendix of Application Note ICAN-6668.

Because the open-loop gain of the error-amplifier is very high (greater than 1000), the output voltage may be directly calculated from the following expression:

$$V_O = \frac{(R2 + R1)}{R1} V_{ref} \quad (1)$$

In the circuit shown in Fig. 3, the output voltage can be adjusted from 1.8 volts to 20 volts by varying R2. The maximum output current is determined by R_{SC}; load-regulation characteristics for varlous values of R_{SC} are shown in Fig. 4.

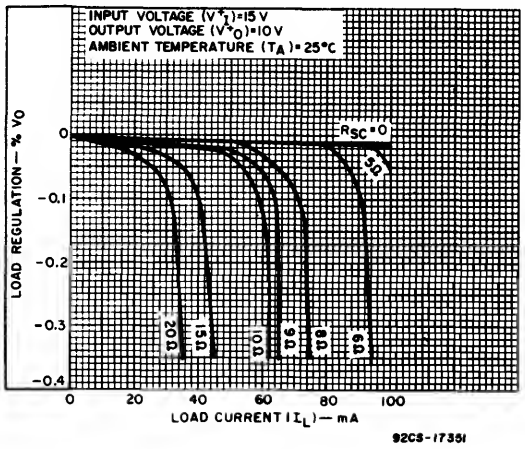


Fig. 4 - Load regulation characteristics for circuit of Fig. 3.

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Fig. 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in V_I) or by using a dropping resistor between the rectifier and the CA3085 regulator. Fig. 5 gives data on dissipation limitation (V_I-V_O vs. I_O) for CA3085-series circuits.

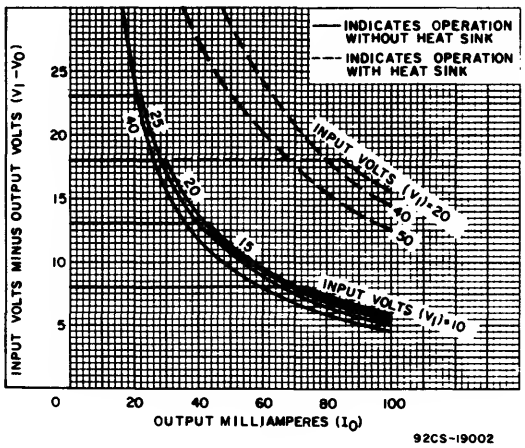


Fig. 5 - Dissipation limitation (V_I-V_O vs. I_O) for CA3085 series circuits.

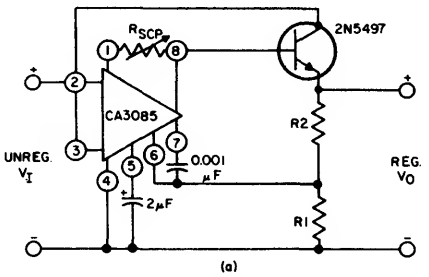
The short-circuit current is determined as follows:

$$I_{sc} \frac{V_{BE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \quad (2)$$

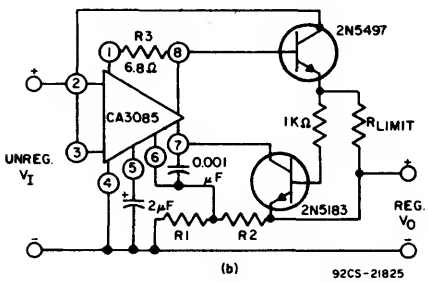
The line- and load-regulation characteristics for the circuit shown in Fig. 3 are approximately 0.05 per cent of the output voltage.

High-Current Voltage Regulator

When regulated voltages at currents greater than 100 milliamperes are required, the CA3085 can be used in conjunction with an external n-p-n pass-transistor as shown in the circuits of Fig. 6. In these circuits the output current available from the regulator is increased in accordance with the h_{FE} of the external n-p-n pass-transistor. Output currents up to 8 amperes can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8 amperes are to be regulated.



(a) with simplified short-circuit protection



(b) with auxiliary short-circuit protection

Fig. 6 - High-current voltage regulator using n-p-n pass transistor.

A simplifled method of short-circuit protection is used in connection with the circuit of Fig. 6(a). The variable resistor R_{SCP} serves two purposes: (1) it can be adjusted to optimize the base drive requirements (h_{FE}) of the particular 2N5497 transistor being used, and (2) in the event of a short-circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop across R_{SCP}. As this voltage-drop increases the short-circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short-circuit protection depends on the value of R_{SCP}, i.e., design compromise is required In choosing the value of R_{SCP} to provide the desired base drive for the 2N5497 whlle maintaining the desired short-circuit protection. Fig. 6(b)

shows an alternate circuit in which an additional transistor (2N2102) and two resistors have been added as an auxiliary short-circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor R_{limit} now controls the short-circuit output current because, in the event of a short-circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N2102 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N2102 diverts base drive from the Darlington output stage of the CA3085 (see Fig. 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3-ampere load-current variation; line regulation is typically 0.025 per cent/volt change in input voltage.

Voltage Regulator with Low V_I-V_O Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4 volts between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Fig. 7 can deliver an output current in the order of 2 amperes with a V_I-V_O difference of only one volt.

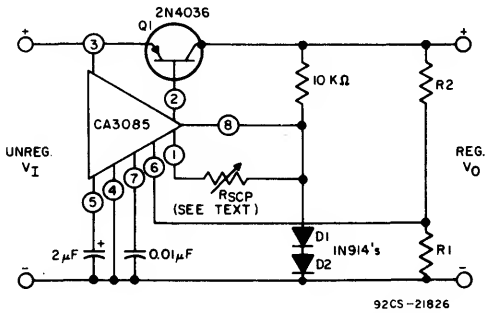


Fig. 7 - Voltage regulator for low V_I-V_O difference.

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Fig. 2) in the CA3085 is returned to the negative supply rail through an external resistor (R_{SCP}) and two series-connected diodes (D1, D2). These forward-biased diodes maintain Q6 in the CA3085 within linear-mode operation. The choice of resistors R1 and R2 is made in accordance with Eq. (1). Adequate frequency compensation for this circuit is provided by the 0.01-microfarad capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

Fig. 8, which shows the output impedance of the circuit of Fig. 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1 kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

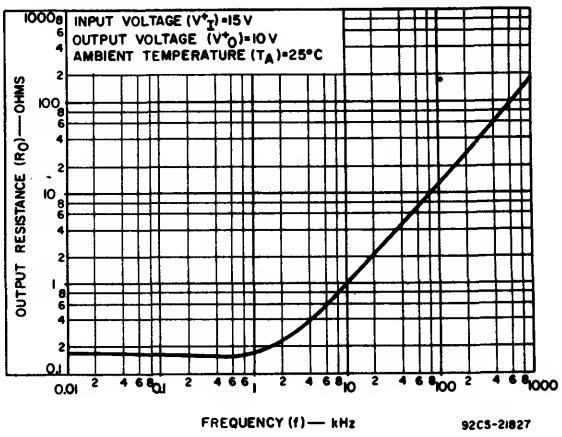


Fig. 8 - Output resistance vs. frequency for circuit of Fig. 7.

High-Voltage Regulator

Fig. 9 shows a circuit that uses the CA3085 as a voltage-reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085-series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated. Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085 regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Eq. (1).

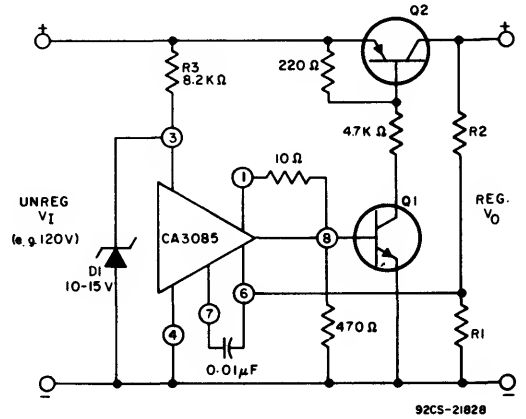


Fig. 9 - High-voltage regulator.

Negative-Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Fig. 10. Transistor Q3 is the series-pass transistor. It should be noted that the CA3085 is effectively connected across the load-side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass-transistor Q3 by means of Q1.

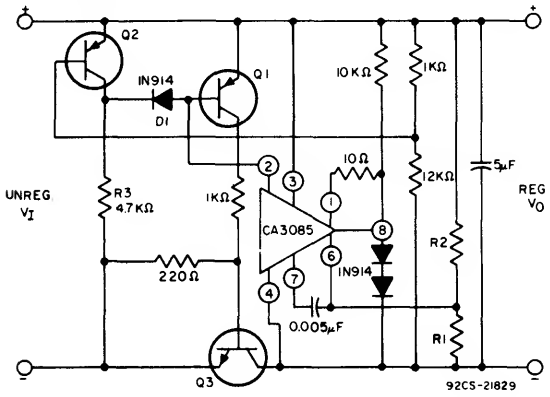


Fig. 10 - Negative-voltage regulator.

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides base drive for the pass-transistor Q3. By this means operating potential for the CA3085 is developed between the collector of Q3 (terminal 4 of the CA3085) and the positive supply-rail (terminal 3 of the CA3085). When the output voltage has risen sufficiently to maintain operation of the CA3085 (approx. 7.5 volts), transistor Q2 is driven into conduction by the base drive supplied from the 1 kilohm-12 kilohm voltage divider. As Q2 becomes conductive, it diverts the base drive being supplied to Q1 through the R3-D1 path, and diode D1 ceases to conduct. Under these conditions, base-current drive to Q1 through terminal 2 of the CA3085 regulates the base drive to Q3. Values of R1 and R2 are determined in accordance with Eq. (1).

The circuit shown in Fig. 11 is similar to that of Fig. 10,

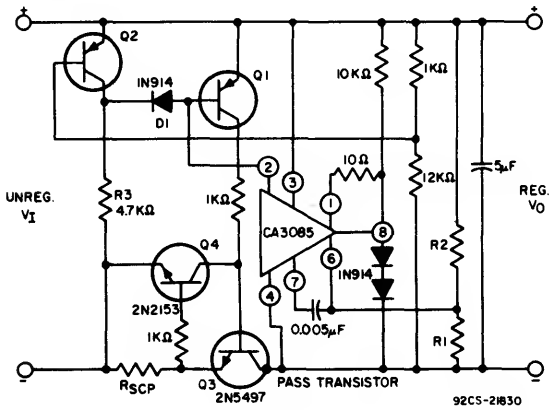


Fig. 11 - Negative-voltage regulator with constant-current limiting circuit.

except for the addition of a constant-current limiting circuit consisting of transistor Q4, a 1-kilohm resistor, and resistor R_{SCP}. When the load current increases above a particular design value, the corresponding increase in the voltage drop across resistor R_{SCP} provides additional base drive to transistor Q4. Thus, as transistor Q4 becomes increasingly conductive, its collector current diverts sufficient base drive from Q3 to limit the current in the pass transistor feeding the regulated load. With the types of transistors shown in Figs. 10 and 11, maximum currents in the order of 5 amperes can be regulated.

High-Output-Current Voltage Regulator With "Foldback" Current-Limiting (Also known as "Switch-Back" Current-Limiting)

In high-current voltage regulators employing constant-current limiting (e.g., Figs. 6 and 7), it is possible to develop excessive dissipation in the series-pass transistor when a short-circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Fig. 12. In this circuit, terminal 8 of the CA3085 senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected between the emitter of the pass-transistor (Q3) and ground. The current-foldback trip-point is established by the value of resistor R_{SC}.

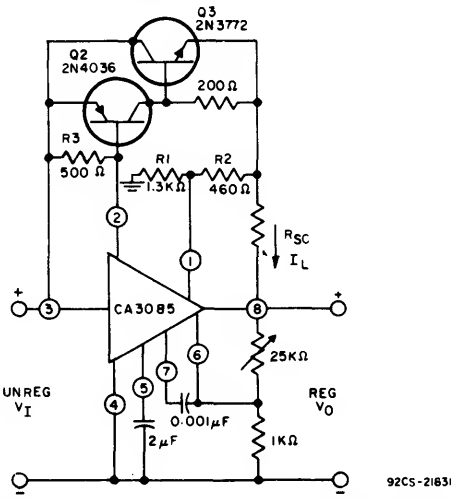


Fig. 12 - High-output-current voltage regulator with "foldback" current limiting.

The protective tripping action is accomplished by forward-biasing Q15 in the CA3085 (see Fig. 2). Conditions for tripping-circuit operation are defined by the following expressions:

$$V_{BE(Q15)} = (\text{voltage at terminal 1}) - (\text{output voltage})$$

$$= \left[(V_O + I_L R_{SC})\frac{R1}{R1+R2}\right] - V_O \qquad (3)$$

$$\text{If } \frac{R1}{R1+R2} = K, \text{ then}$$

$$V_{BE(Q15)} = (V_O + I_L R_{SC})K - V_O = KV_O + KI_L R_{SC} - V_O$$

and therefore

$$R_{SC} = \frac{V_O + V_{BE(Q15)} - KV_O}{KI_L} \qquad (4)$$

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q14 in the CA3085, establishing terminal 1 at one V_{BE}-drop [≅ 0.7 V] above ground and Q15 in a partially conducting state. The current through Q14 necessary to establish this one-V_{BE} condition is the sum of currents flowing to ground through R1 and [R2 + R_{SC}]. Normally R_{SC} is much smaller than R2 and can be ignored; therefore, the equivalent resistance R_{eq} to ground is the parallel combination of R1 and R2.

The Q14 current is then given by:

$$I_{Q14} = \frac{V_{BE(Q15)}}{R_{eq}} = \frac{V_{BE(Q15)}}{\frac{R1R2}{R1+R2}} = \frac{0.7\,[1.3+0.46]}{1.3 \times 0.46} \text{ 2.06 milli-amperes}$$

This current provides a voltage between terminals 2 and 3 as follows:

$$V_{2-3} = I_{Q14} \times 250 \text{ ohms} = 2.06 \times 10^{-3} \times 250 = 0.515 \text{ volt}$$

The effective resistance between terminals 2 and 3 is 250 ohms because the external 500-ohm resistor R3 is in parallel with the internal 500-ohm resistor R5. It should be understood that the V_{2-3} potential of 0.515 volt is insufficient to maintain the external p-n-p transistor Q2 in conduction, and, therefore, Q3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Fig. 13 shows the foldback characteristic typical of the circuit of Fig. 12.

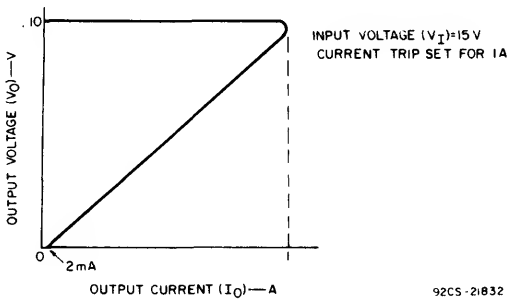


Fig. 13 - Typical "foldback" current-limiting characteristic for circuit of Fig. 12.

An alternative method of providing "foldback" current-limiting is shown in Fig. 14. The operation of this circuit is similar to that of Fig. 12 except that the foldback-control transistor Q2 is external to the CA3085 to permit added flexibility in protection-circuit design.

Under low load conditions Q2 is effectively reverse-biased by a small amount, depending upon the values of R3 and R4. As the load current increases the voltage drop across R_{trip} increases, thereby raising the voltage at the base of Q1, and Q2 starts to conduct. As Q2 becomes increasingly conductive it diverts base current from transistors Q13 and Q14 in the CA3085, and thus reduces base drive to the external pass-transistor Q1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, I_{trip}, is calculated as follows:

$V_{BE(Q1)}$ = voltage at terminal 8 - V_O (assuming a low value for R_{trip})

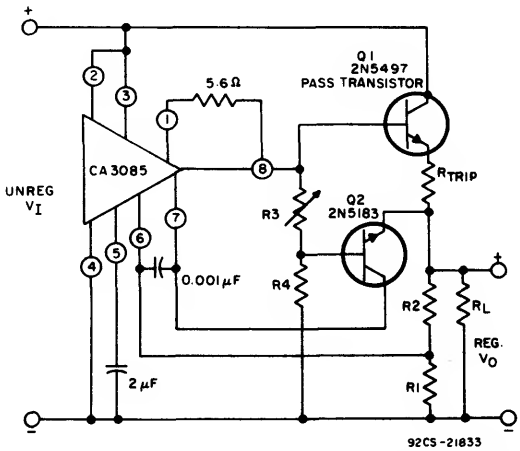


Fig. 14 - High-output-current voltage regulator using auxiliary transistor to provide "foldback" current limiting.

$$V_{BE(Q2)} = \text{voltage at terminal 8} \left(\frac{R4}{R3+R4}\right) - V_O$$

$$= \left[V_O + I_L R_{trip} + V_{BE(Q1)}\right]\left[\frac{R4}{R3+R4}\right] - V_O$$

if $K = \frac{R4}{R3+R4}$, then the trip current is given by:

$$I_{trip} = \frac{V_{BE(Q2)} - K[V_O+V_{BE(Q1)}] + V_O}{KR_{trip}} \quad (7)$$

In the circuit in Fig. 12 the load current goes to zero when a short circuit occurs. In the circuit of Fig. 14 the load current is significantly reduced but does not go to zero. The value for I_{SC} is computed as follows:

$$V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 = V_{BE(Q1)} + I_{SC}R_{trip}$$

$$I_{SC} = \frac{V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 - V_{BE(Q1)}}{R_{trip}} \quad (8)$$

Fig. 15 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

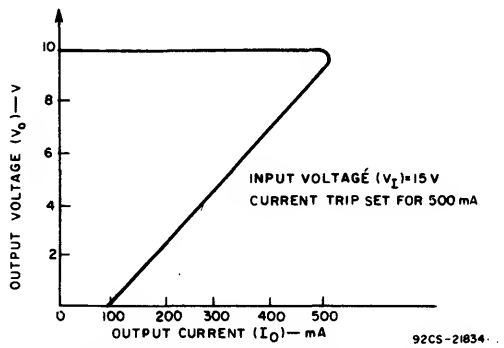


Fig. 15 - Typical foldback current-limiting characteristic for circuit of Fig. 14.

High-Voltage Regulator Employing Current "Snap-Back" Protection

In high-voltage regulators (e.g., see Fig. 9), "foldback" current-limiting cannot be used safely because the high voltage across the pass transistor can cause second breakdown despite the reduction in current flow. To adequately protect the pass transistor in this type of high-voltage regulator, the so-called "snap-back" method of current limiting can be employed to reduce the current to zero in a few microseconds, and thus prevent second-breakdown destruction of the device.

The circuit diagram of a high-voltage regulator employing current "snap-back" protection is shown in Fig. 16. The basic regulator circuit is similar to that shown in Fig. 9. The additional circuitry in the circuit of Fig. 16 quickly interrupts base drive to the pass transistor in event of load fault. The point of current-trip is established as follows:

$$I_{trip} = \frac{V_{BE(Q1)}}{R_{SC}} \qquad (9)$$

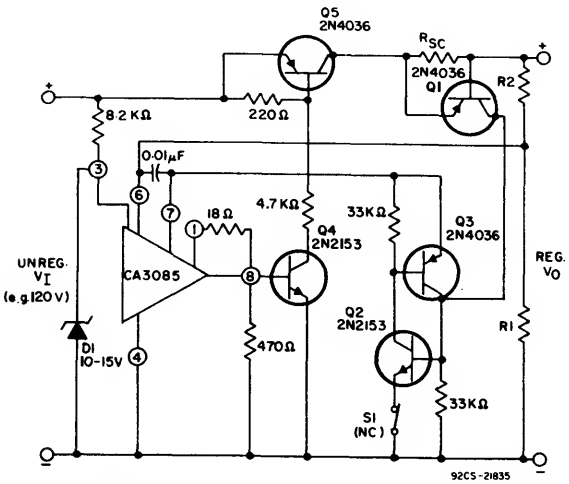


Fig. 16 - High-voltage regulator incorporating current "snap-back" protection.

Thus, when a sufficient voltage drop is developed across R_{SC}, transistor Q1 becomes conductive and current flows into the base of Q2 so that it also becomes conductive. Transistor Q3, in turn, is driven into conduction, thereby latching the Q2-Q3 combination (basic SCR action) so that it diverts (through terminal 7) base drive from the output stage (Q13, Q14) in the CA3085. By this means, base drive is diverted from Q4 and the pass transistor Q5. To restore regulator operation, normally closed switch S1 is momentarily opened and unlatches Q2-Q3.

Switching Regulator

When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Fig. 17(a). Transistor Q1 acts as a keyed switch and operates in either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reverse-biased and current in the inductance L1 increases in accordance with the following relationship:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt \qquad (10)$$

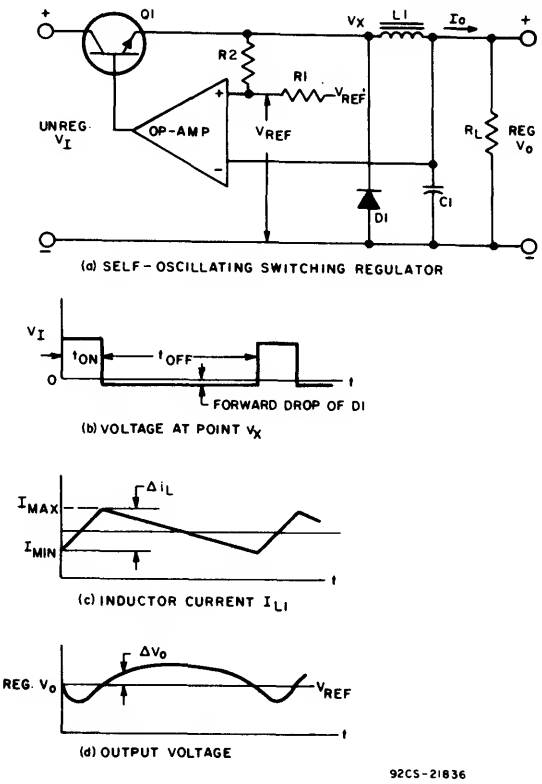


Fig. 17 - Switching regulator and associated waveforms.

Where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage V_{ref}. At this point the op-amp removes base drive to Q1 and the unregulated input voltage V_I is "switched off". The energy stored in the inductor L1 now causes the voltage at V_x to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load R_L. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and V_O decreases. When V_O falls slightly below the value of V_{ref}, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about V_{ref} with an amplitude determined by R1 and R2. Actually, the value of V_{ref} varies from being slightly more positive than V_{ref}' when Q1 is conducting, to being slightly more negative than V_{ref}' when D1 is conducting. The voltage and current waveforms are shown in Fig. 17(b), (c), and (d).

Design Example: The following specifications are used in decomputations for a switching regulator:

V_I = 30 V, V_O = 5 V, I_o = 500 mA,
switching frequency = 20 kHz,
output ripple = 100 mV.

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq. 10, as follows:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt = \left(\frac{V_I - V_O}{L1}\right) t_{on} \qquad (11)$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O+V_{D1})\, t_{off}}{L1} \qquad (12)$$

From Eq. 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad (13)$$

If i_{max} is 1.3 I_L, then during t_{on} the current in the inductor (i_L) will be 0.5 A x 1.3 = 0.65 A; therefore, Δi_L = 0.15 A.

Substitution in Eq. 13 yields

$$L_1 = \frac{(30 - 5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} = 1.4 \text{ mH} \qquad (14)$$

Current discharge from the capacitor C1 is given by:

$$i_c = C \frac{dv}{dt} \qquad (15)$$

Thus, $\Delta i_c = C \frac{\Delta v}{\Delta t}$, or $C = \frac{\Delta i_c\, \Delta t}{\Delta v}$

Since $i_c = i_L$ and $\Delta t = t_{off}$, then

$$C = \frac{\Delta i_L\, t_{off}}{\Delta v}$$

Substitution for the value of i_L from Eq. 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{off}}{\Delta v} \qquad (16)$$

The total period $T = t_{off} + t_{on}$, and $T = \frac{1}{f}$. Therefore,

$$t_{off} = \frac{1}{f} - t_{on} \qquad (17)$$

For optimum efficiency t_{on} should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right) \frac{1}{f} \qquad (18)$$

Substitution for t_{on} in Eq. 18 yields

$$t_{off} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right)\frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \qquad (19)$$

Substitution for t_{off} in Eq. 16 yields

$$C = \frac{\frac{(V_I - V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v} \qquad (20)$$

Substitution of numerical values in Eq. 20 produces the following value for C:

$$C = \frac{\frac{30 - 5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^3} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^3} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\ \mu F$$

A switching-regulator circuit using the CA3085 is shown in Fig. 18. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

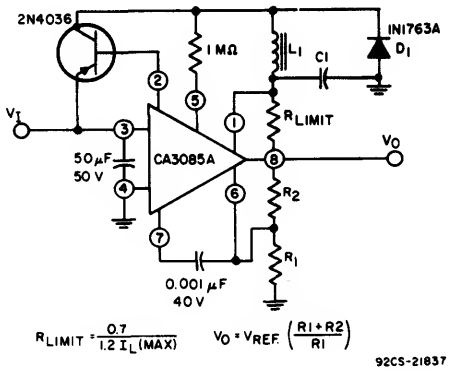
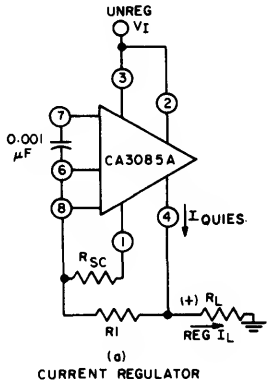


Fig. 18 - Typical switching regulator circuit.

Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100 milliamperes is shown in Fig. 19(a). The regulated load current is



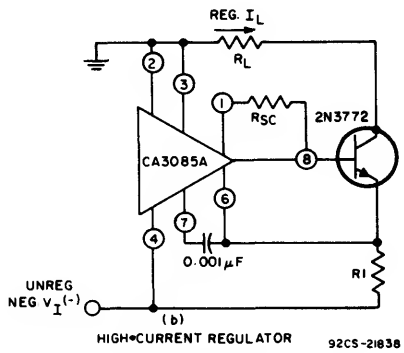


Fig. 19 - Constant current regulators.

controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4. The actual

regulated current, reg I_L, is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{quiescent} + I_{R1}$$

Fig. 19(b) shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3 amperes. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

$$\text{Reg } I_L = \frac{V_{ref}}{R1}$$

With this regulator currents between 1 milliampere and 3 amperes can be programmed directly. At currents below 1 milliampere inaccuracies may occur as a result of leakage in the external transistor.

A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A* is shown in Fig. 20. The CA3094A is basically an op amp capable of supplying 100 milliamperes of output current.

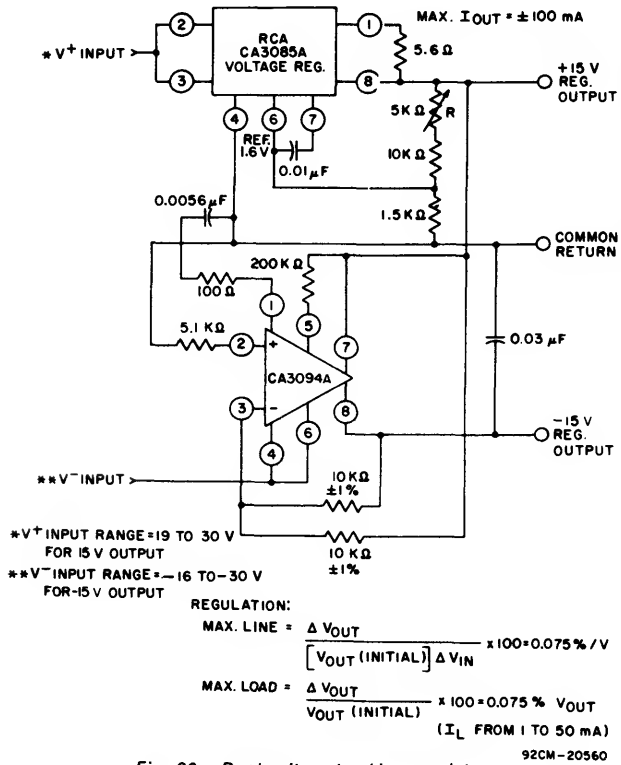


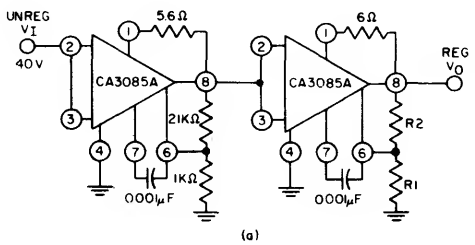
Fig. 20 - Dual-voltage tracking regulator.

The positive output voltage is regulated by a CA3085 operating in a configuration essentially similar to that described in connection with Fig. 3. Resistor R is used as a vernier adjustment of output voltage. The negative output voltage is regulated by the CA3094A, which is "slaved" to the regulated positive voltage supplied by the CA3085. It should be noted that the non-inverting input of the CA3094A and the negative supply terminal of the CA3085 are connected to a common ground reference. The "slaving" potential for the CA3094A is derived from an accurate 1:1 voltage-divider network comprised of two 10-kilohm resistors connected between the +15-volt and -15-volt output terminals. The junction of these two resistors is connected to the inverting input of the CA3094A. The voltage at this junction is compared with the voltage at the non-inverting input, and the CA3094A then automatically adjusts the output current at the negative terminal to maintain a negative regulated output voltage essentially equal to the regulated positive output voltage. Typical performance data for this circuit are shown in Fig. 20.

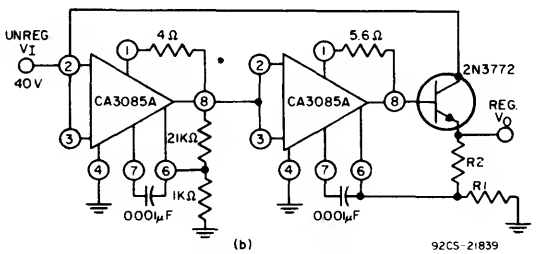
The basic circuit of Fig. 20 can be modified to regulate dissimilar positive and negative voltages (e.g., +15 V, -5 V) by appropriate selection of resistor ratios in the voltage-divider network discussed previously. As an example, to provide tracking of the +15 V and -5 V regulated voltages with the circuit of Fig. 20, it is only necessary to replace the 10-kilohm resistor connected between terminals 3 and 8 of the CA3094A with a 3.3-kilohm resistor.

Regulators With High Ripple Rejection

When the reference-voltage source in the CA3085 is adequately filtered, the typical ripple rejection provided by the circuit is 56 dB. It is possible to achieve higher ripple-rejection performance by cascading two stages of the CA3085, as shown in Fig. 21. The voltage-regulator circuit in Fig. 21(a) provides 90 dB of ripple rejection. The output voltage is adjustable over the range from 1.8 to 30 volts by appropriate adjustment of resistors R1 and R2. Higher regulated output currents up to 1 ampere can be obtained with this circuit by adding an external n-p-n transistor as shown in Fig. 21(b).



(a) voltage regulator with high ripple rejection



(b) high-current voltage regulator with high ripple rejection

Fig. 21 - Regulators with high ripple rejection.

*Specifications for the CA3094A appear in RCA Data File No. 598 and application information is presented in ICAN-6048.

The CA3085 As A Power Source For Sensors

Certain types of sensor applications require a regulated power source. Additionally, low-impedance sensors can consume significant power. An example of a circuit with these requirements, in which a CA3085 provides regulated power for a low-impedance sensor and the CA3059* zero-voltage switch, is shown in Fig. 22. Terminal 12 on the CA3059 provides the ac trigger-signal which actuates the zero-voltage switch synchronously with the power line to control the load-switching triac.

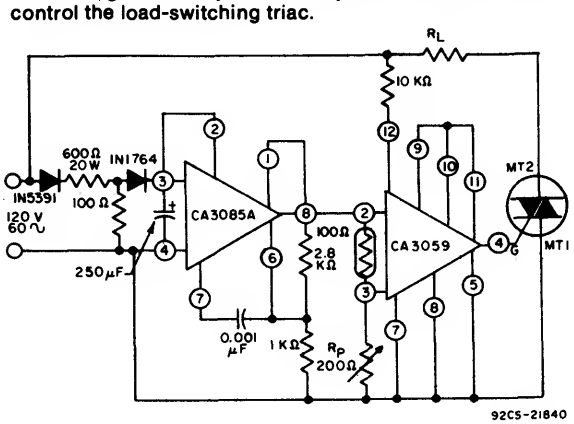


Fig. 22 - Voltage regulator for sensor and zero-voltage switch.

The CA3085 As A General-Purpose Amplifier

As described above, the CA3085 series regulators contain a high-gain linear amplifier having a current-output capability up to 100 milliamperes. The premium type (CA3085B) can operate at supply voltages up to 50 volts. When equipped with an appropriate radiator or heat sink, the TO-5 package of these devices can dissipate up to 1.6 watts at 55° C. A very stable internal voltage-reference source is used to bias the high-gain amplifier and/or provide an external voltage-reference despite extreme temperature or supply-voltage variations. These factors, plus economics, prompt consideration of this circuit for general-purpose uses, such as amplifiers, relay controls, signal-lamp controls, and thyristor firing.

As an example, Fig. 23 shows the application of the CA3085 in a general-purpose amplifier. Under the conditions shown, the circuit has a typical gain of 70 dB with a flat response to at least 100 kHz without the RC network connected between terminals 6 and 7. The RC network is useful as a tone control or to "roll-off" the amplifier response for other reasons. Current limiting is not used in this circuit. The network connected between terminals 8 and 6 provides both dc and ac feedback. This circuit is also applicable for directly driving an external discrete n-p-n power transistor.

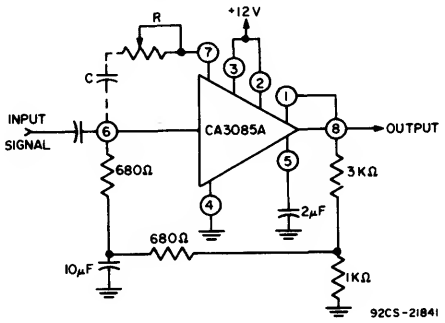


Fig. 23 - General-purpose amplifier using CA3085A.

*Technical specifications for RCA integrated-circuit zero-voltage switches CA3058, CA3059, and CA3079 appear in File No. 490; related application information is given in ICAN-6182.

Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

by A.C.N. Sheng, G.J. Granieri, J. Yellin, and T. McNulty

RCA-CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. These integrated-circuit switches operate from an ac input voltage of 24, 120, 208 to 230, or 277 volts at 50, 60, or 400 Hz.

The CA3059 and CA3079 are supplied in a 14-terminal dual-in-line plastic package. The CA3058 is supplied in a 14-terminal dual-in-line ceramic package. The electrical and physical characteristics of each type are detailed in RCA Data Bulletin File No. 490.

RCA zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply-voltage cycle. Consequently, transient load-current surges and radio-frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on-state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of ac power-control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient-free temperature control in self-cleaning ovens, to control gun-muzzle temperature in low-temperature environments, to provide sequential switching of heating elements in warm-air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different ac power-control functions.

FUNCTIONAL DESCRIPTION

RCA zero-voltage switches are multistage circuits that employ a diode limiter, a zero-crossing (threshold) detector, an on-off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The dc operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3058 and CA3059 also feature an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated-circuit zero-voltage switches are electrically identical.

Over-all Circuit Operation

Fig. 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on-off type of ac power-control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

(1) Limiter-Power Supply – Permits operation directly from an ac line.

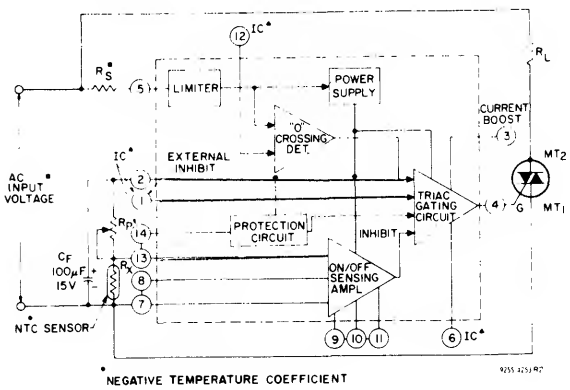
(2) Differential On/Off Sensing Amplifier – Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.

(3) Zero-Crossing Detector – Synchronizes the output pulses of the circuit at the time when the ac cycle is at a zero-voltage point and thereby eliminates radio-frequency inteference (RFI) when used with resistive loads.

(4) Triac Gating Circuit – Provides high-current pulses to the gate of the power-controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (shown in Fig. 1):

(1) A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Fig. 1 – Functional block diagrams of the zero-voltage switches CA3058, CA3059, and CA3079.

(2) Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.

(3) High-power dc-comparator operation is provided by overriding the action of the zero-crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Fig. 2 shows the detailed circuit diagram for the integrated-circuit zero-voltage switches. (The diagrams shown in Figs. 1 and 2 are representative of all three RCA zero-voltage switches, i.e., the CA3058, CA3059, and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)

The limiter stage of the zero-voltage switch clips the incoming ac line voltage to approximately ±8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, C_F, that comprise the dc power supply. The power supply provides approximately 6 volts as the V_{CC} supply to the other stages of the zero-voltage switch. The on-off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "0", and, for the CA3058 and CA3059, the output of the fail-safe circuit must be "high." Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

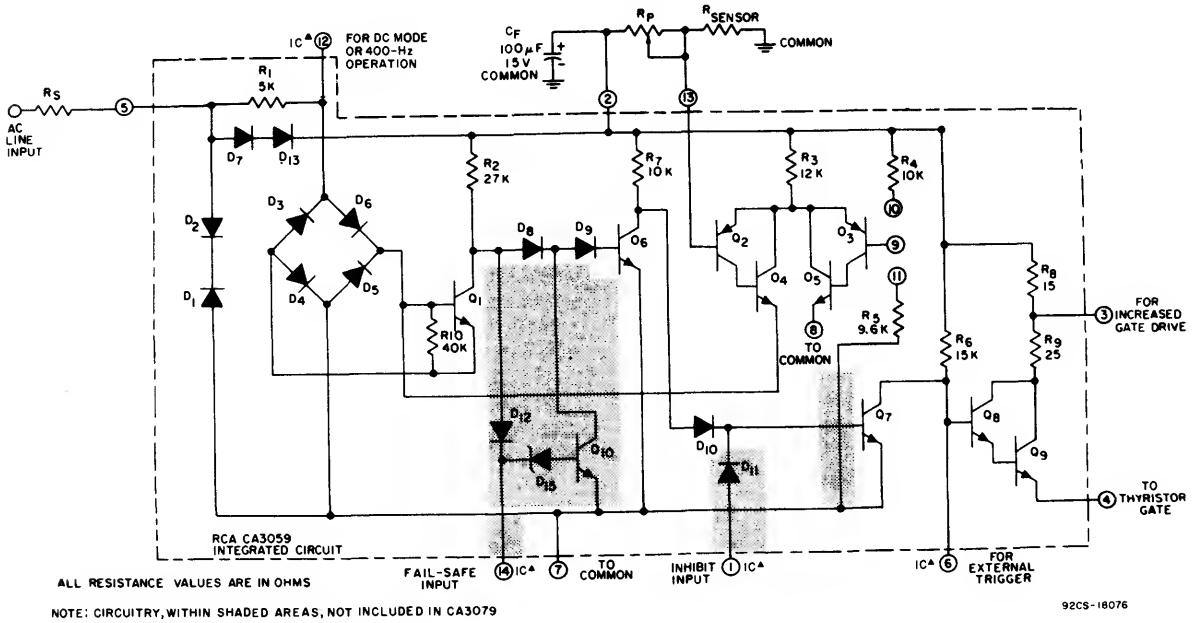


Fig. 2 – Schematic diagram of zero-voltage switches CA3058, CA3059, and CA3079.

Thyristor Triggering Circuits

The diodes D_1 and D_2 in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ±8 volts; the diodes D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor, C_F.

The output pulses used to trigger the power-switching thyristor are actually developed by the zero-crossing detector and the thyristor gating circuit. The zero-crossing detector consists of diodes D_3 through D_6, transistor Q_1, and the associated resistors shown in Fig. 2. Transistors Q_1 and Q_6 through Q_9 and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the ac input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero-crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors Q_8 and Q_9 are conducting, transistor Q_7 is off, and transistor Q_6 is on. Any action that turns on transistor Q_7 removes the drive from transistor Q_8 and thereby turns off the thyristor. Transistor Q_7 may be turned on directly by application of a minimum of ±1.2 volts at 10 microamperes to the external-inhibit input, terminal 1. (If a voltage of more than 1.5 volts is available, an external resistance must be added in series with terminal 1 to limit the current to 1 milliampere.) Diode D_{10} isolates the base of transistor Q_7 from other signals when an external-inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher-priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Transistor Q_7 may also be activated by turning off transistor Q_6 to allow current flow from the power supply through resistor R_7 and diode D_{10} into the base of Q_7. Transistor Q_6 is normally maintained in conduction by current that flows into its base through resistor R_2 and diodes D_8 and D_9 when transistor Q_1 is off.

Transistor Q_1 is a portion of the zero-crossing detector. When the voltage at terminal 5 is greater than +3 volts, current can flow through resistor R_1, diode D_6, the base-to-emitter junction of transistor Q_1, and diode D_4 to terminal 7 to turn on Q_1. This action inhibits the delivery of a gate-drive output signal at terminal 4. For negative voltages at terminal 5 that have magnitudes greater than 3 volts, the current flows through diode D_5, the emitter-to-base junction of transistor Q_1, diode D_3, and resistor R_1, and again turns on transistor Q_1. Transistor Q_1 is off only when the voltage at terminal 5 is less than the threshold voltage of approximately ±2 volts. When the integrated-circuit zero-voltage switch is connected as shown in Fig. 1, therefore, the output is a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Fig. 3. In some applications, however,

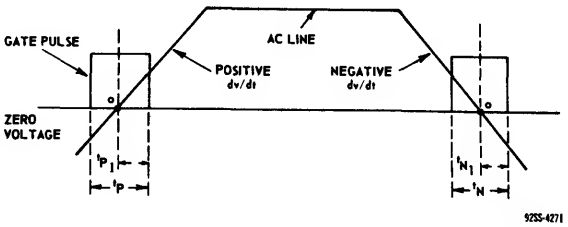


Fig. 3 – Waveform showing output-pulse duration of the zero-voltage switch.

particularly those that use either slightly inductive or low-power loads, the thyristor load current does not reach the latching-current value* by the end of this pulse. An external capacitor C_X connected between terminal 5 and 7, as shown in Fig. 4, can be used to delay the pulse to accommodate such loads. The amount of pulse stretching and delay is shown in Figs. 5(a) and 5(b).

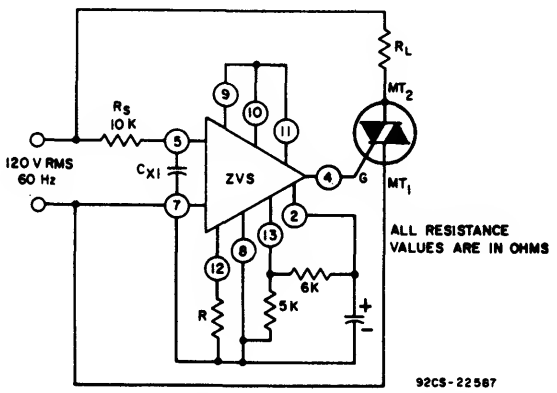


Fig. 4 – Use of a capacitor between terminals 5 and 7 to delay the output pulse of the zero-voltage switch.

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero-crossing detector. In this mode, transistor Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be taken to avoid overloading of the internal power supply in this mode. A sensitive-gate thyristor should be used, and a resistor should be placed between terminal 4 and the gate of the thyristor to limit the current, as pointed out later under **Special Application Considerations.**

Fig. 6 indicates the timing relationship between the line voltage and the zero-voltage- switch output pulses. At 60 Hz, the pulse is typically 100 microseconds wide; at 400 Hz, the pulse width is typically 12 microseconds. In the basic circuit shown, when the dc logic signal is "high", the output is disabled; when it is "low", the gate pulses are enabled.

* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the off to the on state and the gate signal is removed.

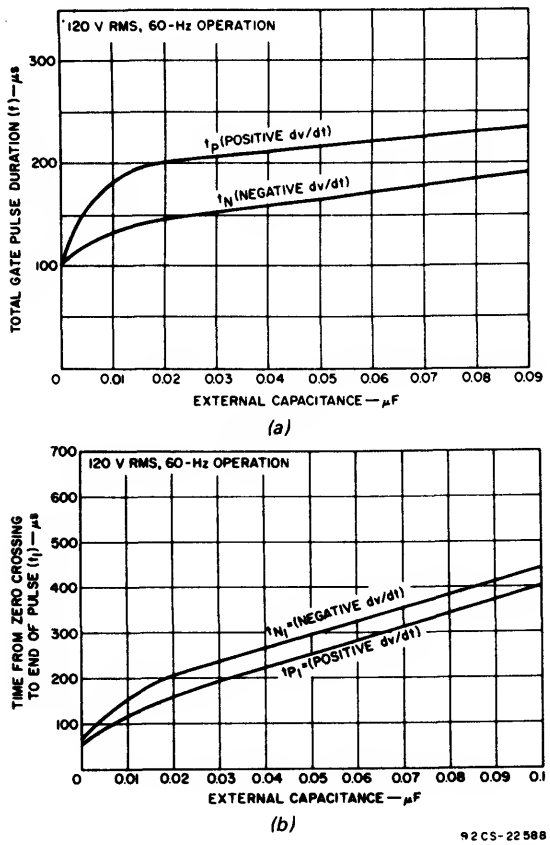


Fig. 5 – Curves showing effect of external capacitance on (a) the total output-pulse duration, and (b) the time from zero crossing to the end of the pulse.

On-Off Sensing Amplifier

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2, Q_3, Q_4, and Q_5 (shown in Fig. 2) makes the zero-voltage switch a flexible power-control circuit. The transistor pairs Q_2-Q_4 and Q_3-Q_5 form a high-beta composite p-n-p transistors in which the emitters of transistors Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with resistor R_3 acting as a constant-current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of transistors Q_2 and Q_3. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of the transistor pair Q_2-Q_4. When terminal 13 is negative with respect to terminal 9, most of the current flows through that path, and none in terminal 8. When current flows in the transistor pair Q_2-Q_4, the path is from the supply through R_3, through the transistor pair Q_2-Q_4, through the base-emitter junction of transistor Q_1, and finally through the diode D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9, transistor Q_1 is on, and the output is inhibited.

In the circuit shown in Fig. 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, and the potentiometer R_p and the negative-temperature-coefficient (NTC) sensor form the other side. At low temperatures, the high resistance of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half-cycle, and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached, and V_{13} approaches V_9. At this point, the transistor pair Q_2-Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of the potentiometer R_p. For cooling service, either the positions of R_p and the sensor may be reversed or terminals 9 and 13 may be interchanged.

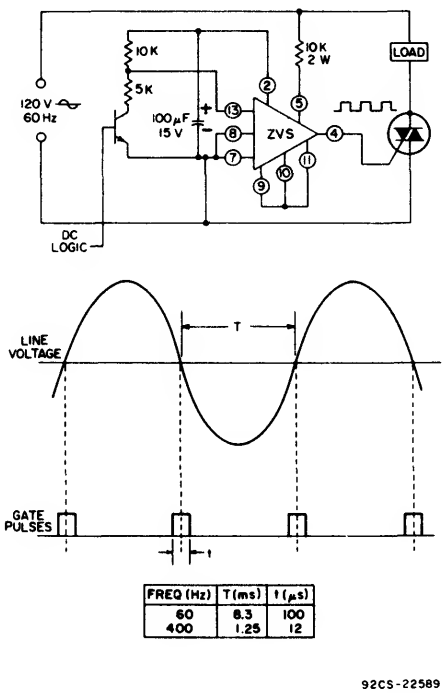


Fig. 6 – Timing relationship between the output pulses of the RCA zero-voltage switch and the ac line voltage.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1 megohm at balance without introduction of substantial error (i.e., greater than 5 per cent). The error may be reduced if the internal bridge elements, resistors R_4 and R_5, are not used, but are replaced with resistances which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply. Operation of the zero-voltage switch with low-impedance sensors is discussed later under **Special Application Considerations**. The voltage applied to terminal 13 must be greater than 1.8 volts at all times to assure proper operation.

Protection Circuit

A special feature of the CA3058 and CA3059 zero-voltage switches is the inclusion of an interlock type of circuit. This circuit removes power from the load by interrupting the thyristor gate drive if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, effective protection-circuit operation is dependent upon the following conditions:

(1) The circuit configuration of Fig. 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.

(2) The value of potentiometer R_P and of the sensor resistance must be between 2000 ohms and 0.1 megohm.

(3) The ratio of sensor resistance and R_P must be greater than 0.33 and less than 3.0 for all normal conditions. (If either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit.)

The protective feature may be applied to other systems when operation of the circuit is understood. The protection circuit consists of diodes D_{12} and D_{15} and transistor Q_{10}. Diode D_{12} activates the protection circuit if the sensor shown in Fig. 1 shorts or its resistance drops too low in value, as follows: Transistor Q_6 is on during an output pulse so that the junction of diodes D_8 and D_{12} is 3 diode drops (approximately 2 volts) above terminal 7. As long as V_{14} is more positive or only 0.15 volt negative with respect to that point, diode D_{12} does not conduct, and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of diode D_8 can have a potential of only 1.6 to 1.7 volts, and current does not flow through diodes D_8 and D_9 and transistor Q_6. The thyristor then turns off.

The actual threshold is approximately 1.2 volts at room temperature, but decreases 4 millivolts per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6 volts, the zener diode D_{15} breaks down and turns on transistor Q_{10}, which then turns off transistor Q_6 and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown voltage of diode D_{15}, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated-circuit zero-voltage switch.

SPECIAL APPLICATION CONSIDERATIONS

As pointed out previously, the RCA integrated-circuit zero-voltage switches (CA3058, CA3059, and CA3079) are exceptionally versatile units that can be adapted for use in a wide-variety of power-control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

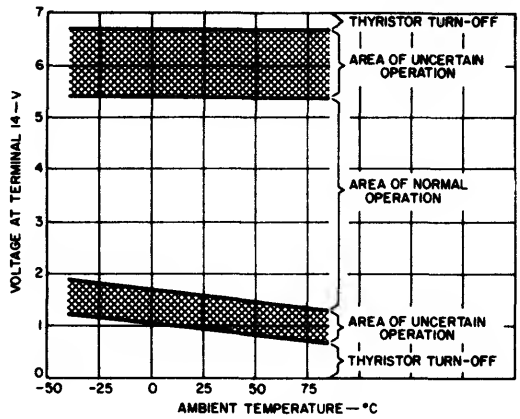


Fig. 7 – Operating regions for built-in protection circuits of a typical zero-voltage switch.

Operating-Power Options

Power to the zero-voltage switch may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 8. When the zero-voltage switch is operated directly from the ac line, a dropping resistor R_S of 5,000 to 10,000 ohms must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal dc power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Fig. 9. The chart shown in Fig. 1 indicates the value and dissipation rating of the resistor R_S for ac line voltages of 24, 120, 208 to 230, and 277 volts.

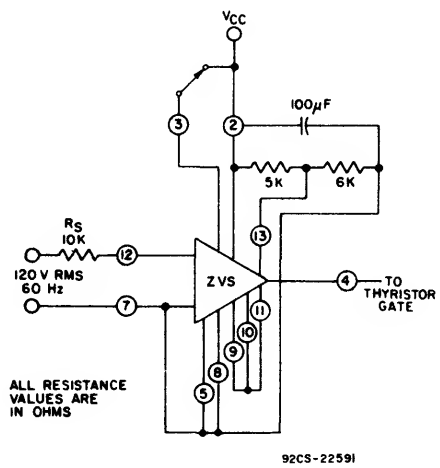


Fig. 8 – Operation of the zero-voltage switch from an external dc power supply connected between terminals 2 and 7.

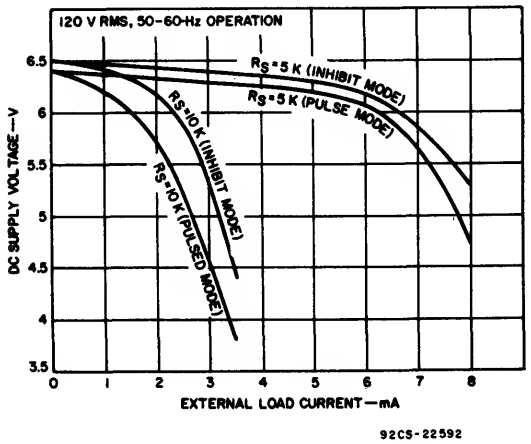


Fig. 9 – DC supply voltage as a function of external load current for several values of dropping resistance R_S.

Half-Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the ac power results in a half-cycling phenomenon at the control point. Fig. 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage crossing every half-cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainity region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the ac line voltage.

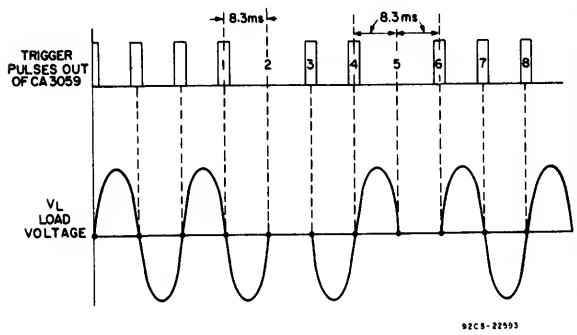


Fig. 10 – Half-cycling phenomenon in the zero-voltage switch.

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive-going cycle, but insufficient to trigger the device on the negative-going cycle of the triac supply voltage. This effect introduces a half-cycling phenomenon, i.e., the triac is turned on during the positive half-cycle and turned off during the negative half-cycle.

Several techniques may be used to cope with the half-cycling phenomenon. If the user can tolerate some hystersis in the control, then positive feedback can be added around the differential amplifier. Fig. 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors R_1 and R_2 for different sensor impedances at the control point.

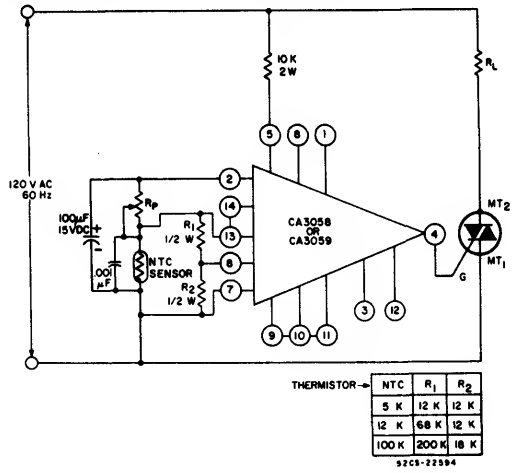


Fig. 11 – CA3058 or CA3059 on-off controller with hysteresis.

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 12 may be employed. In this configuration, external transistor Q_1 can be used to provide an auxiliary timed-delay function.

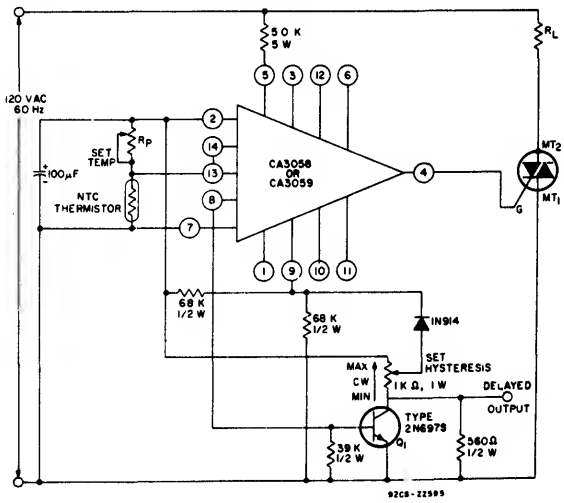


Fig. 12 – CA3058 or CA3059 on-off controller with controlled hysteresis.

For applications that require complete elimination of half-cycling without the addition of hysteresis, the circuit shown in Fig. 13 may be employed. This circuit uses a

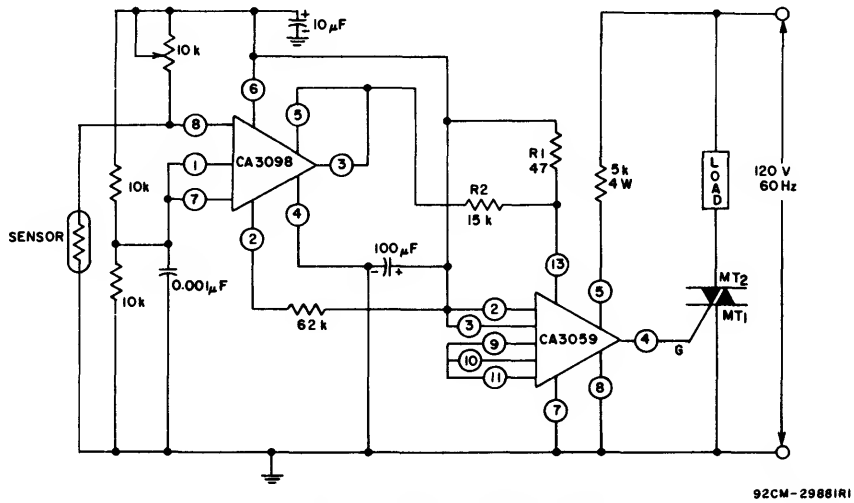


Fig. 13 – Sensitive temperature control.

CA3098E integrated-circuit programmable comparator with a zero-voltage switch. A block diagram of CA3098E is shown in Fig. 14. Because the CA3098E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half-cycling operation is prevented. When the signal-input voltage at terminal 8 of the CA3098E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor R_1 and R_2, and a logic "0" is applied to terminal 13 of the zero-voltage switch. This condition turns off the triac. The triac remains off until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop so that a logic "1" is applied to terminal 13 of the zero-voltage switch, and triggers the triac on.

"Proportional Control" Systems

The on-off nature of the control shown in Fig. 1 causes some overshoot that leads to a definite steady-state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Fig. 15(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free-running multivibrator. At balance, the voltage at terminal 13 is much less than the voltage at terminal 9. The output will be inhibited at all times until the voltage at terminal 13 rises to the design differential voltage between terminals 13 and 9; then proportional control resumes. The voltage at terminal 13 is as shown in Fig. 15(b). When this voltage is more positive than the threshold, power is

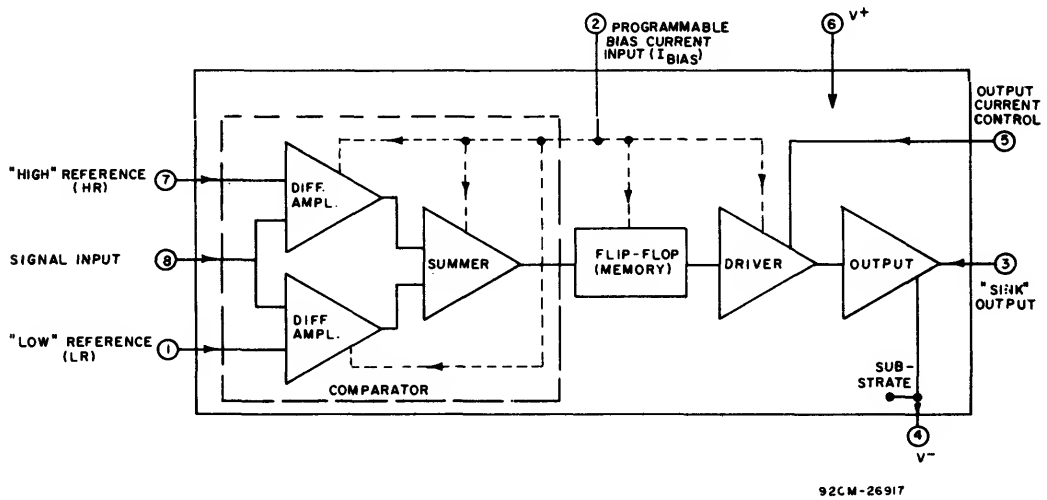


Fig. 14 – Block diagram of CA3098 programmable Schmitt trigger.

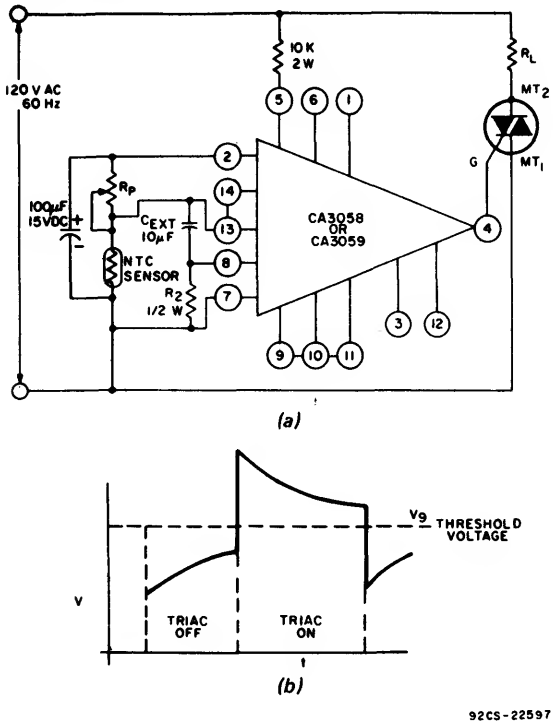


Fig. 15 – Use of the CA3058 or CA3059 in a typical heating control with proportional control: (a) schematic diagram, and (b) waveform of voltage at terminal 13.

applied to the load so that the duty cycle is approximately 50 per cent. With a 0.1 megohm sensor and values of R_P = 0.1 megohm, R_2 = 10,000 ohms, and C_{EXT} = 10 microfarads, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. A change in the value of any of these elements changes the period, as shown in Fig. 16. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9. A cooling sensor moves V_{13} in a positive direction. The triac is on for a larger portion of the pulse cycle and increases the average power to the load.

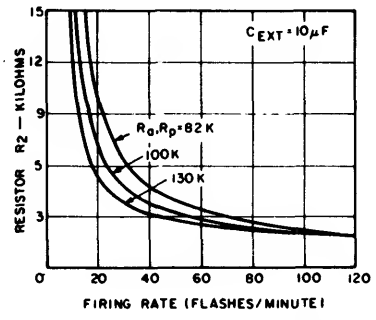


Fig. 16 – Effect of variations in time-constant elements on period.

As in the case of the hysteresis circuitry described earlier, some special applications may require more sophisticated systems to achieve either very precise regions of control or very long periods.

Zero-voltage switching control can be extended to applications in which it is desirable to have constant control of the temperature and a minimization of system hysteresis. A closed-loop top-burner control in which the temperature of the cooking utensil is sensed and maintained at a particular value is a good example of such an application; the circuit for this control is shown in Fig. 17. In this circuit, a unijunction

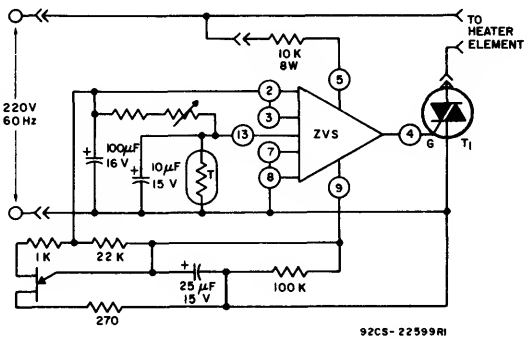


Fig. 17 – Schematic diagram of proportional zero-voltage switching control.

oscillator is outboarded from the basic control by means of the internal power supply of the zero-voltage switch. The output of this ramp generator is applied to terminal 9 of the zero-voltage switch and establishes a varied reference to the differential amplifier. Therefore, gate pulses are applied to the triac whenever the voltage at terminal 13 is greater than the voltage at terminal 9. A varying duty cycle is established in which the load is predominantly on with a cold sensor and predominantly off with a hot sensor. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system but longer than the period of the 60-Hz line. Fig. 18, which contains various waveforms for the system of Fig. 17, indicates that a typical variance of ±0.5°C might be expected at the sensor contact to the utensil. Overshoot of the set temperature is minimized with this approach, and scorching of any type is minimized.

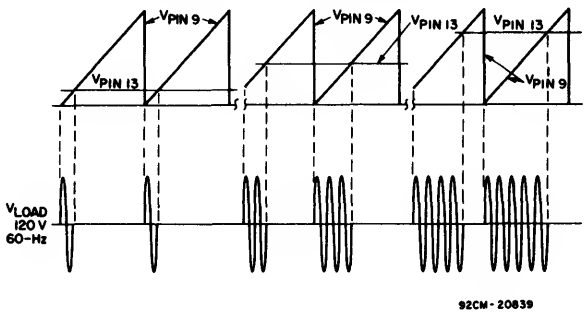


Fig. 18 – Waveforms for the circuit of Fig. 17.

Effect of Thyristor Load Characteristics

The zero-voltage switch is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the switch is of short duration, the latching current of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching-current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the zero-voltage switch to accommodate inductive loads and low-power loads. For example, for loads that are less than approximately 4 amperes rms or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor C_X from terminal 5 to terminal 7. The insertion of capacitor C_X permits switching of triac loads that have a slight inductive component and that are greater than approximately 200 watts (for operation from an ac line voltage of 120 volts rms). However, for loads less than 200 watts (for example, 70 watts), it is recommended that the user employ the T2300B* sensitive-gate triac with the zero-voltage switch because of the low latching-current requirement of this triac.

For loads that have a low power factor, such as a solenoid valve, the user may operate the zero-voltage switch in the dc mode. In this mode, terminal 12 is connected to terminal 7, and the zero-crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the integrated-circuit zero-voltage switch, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the zero-voltage switch no longer operates as a zero-voltage switch. However, for many applications that involve the switching of low-current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high-current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual-output over-under temperature controller and the transient-free switch controller described subsequently in this Note is recommended.

Switching of Inductive Loads

For proper driving of a thyristor in full-cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described previously. For highly inductive loads, however, this method is not suitable, and different techniques must be used.

If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero-crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI-eliminating function of the zero-voltage switch is inhibited when the zero-crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

Circuits that use a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Fig. 19 uses a CA3086 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops, or 1.3 volts. When A is positive, transistors Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors Q_1 and Q_2 conduct. When the voltage at point A is less than ±1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor R_3, and the output in inhibited.

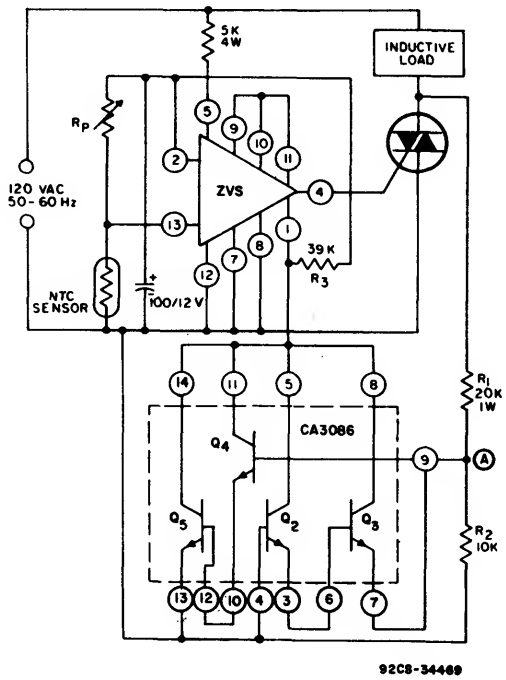


Fig. 19 – Use of the CA3058 or CA3059 together with CA3086 for switching inductive loads.

The circuit shown in Fig. 19 forms a pulse of gate current and can supply high peak drive to power traics with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that

* Formerly RCA 40526

there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts: therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage (v_T) of the thyristor. For most RCA thyristors, v_T (max) is less than 2 volts, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I^+ and II^- modes). Sensitivity is degraded when the polarities are opposite (I^- and III^+ modes). Although RCA triacs are designed and specified to have the same sensitivity in both I^- and III^+ modes, some other types have very poor sensitivity in the III^+ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 20(a) uses the negative-going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Fig. 20(b) shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80 microseconds.

Operation with Low-Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliampere. On the other hand, a 300-ohm sensor draws a current of 8 to 10 milliampers from the power supply.

Fig. 21 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the zero-voltage switch. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts, and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

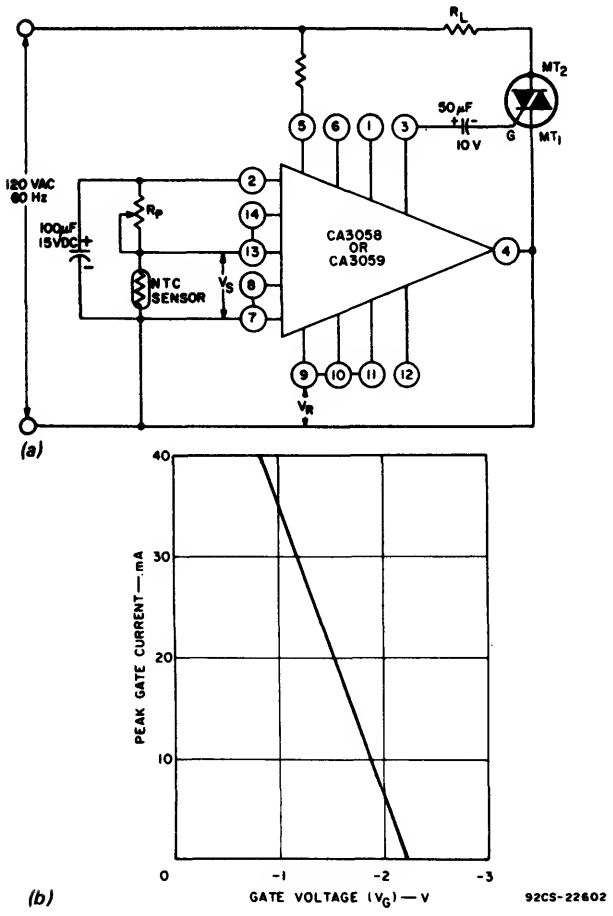


Fig. 20 – Use of the CA3058 or CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.

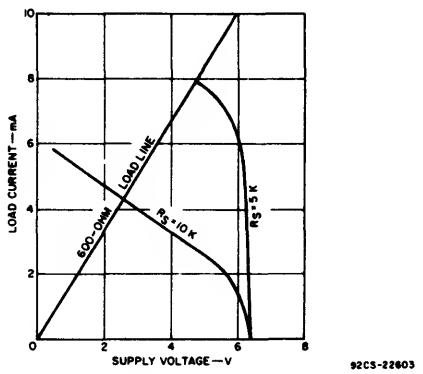


Fig. 21 – Power-supply regulation of the CA3058 or CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.

Although positive-temperature-coefficient (PTC) sensors rated at 5 kilohms are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Fig. 22 is offered to accommodate these inexpensive metal-wound

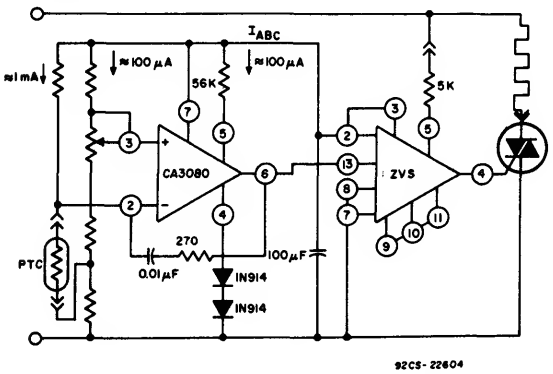


Fig. 22 – Schematic diegrem of circuit for use with low-resistence sensor.

sensors. A schematic diagram of the RCA CA3080 integrated-circuit operational transconductance amplifier used in Fig. 22, is shown in Fig. 23. With an amplifier bias current, I_{ABC}, of 100 microamperes, a forward transconductance of 2 milliohms is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, I_s, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50 kilohms); gate pulses are no longer applied to the triac because Q_2 of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off. Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

Interfacing Techniques

Fig. 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic

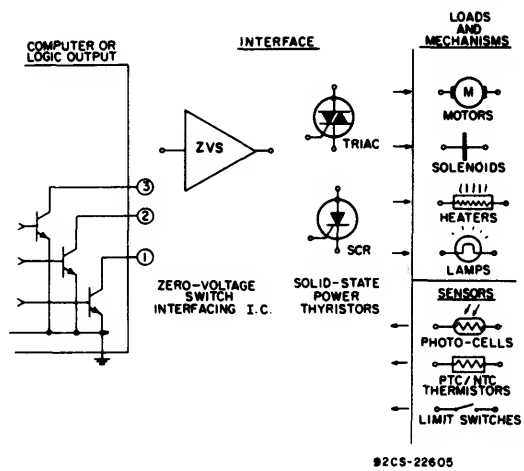


Fig. 24 – The zero-voltage switch and thyristor as an interface.

interfacing techniques. Fig. 25(a) shows the **direct input** technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero-crossing pulses from the zero-voltage switch to the triac

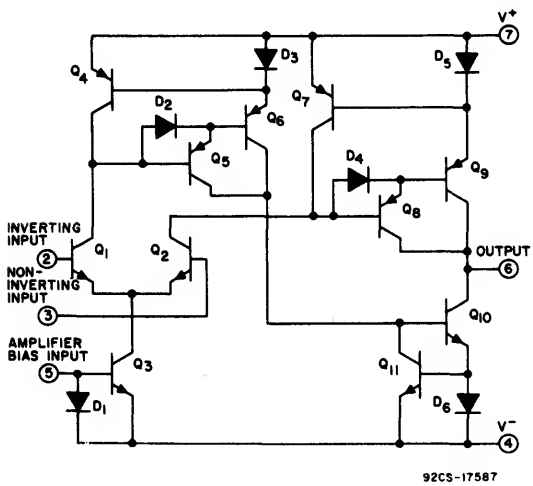


Fig. 23 – Schematic diagram of the CA3080.

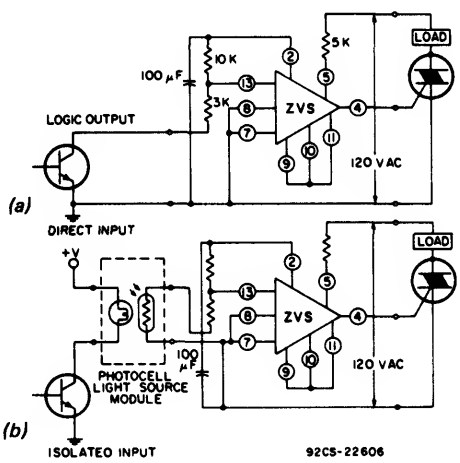


Fig. 25 – Basic interfacing techniques: (a) direct input; (b) isolated input.

gate will immediately cease. Therefore, the load will be turned off when the triac commutates off as the sine-wave load current goes through zero. In this manner, both the turn-on and turn-off conditions for the load are controlled.

When electrical isolation between the logic circuit and the load is necessary, the **isolated-input** technique shown in Fig. 25(b) is used. In the technique shown, optical coupling is used to achieve the necessary isolation. The logic output transistor switches the light-source portion of the isolator. The light-sensor portion changes from a high impedance to a low impedance when the logic output transistor is switched from

In temperature monitoring or control applications the sensor may be a temperature-dependent element such as a resistor, thermistor, or diode. The load may be a lamp, bell, horn, recorder or other appropriate device connected in a feedback relationship to the sensor.

For the purpose of the following explanation, assume that the sensor is a resistor having a negative temperature coefficient and that the load is a heater thermally coupled to the sensor, the object being to maintain the thermal-coupling medium at a desired reference temperature. Assume initially that the temperature at the coupling medium is low.

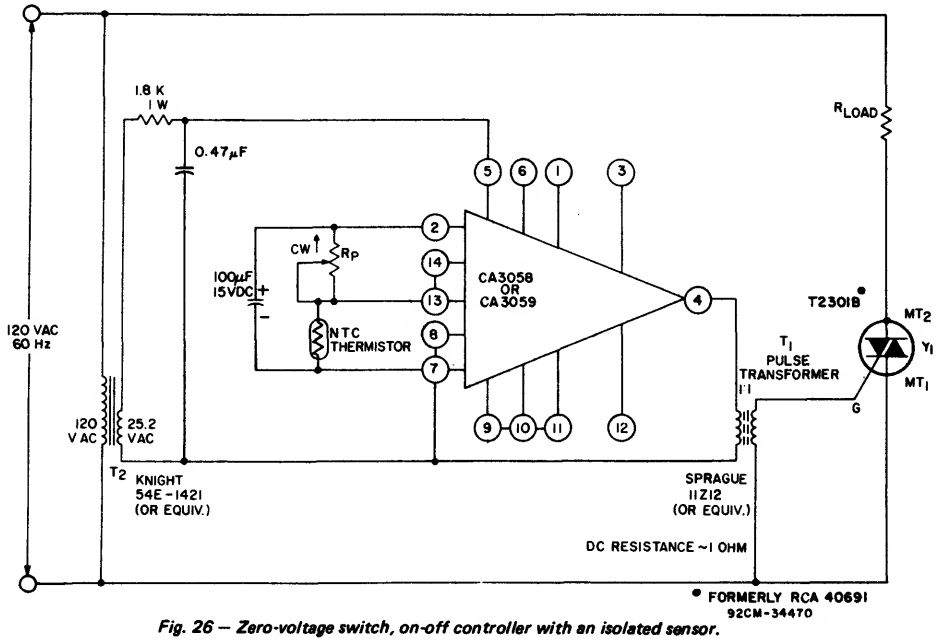


Fig. 26 – Zero-voltage switch, on-off controller with an isolated sensor.

off to on. The light sensor is connected to the differential amplifier input of the zero-voltage switch, which senses the change of impedance at a threshold level and switches the load on as in Fig. 25(a).

Sensor Isolation

In many applications, electrical isolation of the sensor from the ac input line is desirable. Several isolation techniques are shown in Figs. 26, 27, and 28.

Transformer Isolation – In Fig. 26, a pulse transformer is used to provide electrical isolation of the sensor from incoming ac power lines. The pulse transformer T_1 isolates the sensor from terminal No. 1 of the triac Y_1, and transformer T_2 isolates the CA3058 or CA3059 from the power lines. Capacitor C_1 shifts the phase of the output pulse at terminal No. 4 in order to retard the gate pulse delivered to triac Y_1 to compensate for the small phase-shift introduced by transformer T_1.

Many applications require line isolation but not zero-voltage switching. A line-isolated temperature controller for use with inductive or resistive loads that does not include zero-voltage switching is shown in Fig. 27.

The operating potentials applied to the bridge circuit produce a common-mode potential, V_{CM}, at the input terminals of the CA3094. Assuming the bridge to have been initially balanced (by adjustment of R4), the potential at point A will increase when temperature is low since it was assumed that the sensor has a negative temperature coefficient. The potential at the noninverting terminal, being greater than that at the inverting terminal at the amplifier, causes the multivibrator to oscillate at approximately 10 kHz. The oscillations are transformer-coupled through a current-limiting resistor to the gate of the thyristor, and trigger it into conduction.

When the thyristor conducts, the load receives ac input power, which tends to increase the temperature of the sensor. This temperature increase decreases the potential at point A to a value below that at point B and the multivibrator is disabled, which action, in turn, turns off the thyristor. The temperature is thus controlled in an on-off fashion.

Capacitor C_1 is used to provide a low impedance path to ground for feedback-induced signals at terminal No. 5 while blocking the direct current bias provided by resistor R1. Resistor R2 provides current limiting. Resistor R3 limits the

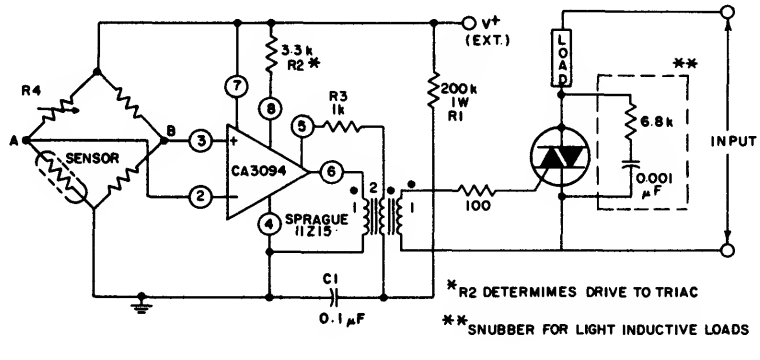


Fig. 27 – A line-isolated temperature controller for use with inductive or resistive loads; this controller does not include zero-voltage switching.

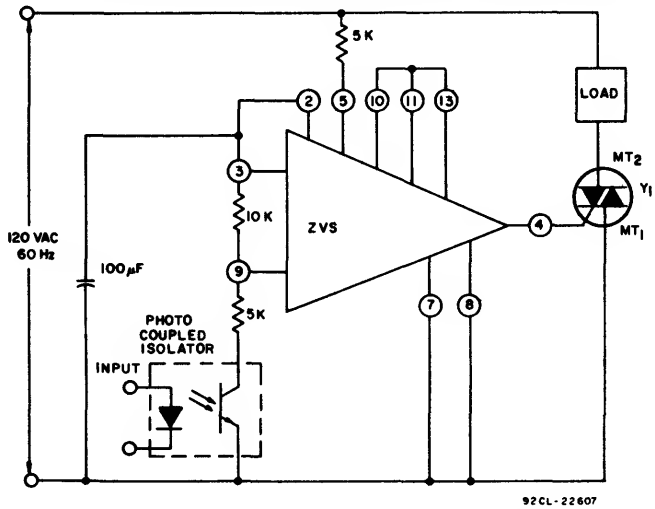


Fig. 28 – Zero-voltage switch, on-off controller with photocoupler.

secondary current of the transformer to prevent excessive current flow to the control terminal of the CA3094.

Photocoupler Isolation – In Fig. 28, a photocoupler provides electrical isolation of the sensor logic from the incoming ac power lines. When a logic "1" is applied at the input of the photocoupler, the triac controlling the load will be turned on whenever the line voltage passes through zero. When a logic "0" is applied to the photocoupler, the triac will turn off and remain off until a logic "1" appears at the input of the photocoupler.

TEMPERATURE CONTROLLERS

Fig. 29 shows a triac used in an on-off temperature-controller configuration. The triac is turned on at zero voltage whenever the voltage V_s exceeds the reference

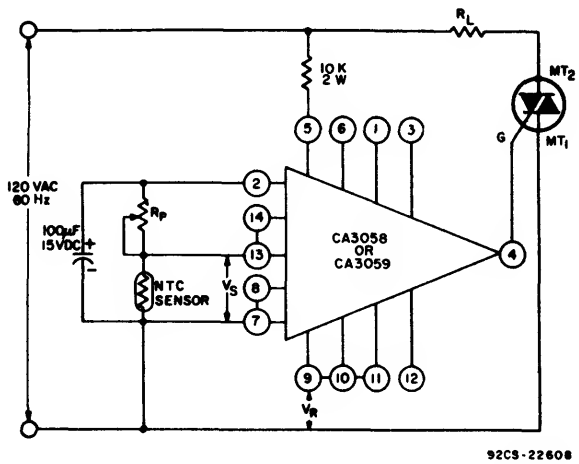


Fig. 29 – CA3058 or CA3059 on-off temperature controller.

voltage V_r. The transfer characteristic of this system, shown in Fig. 30(a), indicates significant thermal overshoots and undershoots, a well-known characteristic of such a system. The differential or hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

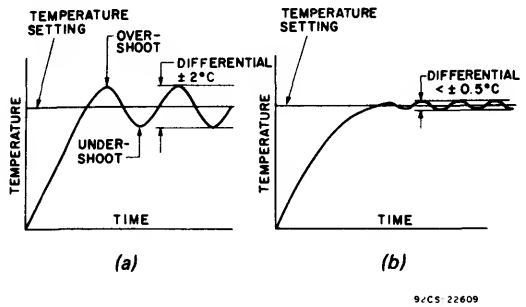


Fig. 30 – Transfer characteristics of (a) on-off and (b) proportional control systems.

For precise temperature-control applications, the proportional-control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Fig. 30(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an on-off type of controller, full power (100 per cent duty cycle) is supplied to the system. This effect results in significant temperature excursions because there is no anticipatory circuit to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

Before such a system is implemented, a time base is chosen so that the on-time of the triac is varied within this time base. The ratio of the on-to-off time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Fig. 31 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the dc control signal supplied to the opposite side of the differential amplifier. The triac then remains off for the remainder of the time-base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. A ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed-loop type of control. In the circuit shown in Fig. 32, the ramp voltage is generated when

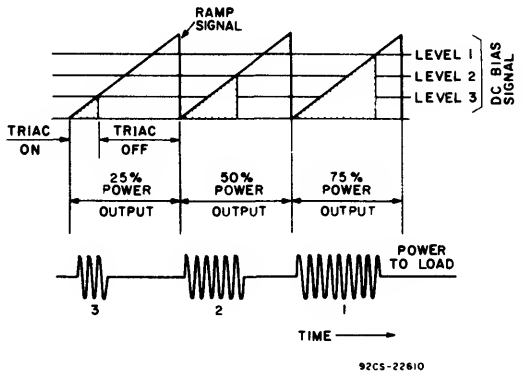


Fig. 31 – Principles of proportional control.

the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the D3202U* diac.

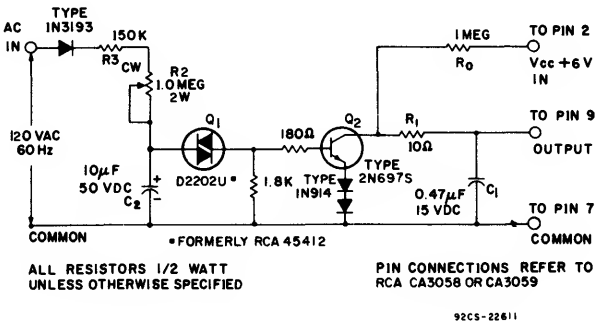


Fig. 32 – Ramp generator.

When the voltage across C_2 reaches approximately 32 volts, the diac switches and turns on the 2N697S transistor and 1N914 diodes. The capacitor C_1 then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60-Hz line voltage. Fig. 33 shows a triac connected for the proportional mode.

Fig. 34(a) shows a dual-output temperature controller that drives two triacs. When the voltage V_s developed across the temperature-sensing network exceeds the reference voltage V_{R1}, motor No. 1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, motor No. 2 turns on. Because the motors are inductive, the currents I_{M1} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 34(b).

* Formerly RCA 45412

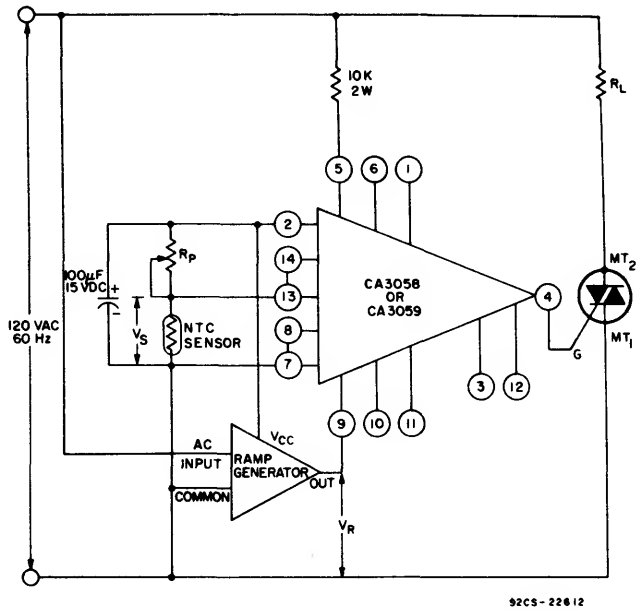
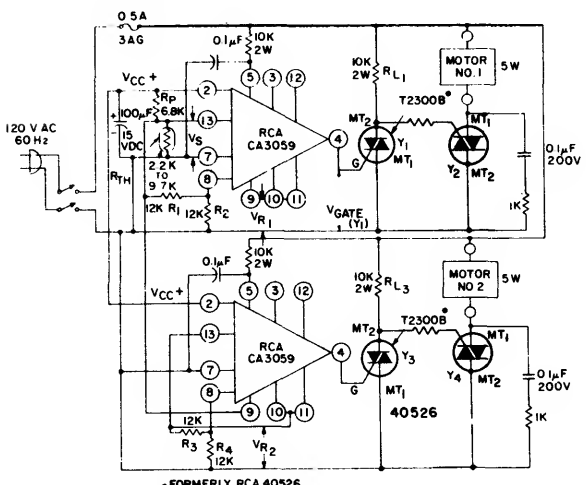


Fig. 33 – CA3058 or CA3059 proportional temperature controller.

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 34(a), it is apparent that, though the gate pulse V_g of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in R_{L1}, as opposed to 10 to 20 watts when devices that have high latching currents are used.



Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from the switching transients. The salient features of the 2N5444 40-ampere triac are as follows:

(1) 300-ampere single-surge capability (for operation at 60-Hz),

(2) a typical gate sensitivity of 20 milliamperes in the $I(^+)$ and $III(^+)$ modes,

(3) low on-state voltage of 1.5 volts maximum at 40 amperes, and

(4) available V_{DROM} equal to 600 volts.

Fig. 35 shows the circuit diagram of a synchronous-switching heat-staging controller that is used for electric heating systems. Loads as heavy as 5 kilowatts are switched sequentially at zero voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25 kilowatts were to be switched simultaneously.

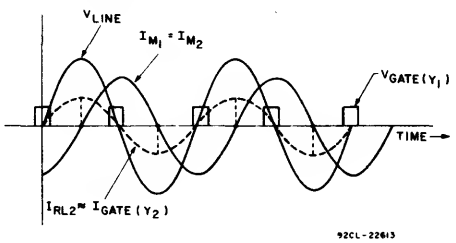


Fig. 34 – Dual output, over-under temperature controller (a) circuit, (b) voltage and current waveforms.

Transistor Q_1 and Q_4 are used as a constant-current source to charge capacitor C in a linear manner. Transistor Q_2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_o. At approximately 3-second intervals, each 5-kilowatt heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R_1 and R_2 to cause each triac to turn off in the reverse heating sequence. It should be noted that some half-cycling occurs before the heating element is switched fully on. This condition can be attributed to the inherent dissymmetry of the triac and is further aggravated by the slow-rising ramp voltage applied to one of the inputs. The timing diagram in Fig. 36 shows the turn-on and turn-off sequence of the heating system being controlled.

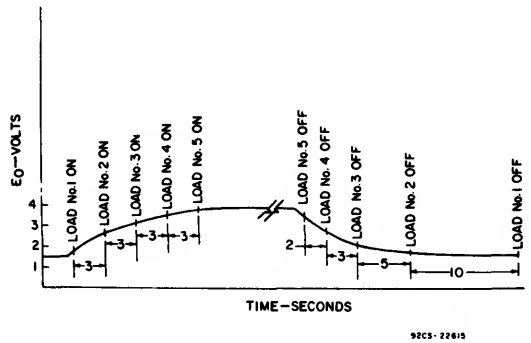


Fig. 36 — Ramp-voltage waveform for the heat-staging controller.

Seemingly, the basic method shown in Fig. 35 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitably results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.

Oven/Broiler Control

Zero-voltage switching is demonstrated in the oven control circuit shown in Fig. 37. In this circuit, a sensor element is included in the oven to provide a closed-loop system for accurate control of the oven temperature.

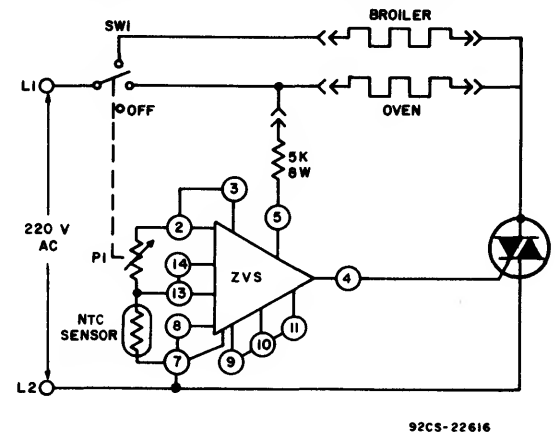


Fig. 37 — Schematic diagram of basic oven control.

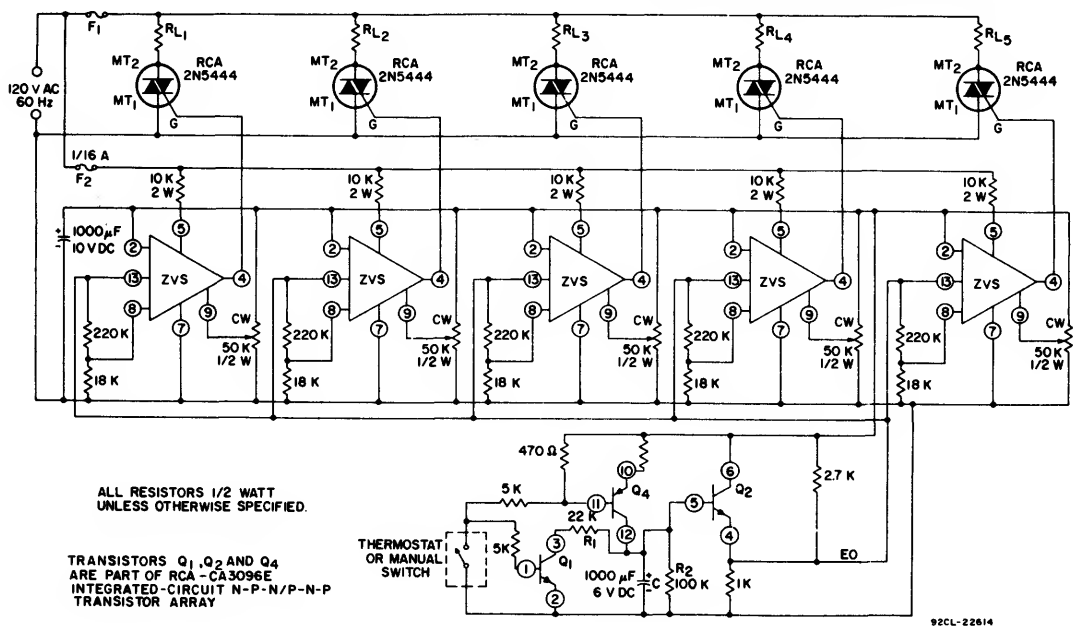


Fig. 35 — Synchronous-switching heat-staging controller using a series of zero-voltage switches.

As shown in Fig. 37, the temperature of the oven can be adjusted by means of potentiometer R_1, which acts, together with the sensor, as a voltage divider at terminal 13. The voltage at terminal 13 is compared to the fixed bias at terminal 9 which is set by internal resistors R_4 and R_5. When the oven is cold and the resistance of the sensor is high, transistors Q_2 and Q_4 are off, a pulse of gate current is applied to the triac, and heat is applied to the oven. Conversely, as the desired temperature is reached, the bias at terminal 13 turns the triac off. The closed-loop feature then cycles the oven element on and off to maintain the desired temperature to approximately ±2°C of the set value. Also, as has been noted, external resistors between terminals 13 and 8, and 7 and 8, can be used to vary this temperature and provide hysteresis. In Fig. 11, a circuit that provides approximately 10-per-cent hysteresis is demonstrated.

In addition to allowing the selection of a hysteresis value, the flexibility of the control circuit permits incorporation of other features. A PTC sensor is readily used by interchanging terminals 9 and 13 of the circuit shown in Fig. 37 and substituting the PTC for the NTC sensor. In both cases, the sensor element is directly returned to the system ground or common, as is often desired. Terminal 9 can be connected by external resistors to provide for a variety of biasing, e.g., to match a lower-resistance sensor for which the switching-point voltage has been reduced to maintain the same sensor current.

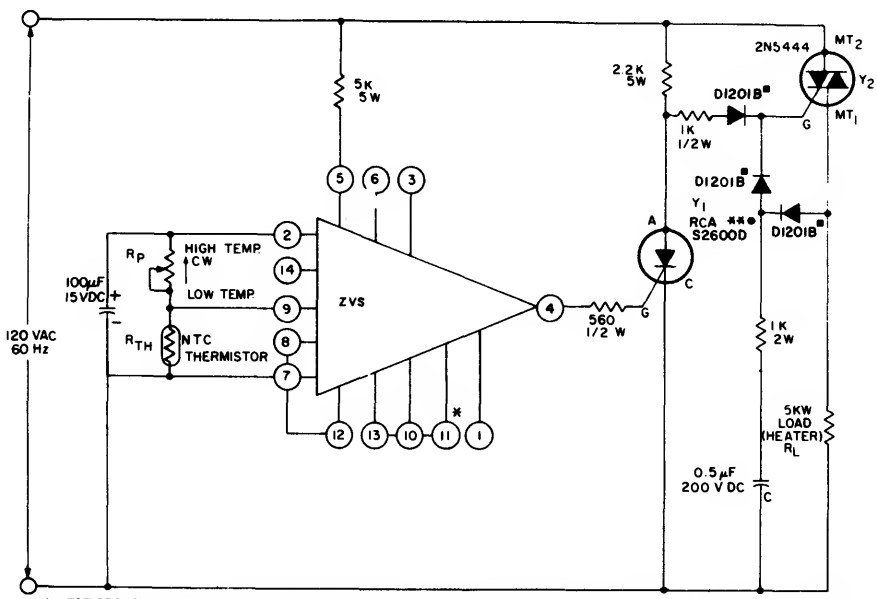
To accommodate the self-cleaning feature, external switching, which enables both broiler and oven units to be paralleled, can easily be incorporated in the design. Of course, the potentiometer must be capable of a setting such that the sensor, which must be characterized for the high, self-clean temperature, can monitor and establish control of the high-temperature, self-clean mode. The ease with which this self-clean mode can be added makes the over-all solid-state systems cost-competitive with electromechanical systems of comparable capability. In addition, the system incorporates solid-state reliability while being neater, more easily calibrated, and containing less-costly system wiring.

Integral-Cycle Temperature Controller (No half-cycling)

If a temperature controller which is completely devoid of half-cycling and hysteresis is required, then the circuit shown in Fig. 38 may be used. This type of circuit is essential for applications in which half-cycling and the resultant dc component could cause overheating of a power transformer on the utility lines.

In the integral-cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high, and an output signal at terminal 4 of zero volts is obtained. The SCR (Y_1), therefore, is turned off. The triac (Y_2) is then triggered directly from the line on positive cycles of the ac voltage. When Y_2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage. When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycle to provide only **integral** cycles of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 10,11, AND 13, AND CONNECT POSITIVE RAMP VOLTAGE TO TERMINAL 13
** SELECTED FOR I_{GT}=6 mA MAXIMUM.
■ FORMERLY RCA 44003
● FORMERLY RCA 40655

92CM-22617

Fig. 38 — Integral-cycle temperature controller in which half-cycling effect is eliminated.

then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

The circuit shown in Fig. 39 is similar to the configuration in Fig. 38 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_O inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the zero-voltage switch supplies bias current to transistor Q_O.

Of course, the circuit shown in Fig. 39 can readily be converted to a **true proportional integral-cycle temperature controller** simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.

Thermocouple Temperature Control

Fig. 40 shows the CA3080A operating as a pre-amplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.

Thermocouple Temperature Control with Zero-Voltage Load Switching

Fig. 41 shows the circuit diagram of a thermocouple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connected to one leg of the supply line. Consequently, the thermocouple can be "ground-referenced", provided the appropriate

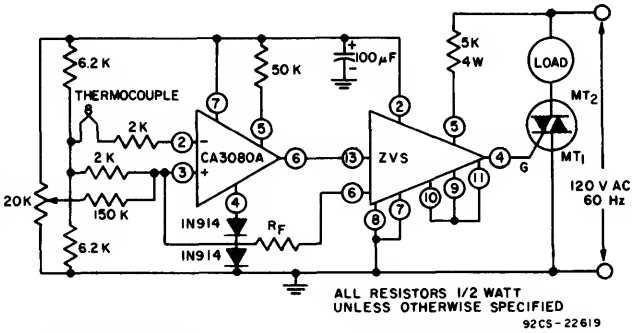


Fig. 40 – Thermocouple temperature control with zero-voltage switching.

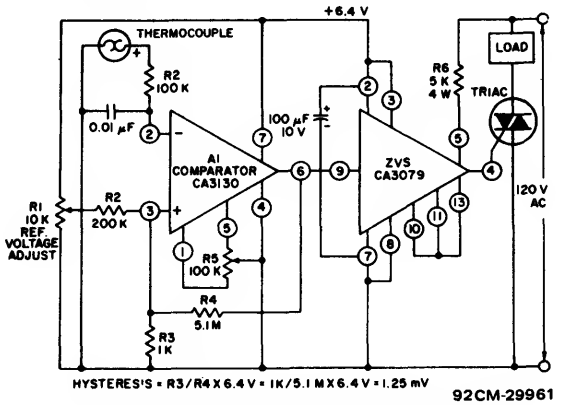
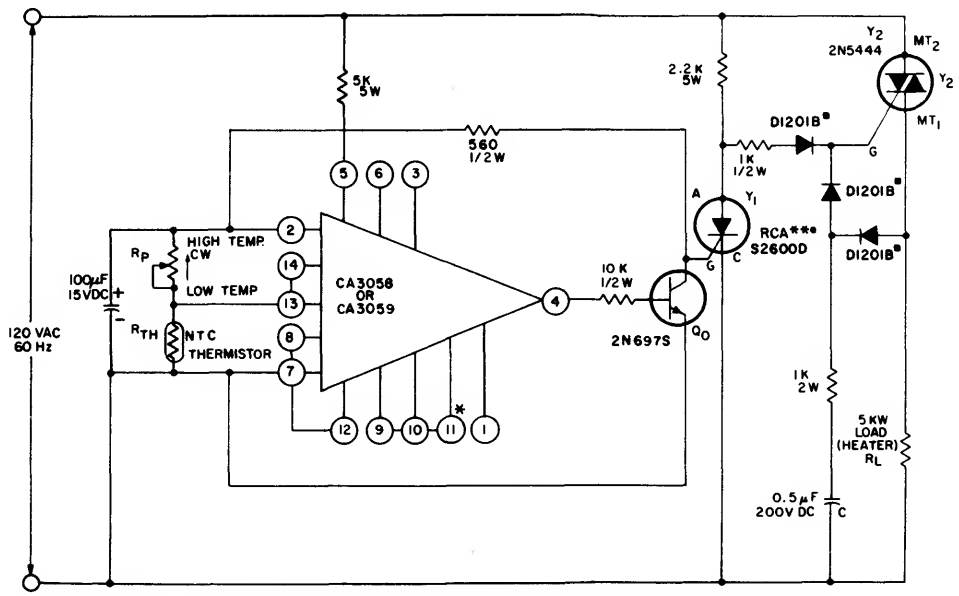


Fig. 41 – Thermocouple temperature control with zero-voltage switching.



* FOR PROPORTIONAL OPERATION OPEN TERMINALS 9,10 AND 11 AND CONNECT POSTIVE RAMP VOLTAGE TO TERMINAL 9
** SELECTED FOR I_{GT} = 6 mA MAXIMUM
92CM-22618
*FORMERLY RCA 44003
*FORMERLY RCA 40655

Fig. 39 – CA3058 or CA3059 integral-cycle temperature controller that features a protection circuit and no half-cycling effect.

leg of the ac line is maintained at ground. The comparator, A_1 (a CA3130), is powered from a 6.4-volt source of potential provided by the zero-voltage-switch (ZVS) circuit (a CA3079). The ZVS, in turn, is powered off-line through a series-dropping resistor R6. Terminal 4 of the ZVS provides trigger-pulses to the gate of the load-switching triac in response to an appropriate control signal at terminal 9.

The CA3130 is an ideal choice for the type of comparator circuit shown in Fig. 41 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R1 drives the voltage-divider network R3, R4 so that reference voltages over the range of 0 to 20 millivolts can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Fig. 41, the circuit is provided with a control-point "hysteresis" of 1.25 millivolts.

Nulling of the comparator is performed by means of the following procedure: Set R1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the nonconductive mode under the conditions above, adjust R5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R1 can be set to the voltage threshold desired for control-circuit operation.

MACHINE CONTROL AND AUTOMATION

The earlier section on interfacing techniques indicated several techniques of controlling ac loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Fig. 42; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

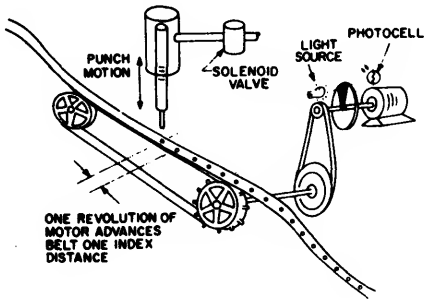


Fig. 42 – Step-and-punch machine.

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial-grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Fig. 43 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

a. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.

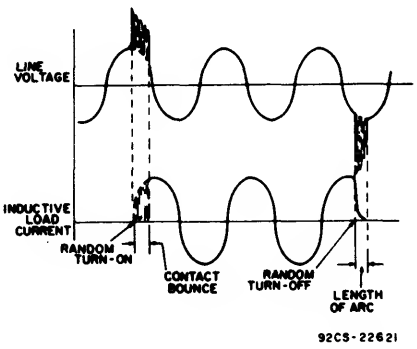


Fig. 43 – Transients generated by relay-contact bounce and non-zero turn-off of inductive load.

b. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.
c. Elimination of high-voltage transients generated by relay-contact bounce and contacts breaking inductive loads, as shown in Fig. 42.
d. Compactness of the control system.

The entire control system could be on one printed-circuit board, and an over-all cost advantage would be achieved. Fig. 44 is a timing diagram for the proposed solid-state

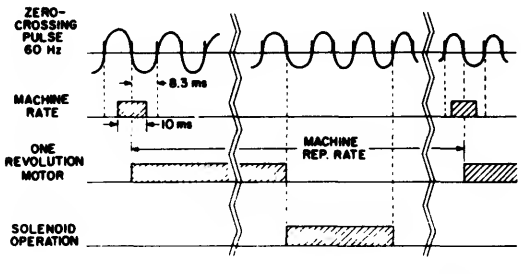


Fig. 44 – Timing diagram for proposed solid-state machine control.

machine control, and Fig. 45 is the corresponding control schematic. A variable-speed machine repetition rate pulse is set up using either a unijunction oscillator or a transistor astable multivibrator in conjunction with a 10-millisecond one-shot multivibrator. The first zero-voltage switch in Fig. 45 is used to synchronize the entire system to zero-voltage crossing. Its output is inverted to simplify adaptation to the rest of the circuit. The center zero-voltage switch is used as an interface for the photo-cell, to control one revolution of the motor. The gate drive to the motor triac is continuous dc, starting at zero voltage crossing. The motor is initiated when both the machine rate pulse and the zero-voltage sync are at low voltage. The bottom zero-voltage switch acts as a time-delay for pulsing the solenoid. The inhibit input, terminal 1, is used to assure that the solenoid will not be operated while the motor is running. The time delay can be adjusted by varying the reference level (50K potentiometer) at terminal 13 relative to the capacitor charging to that level on terminal 9. The capacitor is reset by the SCR during the motor operation. The gate drive to the solenoid triac is direct current. Direct current is used to trigger both the motor and solenoid triacs because it is the most desirable means of switching a triac into an inductive load. The output of the zero-voltage switch will be continuous dc by connecting terminal 12 to common. The output under dc operation should be limited to 20 milliamperes. The motor

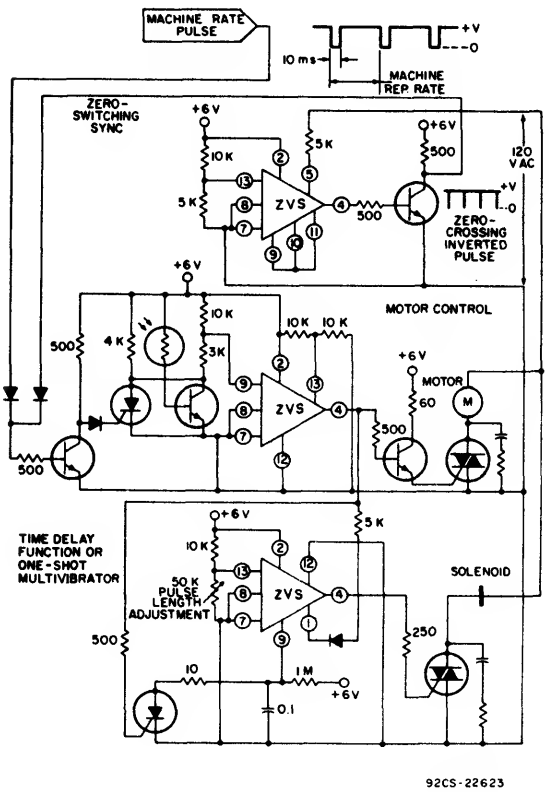


Fig. 45 – Schematic of proposed solid-state machine control.

triac is synchronized to zero crossing because it is a high-crurent inductive load and there is a chance of generating RFI. The solenoid is a very low current inductive load, so there would be little chance of generating RFI: therefore, the initial triac turn-on can be random, which simplifies the circuitry.

This example shows the versatility and advantages of the RCA zero-voltage switch used in conjunction with triacs as interfacing and control elements for machine control.

400-Hz TRIAC APPLICATIONS

The increased complexity of aircraft control systems, and the need for greater reliability than electromechanical switching can offer, has led to the use of solid-state power switching in aircraft. Because 400-Hz power is used almost universally in aircraft systems, RCA offers a complete line of triacs rated for 400-Hz applications. Use of the RCA zero-voltage switch in conjunction with these 400-Hz triacs results in a minimum of RFI, which is especially important in aircraft.

Areas of application for 400-Hz triacs in aircraft include:

a. Heater controls for food-warming ovens and for windshield defrosters.
b. Lighting controls for instrument panels and cabin illumination
c. Motor controls
d. Solenoid controls
e. Power-supply switches

Lamp dimming is a simple triac application that demonstrates an advantage of 400-Hz power over 60-Hz power. Fig. 46 shows the adjustment of lamp intensity by phase control of the 60-Hz line voltage. RFI is generated by the step functions of power each half cycle, requiring extensive filtering. Fig. 47 shows a means of controlling power to the lamp by the zero-voltage-switching technique. Use of 400-Hz power makes possible the elimination of complete or half cycles within a period (typically 17.5 milliseconds)

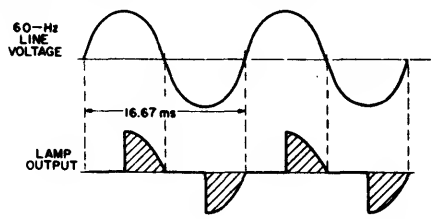


Fig. 46 – Waveforms for 60-Hz phase-controlled lamp dimmer.

without noticeable flicker. Fourteen different levels of lamp intensity can be obtained in this manner. A line-synced ramp is set up with the desired period and applied to terminal No. 9 of the differential amplifier within the zero-voltage switch, as shown in Fig. 48. The other side of the differential amplifier (terminal No. 13) uses a variable reference level, set by the 50K potentiometer. A change of the potentiometer setting changes the lamp intensity.

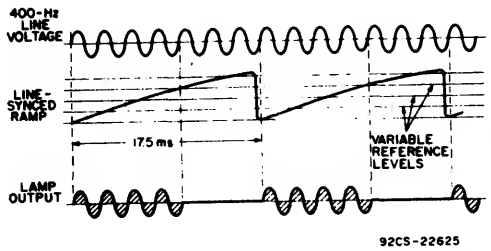


Fig. 47 – Waveforms for 400-Hz zero-voltage-switched lamp dimmer.

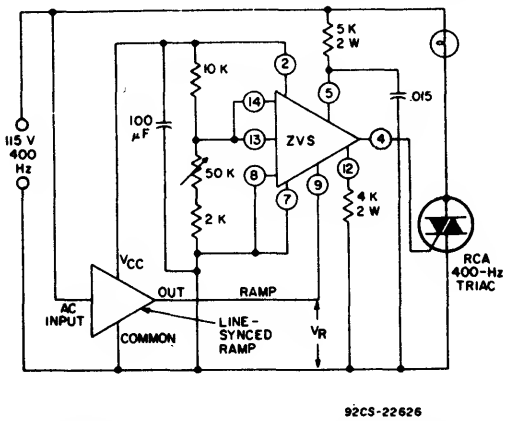


Fig. 48 – Circuit diagram for 400-Hz zero-voltage-switched lamp dimmer.

In 400-Hz applications it may be necessary to widen and shift the zero-voltage switch output pulse (which is typically 12 microseconds wide and centered on zero voltage crossing), to assure that sufficient latching current is available. The 4K resistor (terminal No. 12 to common) and the 0.015-microfarad capacitor (terminal No. 5 to common) are used for this adjustment.

SOLID-STATE TRAFFIC FLASHER

Another application which illustrates the versatility of the zero-voltage switch, when used with RCA thyristors, involves switching traffic-control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current-surge peak is approximately ten times the peak steady-state value or fifteen times the steady-state rms value. The second current-surge peak is approximately four times the steady-state rms value.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn-on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the ac line.

Fig. 49 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt, decreases the required triac surge-current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the zero-voltage switch, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs Y_1 or Y_2 by the output pulses at terminal 4 generated by the zero-crossing circuit.

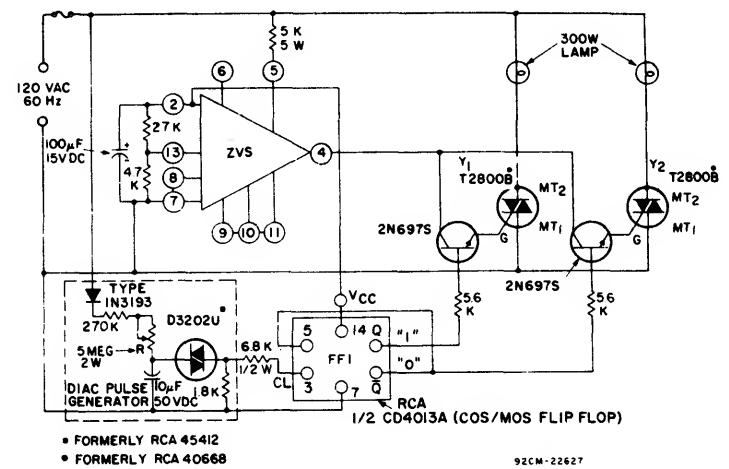


Fig. 49 – Synchronous-switching traffic flasher.

Transistors Q_1 and Q_2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.

The arrangement described can also be used for a synchronous, sequential traffic-controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

SYNCHRONOUS LIGHT FLASHER

Fig. 50 shows a simplified version of the synchronous-switching traffic light flasher shown in Fig. 49.

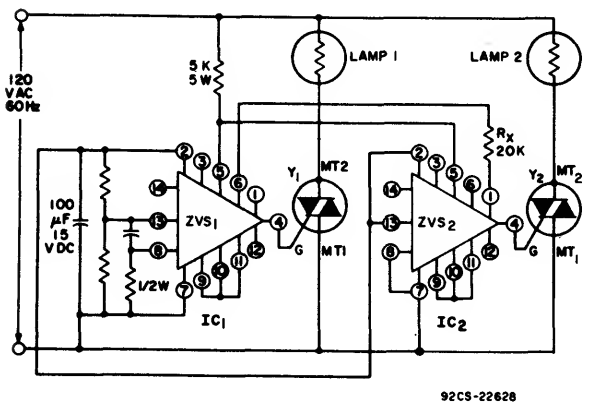


Fig. 50 — Synchronous light flasher.

Flash rate is set by use of the curve shown in Fig. 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, ZVS_1 is the master control unit and ZVS_2 is slaved to the output of ZVS_1 through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on ZVS_1 is high and ZVS_2 is inhibited by the current in R_X. When lamp No. 1 is off, ZVS_2 is not inhibited, and triac Y_2 can fire. The power supplies operate in parallel. The on-off sensing amplifier in ZVS_2 is not used.

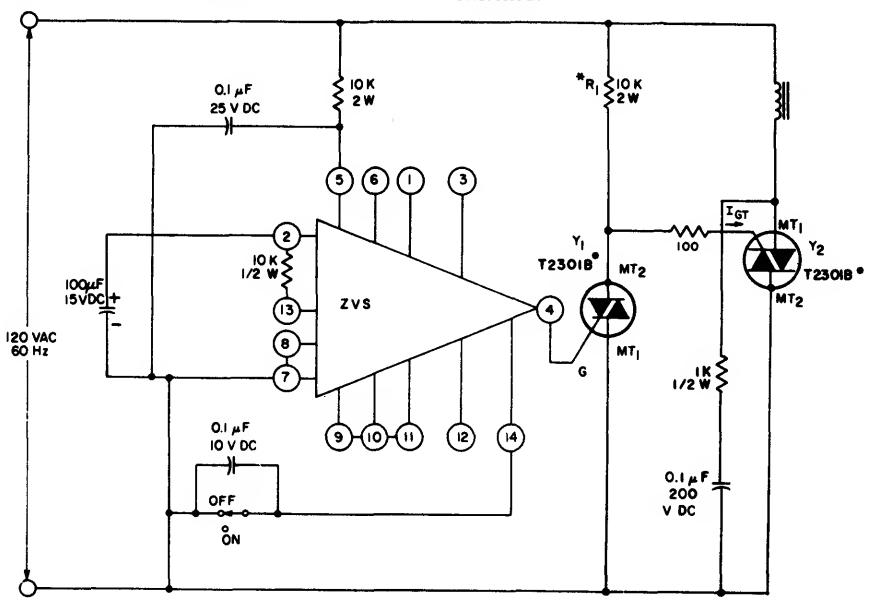
TRANSIENT-FREE SWITCH CONTROLLERS

The zero-voltage switch can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 51 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 52 is connected to provide the opposite control logic to that of the circuit shown in Fig. 51. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2. If Y_2 is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2.

•FORMERLY RCA 40691

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Fig. 51 — Zero-voltage switch transient-free switch controller in which power is supplied to the load when the switch is open.

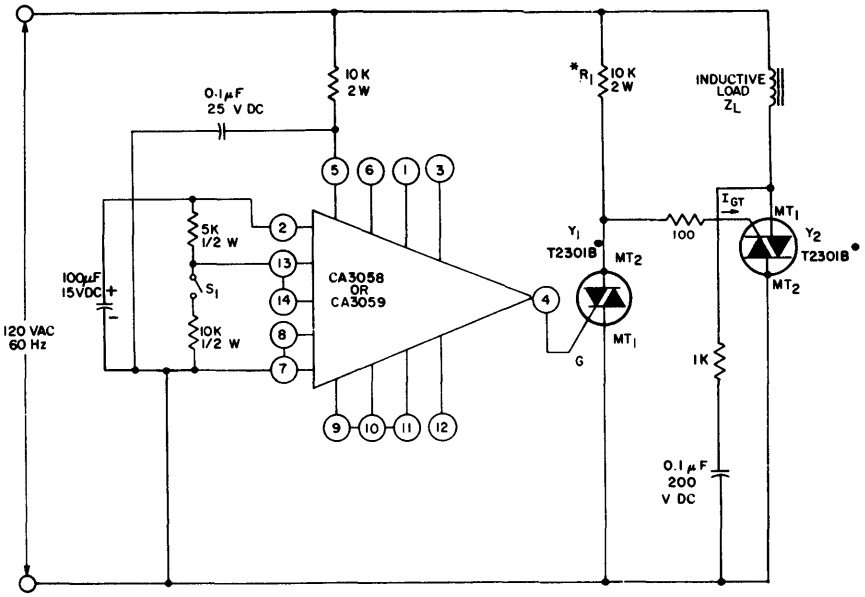

Fig. 52 – Zero-voltage switch transient-free switch controller in which power is applied to the load when the switch is closed.

DIFFERENTIAL COMPARATOR FOR INDUSTRIAL USE

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic 'one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Fig. 53 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the zero-voltage switch is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

When the zero-voltage switch is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of dc voltage from terminals 2 and 7. This curve is shown in the technical bulletin for RCA integrated-circuit zero-voltage switches, File No. 490. Of course, if additional output current is required, an external dc supply may be connected between terminals 2 and 7, and resistor R_X (shown in Fig. 53) may be removed.

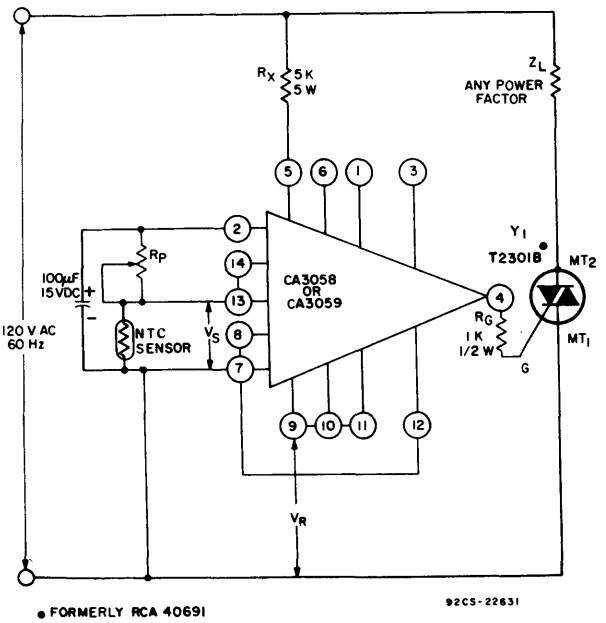

Fig. 53 – Differential comparator using the CA3058 or CA3059 integrated-circuit zero-voltage switch.

The chart below compares some of the operating characteristics of the zero-voltage switch, when used as a comparator, with a typical high-performance commercially available integrated-circuit differential comparator.

Parameters	Zero-Voltage Switch (Typical Values)	Typical Integrated-Circuit Comparator (710)
Sensitivity	30 mV	2 mV
Switching speed (rise time)	$> 20\ \mu s$	90 ns
Output drive capability	*4.5 V at $\leqslant$ 4 mA	3.2 V at $\leqslant$ 5.0 mA

* Refer to Fig. 20; R_X equals 5000 ohms.

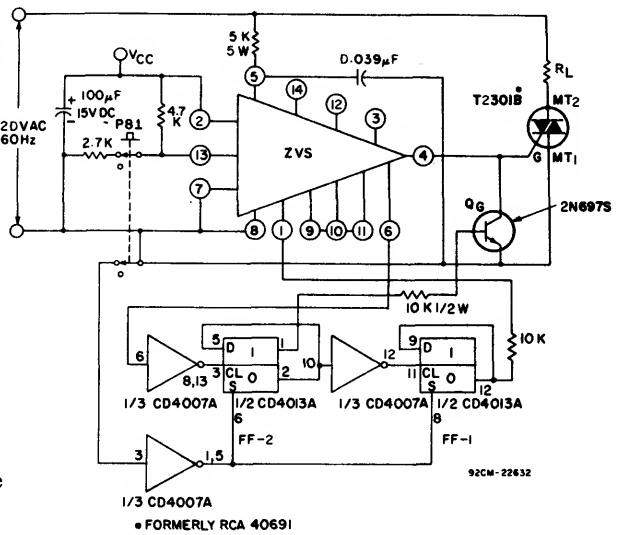

Fig. 54 — Block diagram of a power one-shot control using a zero-voltage switch.

POWER ONE-SHOT CONTROL

Fig. 54 shows a circuit which triggers a triac for one complete half-cycle of either the positive or negative alternation of the ac line voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the ac cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and the like, where load-current flow is required for only one complete half-cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Fig. 54, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor Q_G is biased on by the output of flip-flop FF-1. The differential comparator which is part of the zero-voltage switch is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor Q_7, as shown in Fig. 55, which inhibits all further output pulses. When the pushbutton is released, the circuit resets itself until the process is repeated with the button. Fig. 56 shows the timing diagram for the described operating sequence.

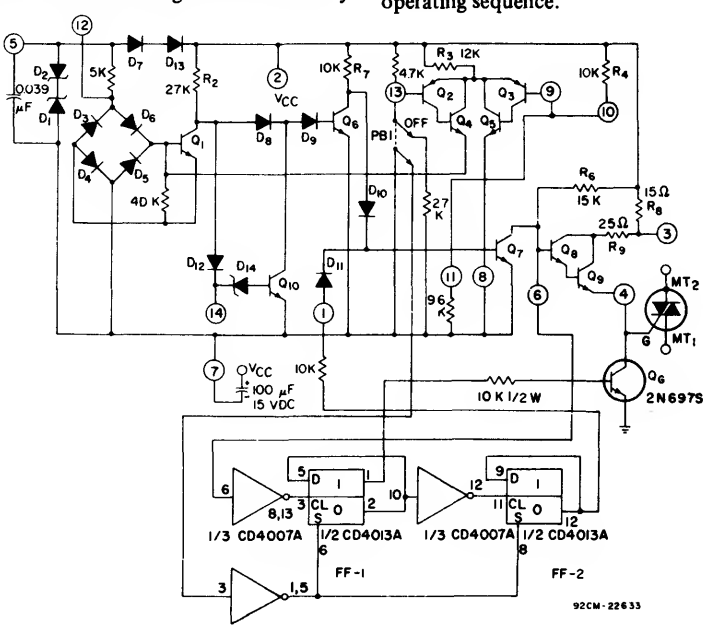

Fig. 55 — Circuit diagram for the power one-shot control.

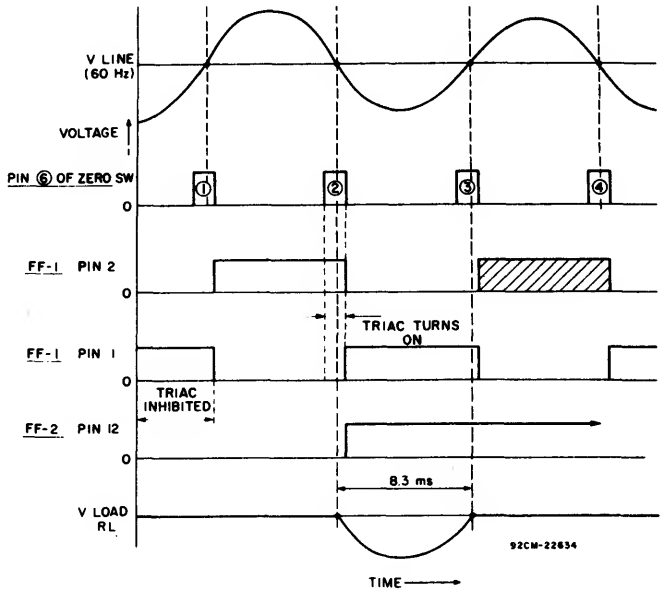

Fig. 56 – Timing diagram for the power one-shot control.

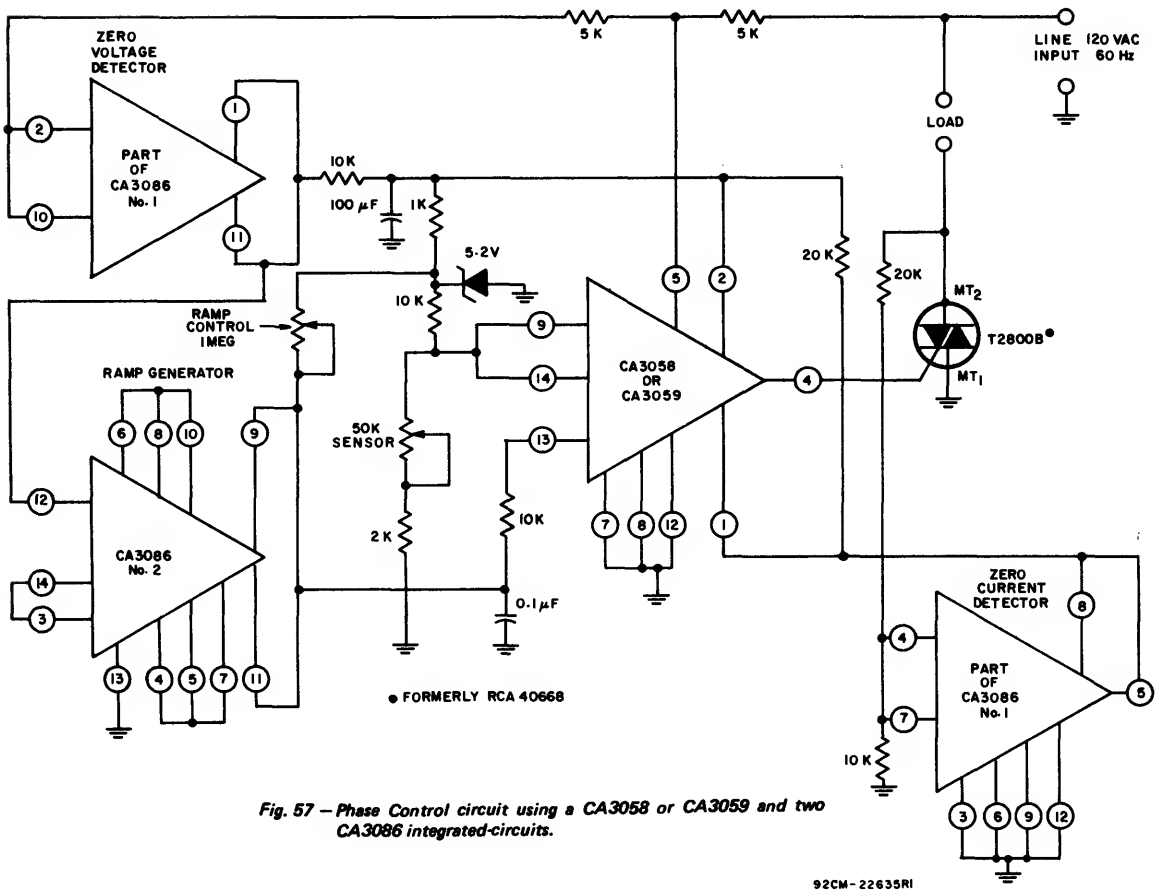

Fig. 57 – Phase Control circuit using a CA3058 or CA3059 and two CA3086 integrated-circuits.

PHASE CONTROL CIRCUIT

Fig. 57 shows a circuit using a CA3058 or CA3059 zero-voltage switch together with two CA3086 integrated-circuit transistor arrays to form a phase-control circuit. This circuit is specifically designed for speed control of ac induction motors, but may also be used as a light dimmer. The circuit, which can be operated from a line frequency of 50-Hz to 400-Hz, consists of a zero-voltage detector, a line-synchronized ramp generator, a zero-current detector, and a line-derived control circuit (i.e., the zero-voltage switch). The zero-voltage detector (part of CA3086 No. 1) and the ramp generator (CA3086 No. 2) provide a line-synchronized ramp-voltage output to terminal 13 of the zero-voltage switch. The ramp voltage, which has a starting voltage of 1.8 volts, starts to rise after the line voltage passes the zero point. The ramp generator has an oscillation frequency of twice the incoming line frequency. The slope of the ramp voltage can be adjusted by variation of the resistance of the 1-megohm ramp-control potentiometer. The output phase can be controlled easily to provide 180° firing of the triac by programming the voltage at terminal 9 of the zero-voltage switch. The basic operation of the zero-voltage switch driving a thyristor with an inductive load was explained previously in the discussion on switching of inductive loads.

ON/OFF TOUCH SWITCH

The on/off touch switch shown in Fig. 58 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the on plate is touched, current flows between the two halves of the grid, causing a positive shift in the output voltage (terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at terminal No. 7 of the CA3240E, the triac is turned on and held on by the CA3059 and associated positive feedback circuitry (51-kilohm resistor and 36-kilohm/42-kilohm voltage divider). When the pulse occurs at terminal No. 1, the triac is turned off and held off in a similar manner. Note that power for the CA3240E is derived from the CA3059 internal power supply. The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while maintaining sufficiently high circuit impedance to protect against electrical shock.

TRIAC POWER CONTROLS FOR THREE-PHASE SYSTEMS

This section describes recommended configurations for power-control circuits intended for use with both inductive and resistive balanced three-phase loads. The specific design requirements for each type of loading condition are discussed.

In the power-control circuits described, the integrated-circuit zero-voltage switch is used as the trigger circuit for the power triacs. The following conditions are also imposed in the design of the triac control circuits:

1. The load should be connected in a three-wire configuration with the triacs placed external to the load; eiter delta or wye arrangements may be used. Four-wire loads in wye configurations can be handled as three independent single-phase systems. Delta configurations in which a triac is connected within each phase rather than in the incoming lines can also be handled as three independent single-phase systems.
2. Only one logic command signal is available for the control circuits. This signal must be electrically isolated from the three-phase power system.
3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio-frequency interference (RFI) that may be generated.

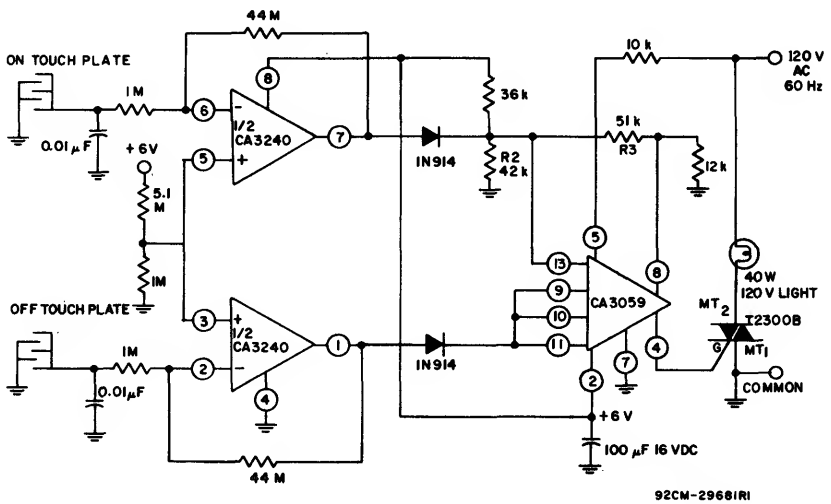

Fig. 58 – On-off touch switch.

Isolation of DC Logic Circuitry

As explained earlier under **Special Application Considerations**, isolation of the dc logic circuitry* from the ac line, the triac, and the load circuit is often desirable even in many single-phase power-control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the dc logic circuitry cannot be referenced to a common line in all phases.

In the three-phase circuits described in this section, photo-optic techniques (i.e., photo-coupled isolators) are used to provide the electrical isolation of the dc logic command signal from the ac circuits and the load. The photo-coupled isolators consist of an infrared light-emitting diode aimed at a silicon photo transistor, coupled in a common package. The light-emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500 volts. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

Resistive Loads

Fig. 59 illustrates the basic phase relationships of a balanced three-phase resistive load, such as may be used in heater applications, in which the application of load power is controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three-wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single-phase circuit which is out of phase with both of its component phases. The single-phase circuit leads one phase by 30 degrees and lags the other phase by 30 degrees.

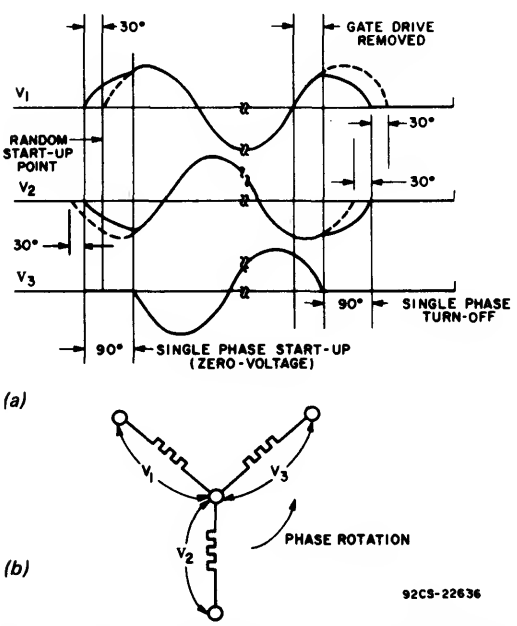

Fig. 59 – Voltage phase relationship for a three-phase resistive load when the application of load power is controlled by zero-voltage switching: (a) voltage waveforms, (b) load-circuit orientation of voltages. (The dashed lines indicate the normal relationship of the phases under steady-state conditions. The deviation at start-up and turn-off should be noted.)

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady-state operating condition, the system must first be turned on, by zero-voltage switching, as a single-phase circuit and then must revert to synchronous three-phase operation.

Fig. 60 shows a simplified circuit configuration of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo-coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100 microseconds in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three-phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current-limiting resistors R4, R5, and R6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three-wire load and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three-wire load. Because only one triac is pulsed on at a time, the diodes (D1, D2, and D3) are necessary to trigger the opposite-polarity triac, and, in this way, to assure initial latching-on of the system. The three resistors (R1, R2, and R3) are used for current limiting of the gate drive when the opposite-polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Fig. 61 may be used. In addition to synchronous steady-state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start-up condition is zero-voltage synchronized to a single-phase, 2-wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single-phase start-up zero-voltage switch and three-phase photo-coupled isolators OC13, OC14, OC15 through the photo-coupled

* The dc logic circuitry provides the low-level electrical signal that dictates the state of the load. For temperature controls, the dc logic circuitry includes a temperature sensor for feedback. The RCA integrated-circuit zero-voltage switch, when operated in the dc mode with some additional circuitry, can replace the dc logic circuitry for temperature controls.

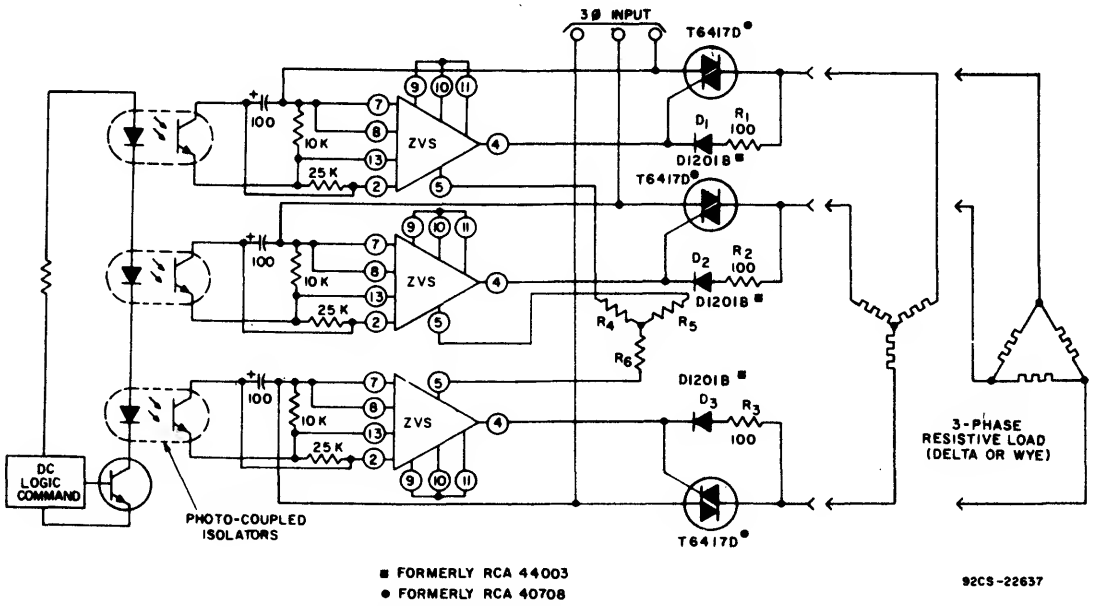

Fig. 60 – Simplified diagram of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating conditions.

isolators OC11 and OC12. The single-phase zero-voltage switch, which is synchronized to phases A and B, starts the system at zero voltage. As soon as start-up is accomplished, the three photo-coupled isolators OC13, OC14, and OC15 take control, and three-phase synchronization begins. When the "logic command" is turned off, all control is ended, and the triacs automatically turn off when the sine-wave current decreases to zero. Once the first phase turns off, the other two will turn off simultaneously, 90° later, as a single-phase line-to-line circuit, as is apparent from Fig. 59.

Inductive Loads

For inductive loads, zero-voltage turn-on is not generally required because the inductive current cannot increase instantaneously; therefore, the amount of RFI generated is usually negligible. Also, because of the lagging nature of the inductive current, the triacs cannot be pulse-fired at zero voltage. There are several ways in which the zero-voltage switch may be interfaced to a triac for inductive-load applications. The most direct approach is to use the zero-voltage switch in the dc mode, i.e., to provide a continuous dc output instead of pulses at points of zero-voltage crossing. This mode of operation is accomplished by connection of terminal 12 to terminal 7, as shown in Fig. 62. The output of the zero-voltage switch should also be limited to approximately 5 milliamperes in the dc mode by the 750-ohm series resistor. Use of a triac such as the T2301D* is recommended for this application. Terminal 3 is connected to terminal 2 to limit the steady-state power dissipation within the zero-voltage switch. For most three-phase inductive load applications, the current-handling capability of the 40692 triac (2.5 amperes) is not sufficient. Therefore, the 40692 is used as a trigger triac to turn on any other currently available power triac that may be used. The trigger triac is used only to provide trigger pulses to the gate of the power triac (one pulse per half cycle); the power dissipation in this device, therefore, will be minimal.

Simplified circuits using pulse transformers and reed relays will also work quite satisfactorily in this type of application. The RC networks across the three power triacs are used for suppression of the commutating dv/dt when the circuit operates into inductive loads.

The specific integrated-circuits, triacs, SCR's, and rectifiers included in circuit diagrams shown in this Application Note are listed below. Additional information on these devices can be obtained by requesting the applicable RCA data-bulletin file number.

Type No.	File No.
CA3058, CA3059, and CA3079	490
CA3099E	620
CA3086	483
CA3080	475
CD4007A, CD4013A	479
2N5444	456
T2800B (40668)	364
T2300B (40526)	470
T2301B (40691), T2301D (40692)	431
T64170 (40708)	406
S2600D (40655)	496
D1201B (44003)	495
D3202U (45412)	577

Note: Numbers in parenthesis (e.g. 40668) are former RCA type numbers.

* Formerly RCA 40692

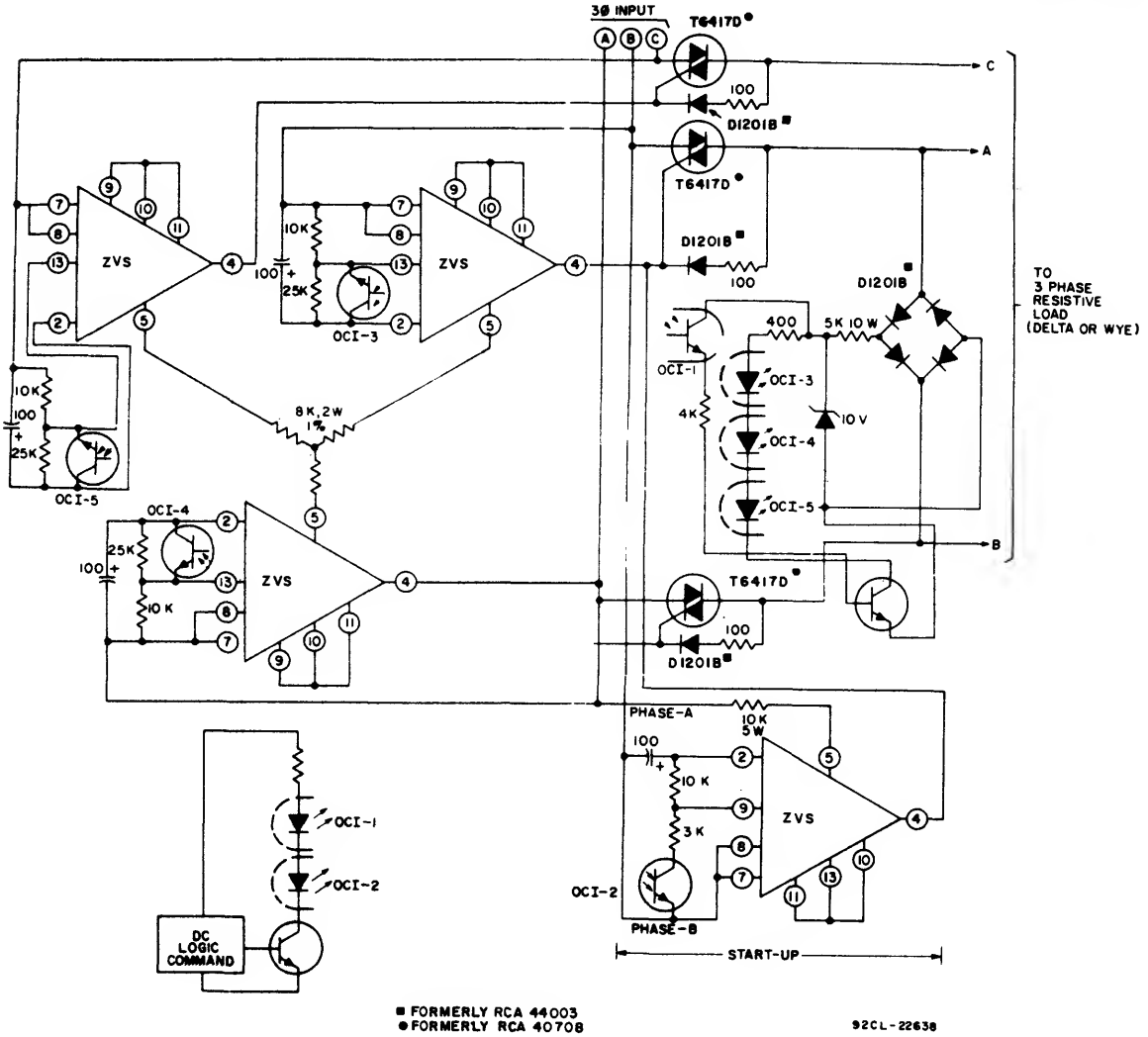

Fig. 61 — Three-phase power control that employs zero-voltage synchronous switching both for steady-state operation and for starting.

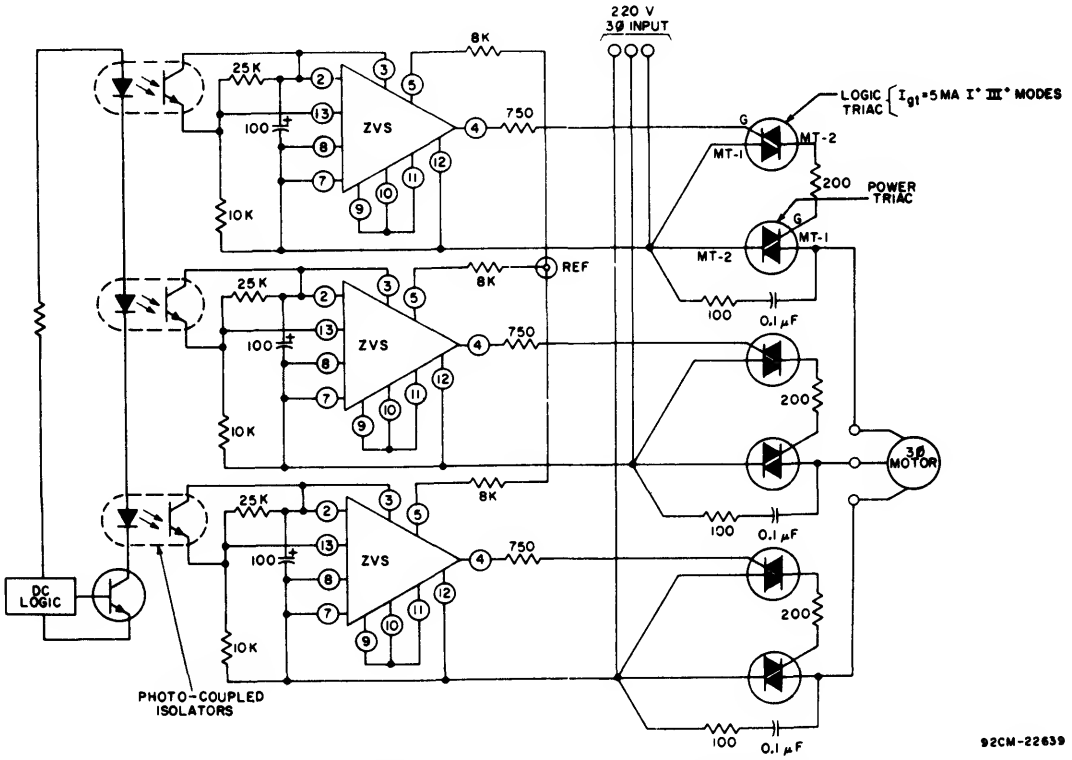

Fig. 62 – Triac three-phase control circuit for an inductive load, i.e., three-phase motor.

Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note* describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

As contrasted with prior state-of-the-art IC designs, sample-and-hold techniques are used in the phase detectors for the AFPC and the ACC-killer loops of the CA3126Q. The improved signal-to-dc unbalance attained thereby makes it possible to eliminate the adjustments conventionally used in those circuits. The only set-up adjustment is a trimmer capacitor to tune the crystal filter.

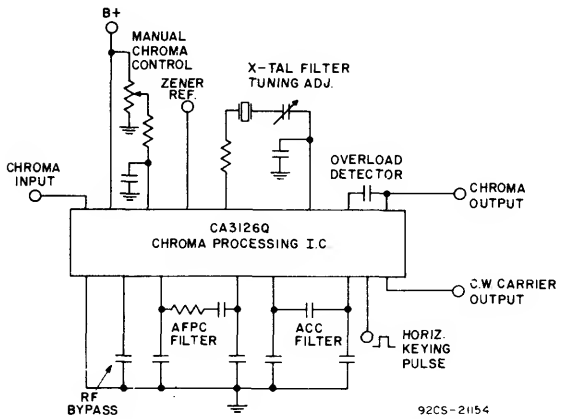

Fig. 1– Components external to the CA3126Q.

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Two controls serve to adjust the chroma level: One control is automatic and functions as a supplementary ACC loop to prevent oversaturation under condition of improper transmitted burst-to-chrominance ratio, and under noisy-signal conditions. The second chroma level control is for manual adjustment of the saturation by the viewer. This control has a linear characteristic over the range of the chroma gain control.

The CA3126Q integrated circuit which performs these functions is housed in a 16-terminal package. The external components, shown in Fig. 1, are relatively few and consist of integration capacitors for the servo loops and the filter network in the VCO. Table I summarizes the performance of the circuit.

Table I – Performance Data Typical Values

Function	Nom. Supply V_{CC} = 11.2 V	Supply Var. V_{CC} ±2 V	Temp. Var. ΔT = 50°C
Oscillator Characteristic			
C. W. Carrier Ampl.	1 V_{pp}	±5%	+ 10%
Frequency	Nom. Sub Carrier	∓70 Hz	−70 Hz
AFPC Characteristic			
DC Loop Gain	40 Hz/deg.		
Pull-in Range	±500 Hz		
Phase Error		∓2°	−2°
Noise Bandwidth f_{NN}	100 Hz		
ACC and Killer Characteristic			
100% Input Level (Red Field)	0.25 V_{pp}		
Nominal Output with Overload Detector	0.5 V_{pp}	±2.5%	−5%
Nominal Output without Overload Detector	2.7 V_{pp}	±10%	−5%
ACC–3 dB Point	20% E_{IN}		
Killer Threshold	5% E_{IN}		
Diff. Phase Error Over Entire ACC Range	1°		
Manual Control Characteristic			
Chroma Output Linearly Proportional to Control Bias			
Diff. Phase Shift with Bias Var.	2°		

MAJOR FUNCTIONS

The signal flow and organization of the CA3126Q are shown in block form in Fig. 2. The composite chroma signal is applied to the first chroma amplifier. The output from this stage proceeds along three paths. The first path leads to the doubly-balanced wide-band AFPC detector. Here the burst signal is compared with the reference carrier to produce the required error signal for synchronization. Two sample-and-hold circuits serve to achieve high detection efficiency and bias stability. One sample-and-hold circuit samples the detected signal during the horizontal keying interval and stores the peak error signal in a filter capacitor. A second similar circuit provides an accurate reference potential as described later. The bias stability of this system is sufficient to eliminate the need for the adjustments required in conventional circuit design.

The detected and filtered burst signal controls the frequency and phase of a voltage-controlled oscillator (VCO) by operating on an electronic phase-shifter. The VCO consists of an amplifier-limiter followed by the electronic phase-shifter. A crystal filter located between the output of the phase-shifter and the input of the amplifier-limiter closes the loop of the VCO. The filtered oscillator signal is amplified to produce the required reference carriers for the AFPC and ACC synchronous detectors. The required quadrature relationship is obtained by $+\pi/4$ and $-\pi/4$ radian integrated phase-shift networks.

The ACC-killer detector is similar in structure to the AFPC detector, and is also driven from the first chroma amplifier stage. It detects synchronously the in-phase component of the burst signal and produces a pulse signal proportional in amplitude to the level of the burst signal. The resulting control signal passes through a sampling circuit, as described above, and is applied to the killer and ACC amplifiers. The action of both amplifiers is delayed so that the unkill action takes place prior to ACC and the latter is fully activated upon reaching the predetermined burst level. The ACC amplifier controls the gain of the first chroma amplifier so as to maintain the burst signal constant while the killer amplifier enables the output stage in the presence of the burst signal.

The signal level to the second chroma amplifier is reduced to one fourth of the available signal level to allow for the extremes of the chroma signal excursions. A horizontal rate keyer operating on this stage removes the burst signal so that the output stage is activated only during the horizontal scanning interval. A saturation control, available for front panel control, allows a continuous gain adjustment of this amplifier. A desirable feature of this control is the linear correspondence between the control bias and the chroma output signal. The chroma maximum level corresponds to the maximum bias potential without a dead spot at the extreme of the control range. A threshold type overload detector monitors the output signal and maintains the output from the second chroma amplifier below an arbitrarily set level. This prevents the overload of the picture tube usually experienced on noisy or excessively large chroma signals. The required keying signals for the various functions are generated by two cascaded keyer stages where either polarity pulses are generated.

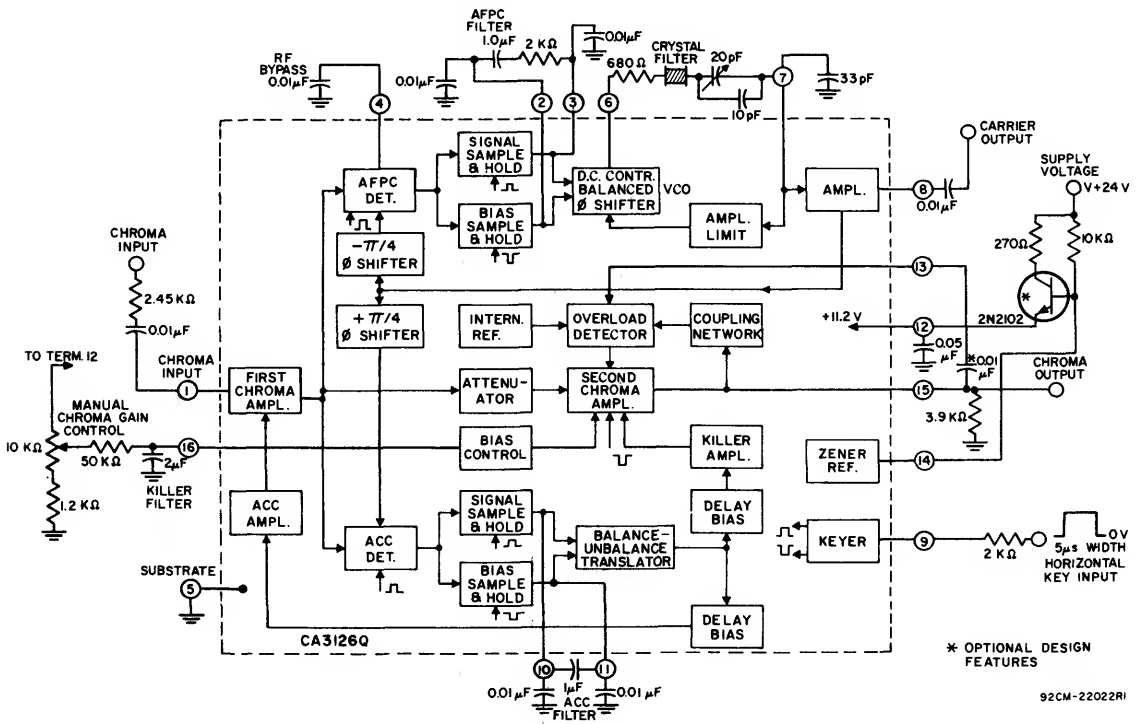


Fig. 2— Signal flow and organization of the CA3126Q.

REGENERATION OF THE SUBCARRIER

The regeneration of the subcarrier is performed in the circuit shown in Fig. 3. This section consists of a synchronous phase detector, the sample-and-hold circuits, and a voltage-controlled oscillator. Several keying circuits serve to maintain the operation in proper time sequence.

The Phase Detector

The phase detector is formed by transistors Q_{51}, Q_{52} and Q_5 to Q_{10}. The composite chroma signal amplified by the first chroma amplifier is applied to transistors Q_7 and Q_8 and the reference carrier is applied to transistors Q_9 and Q_{52}. The product of the two signals is developed across the load resistor R_{13}. Transistors Q_5 and Q_6, triggered by a horizontal rate keyer circuit, operate on the phase detector so as to allow detection of the burst signal only. The current compensation of transistors Q_7 and Q_8 by the gating transistors Q_5 and Q_6 and the absence of filtering at the output of the detector results in transient-free switching of the phase detector. In the absence of chrominance, the potential across the load resistor R_{13} remains constant regardless of the keying. In the presence of the chrominance signal, the phase detector produces two time-spaced outputs: one during the horizontal scanning interval corresponding to the quiescent potential, the second during the horizontal keying interval representing the detected burst. Thus, the detected burst can be measured relative to the quiescent potential rather than to an arbitrary reference. This results in excellent stability for temperature and supply variations.

Sample-and-Hold Circuits

As previously stated, the sample-and-hold circuits shown in Fig. 3 allow efficient utilization of the detected error signal and provide a reliable reference potential. During the sampling interval, the detected pulse signal available at the detector load resistor R_{13} is translated to the AFPC filter capacitor of terminal 2 via transistors Q_{53} and Q_{54}. Q_{53} serves to isolate the detector from the switching pulses generated in the sampling circuits. The sample-and-hold action is accomplished by controlling the conduction current in transistor Q_{54} thus alternating the charge path during those intervals. During the sampling interval, transistor Q_{54} conducts and its emitter exhibits a relatively low impedance in comparison with the value of the integrated charging resistor R_{20}. The detected or sampled signal is stored in the AFPC filter capacitor which, with R_{20}, determines the time constant during this time interval. During the hold period, transistor Q_{54} is off and the filter time constant is several orders of magnitude larger than previously. The discharge of the filter capacitor is reduced to very small base bias currents only and little of the stored information is lost.

The "on" and "off" condition of the transistor Q_{54} is determined by the state of the transistor-pair Q_{11} and Q_{12}. During the "on" (sampling) interval, a signal from the horizontal rate keyer disables transistor Q_{11} and the collector current of the transistor Q_{12} maintains the transistor Q_{54} in the "on" condition. During the "off" (hold) period, transistors Q_{11} and Q_{12} change their states and the transistor Q_{54} is "off".

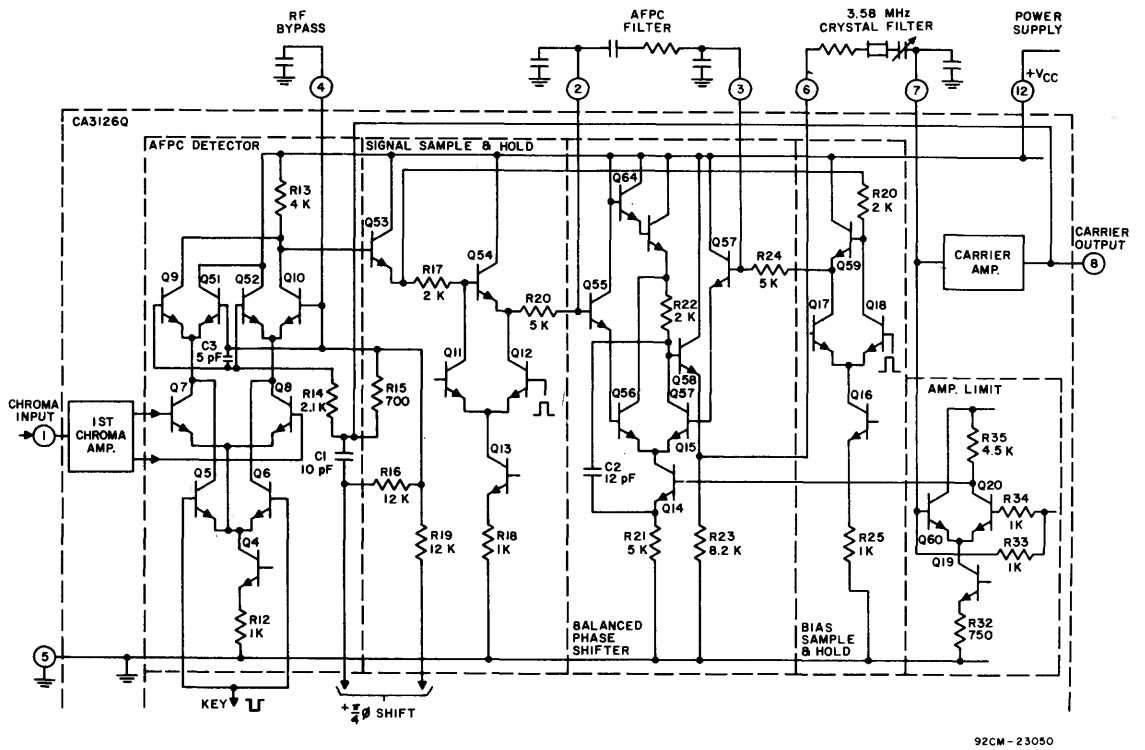


Fig. 3— Subcarrier regeneration circuit.

The bias sample-and-hold circuit, similar in structure to the above-described circuit, consists of the sampling switch Q_{59} and the transistor-pair Q_{17} and Q_{18}. This circuit, also activated by a signal from a horizontal rate keyer, samples the quiescent potential of the phase detector. The two signals, the error and the bias, processed by the sampling circuits, are stored in filter capacitors, and are applied to opposite terminals of a differential phase control. The phase control circuit synchronizes the reference carrier produced by the VCO.

Depending on the free-running frequency of the VCO, the detected signal is in the form of positive or negative going pulse trains which are then stored in a filter capacitor. The sampling switch has equal drive capabilities for both polarities of the signal; a requirement of particular importance in the presence of noise signals. Non-linear operation of the detector and sampling circuit would produce a rectified dc component causing an erroneous detuning of the VCO.

The VCO Loop

The amplification and amplitude limiting of the oscillator signal takes place in the amplifier-limiter formed by the transistor-pair Q_{60} and Q_{20}. The output from Q_{20} is fed to the dc controlled phase-shifter and returns to the amplifier through a crystal filter. The amplifier operates in a non-inverting mode, hence, the total phase shift through the phase-shifter plus crystal filter must be a multiple of 2π radians. The crystal filter is tuned to the subcarrier frequency and the filter band-width is determined by a resistor in series with the crystal. The DC controlled phase-shifter has a phase range of approximately $\pm \frac{\pi}{4}$ radians, and a phase change activated by a control signal results in a corresponding oscillator frequency change.

In the phase-shifter, the oscillator signal available at the collector of Q_{20} is applied to the base of Q_{14} from which it proceeds along two paths. An integrated capacitor C_2 couples this signal from the emitter of Q_{14} to the collector load of Q_{15} and, at this point, the signal is phase-shifted by approximately $\pi/4$ radians. In the second path, the signal arriving at the collector of Q_{15} passes through a current splitter formed by the transistor-pair Q_{56}, Q_{15}. This signal is reduced to a level determined by the control voltage at the bases of transistors Q_{56} and Q_{15}. At one extreme, transistor Q_{15} is OFF and the signal at the collector of Q_{15} arrives through the capacitor C_2 only. Conversely, with transistor Q_{15} ON, and Q_{56} OFF, the signal arriving through the transistor Q_{15} is phase-oriented so that the resultant signal has a phase of $+3/4\ \pi$ radians. The phase-control is linear throughout most of the control range.

A buffer amplifier is used to supply the CW carrier required for the demodulators, and the carrier is available at terminal 8. Internally, the buffer amplifier supplies the two synchronous detectors. Two R-C phase-shifters fed from the buffer amplifier provide the required phase orientation. A low-pass R_{14}-C_3 filter shifts the carrier to the AFPC detector by $-\pi/4$ while a high-pass filter provides a $+\pi/4$ oriented carrier for the ACC-killer detector.

AMPLITUDE CONTROL OF THE CHROMINANCE SIGNAL

Two cascaded amplifier stages serve to process the chroma signal and several signals are developed to control the gain of each stage.

First Chroma Amplifier and ACC Servo Loop

The first chroma amplifier, shown in Fig. 4, is controlled by the burst responsive ACC-killer detector only. The amplifier formed by the transistor-pair Q_1, Q_2 is driven single-ended by the applied composite chroma signal. The amplified output from this stage drives differentially the synchronous ACC-killer detector. The gain of the first amplifier is a function of the dc emitter current supplied by the constant current source Q_3. This current source is biased to provide a nominal current and, hence, a nominal gain in the first amplifier stage. The bias of the current source is reduced in response to a detected burst signal and the gain of the first stage diminishes correspondingly.

The ACC-killer detector is similar in structure to the AFPC detector. However, the CW carrier applied to the detector is in phase with the burst signal. The detected burst signal is processed by a sampling circuit in the same manner as previously described in connection with the AFPC circuit. The signal sampling consists of the transistor follower Q_{73} and the keyed transistor-pair Q_{40}, Q_{41}. Resistor R_{63} serves to produce an intentional dc offset across the inputs of the differential pair Q_{43}, Q_{76}. The detected ACC signal is unipolar with respect to the reference potential; thus, the dc offset extends the linear operating range of the amplifier Q_{43}, Q_{76}. The bias sampling circuit consisting of transistors Q_{79}, Q_{44}, Q_{45} applies the quiescent bias to the base of transistor Q_{76}. In the absence of a burst signal, the dc offset maintains transistor Q_{43} in the OFF condition and the following p-n-p transistor, Q_{29}, is also disabled. Thus, the ACC amplifier Q_{28} is non-conducting and the current source Q_3 provides the maximum current to the input stage.

The OFF state of transistor Q_{29} renders the killer amplifier (transistor Q_{27}) inoperative, a condition required to disable the second chroma stage.

Upon amplification of the burst signal in the first chroma amplifier, the detected burst signal increases proportionately to the amplitude of the input signal and combines differentially with the previously described bias signal in the collector load of transistor Q_{43}. Prior to it, the detected and bias signals are smoothed by the ACC filter capacitors. The linear operation of the chroma amplifier, the detector, and the amplifier which follows the sampling circuits is maintained to a signal level sufficient to enable the transistor Q_{28}. This potential, approximately 0.7 V, establishes the delay of the ACC charac-

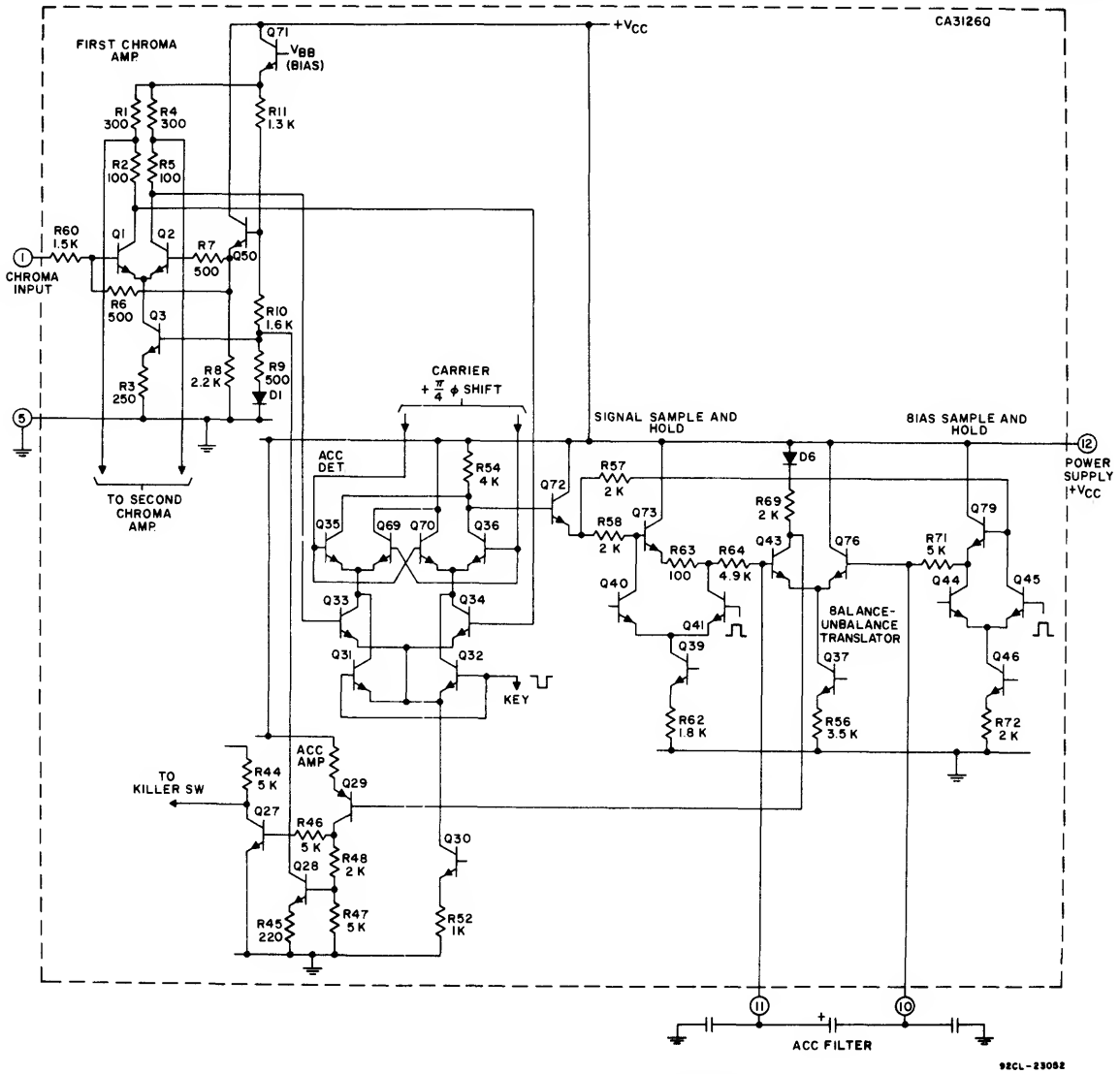


Fig. 4– The first chroma amplifier and the ACC servo loop.

teristic as shown in Fig. 5. The chroma (burst) signal at the output of the first stage remains essentially constant with further increase of the input signal. The increasing dc potential at the collector of Q_{29} also activates the killer-amplifier Q_{27}. In order to maintain a predictable killer threshold, this action is referenced to the delay point of the ACC. As previously stated, the ACC begins to function at a signal level at which the dc potential across resistor R_{47} reaches 0.7 V. The killer threshold is lower than that of the ACC action and is determined by the voltage drop across resistors R_{48} and R_{47}. Thus, the two threshold signals are predictably established by the ratio $R_{47}/(R_{47} + R_{48})$.

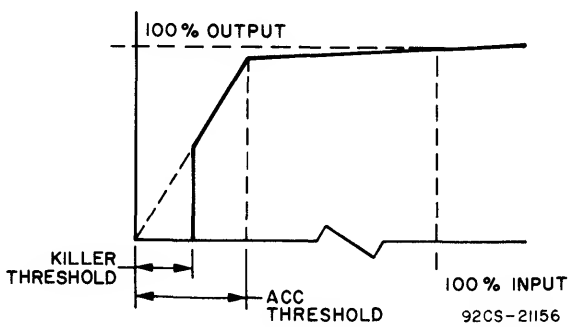


Fig. 5– Normalized ACC characteristic.

The Second Chroma Amplifier

The operation of the second chroma amplifier is controlled simultaneously by several signals. As described previously, they are: a customer-operated chroma gain (saturation) control, the killer detector signal, the overload detector, and the keyer.

The amplifier circuit shown in Fig. 6 is formed by the transistor-pair Q_{65}, Q_{24} and is driven differentially by the first chroma amplifier. The signal level to this stage is reduced by means of a resistive voltage divider. The amplifier Q_{65},Q_{24} is interrupted during the horizontal keying interval by the transistor-pair Q_{66}, Q_{23} to remove the burst information from the composite signal. The gating transistors Q_{66} and Q_{23} are connected so that their emitters and collectors are in parallel with the respective emitters and collectors of transistors Q_{65} and Q_{24}. The resulting collector current compensation maintains the quiescent output potential regardless of the keying operation.

The gain of the second chroma amplifier is adjusted by varying the current in the transistor Q_{25}. A resistive divider R_{41},R_{42} fed from a follower stage Q_{67} provides the bias potential to the base of the transistor Q_{25} and the voltage drop across resistor R_{40} determines the current flowing from the collector of Q_{25} to the emitters of Q_{65} and Q_{24}. The diode D_3 compensates the base to emitter potential of the transistor Q_{25}.

Since the bias resistors R_{40}, R_{41}, and R_{47}, and also the amplifier load resistor R_{43}, are located on the same IC chip, the resistance ratio of these components is accurately controlled. Thus, the gain of the second chroma amplifier determined by these components is very predictable, and is a function of the bias potential applied to the base of transistor Q_{67} only.

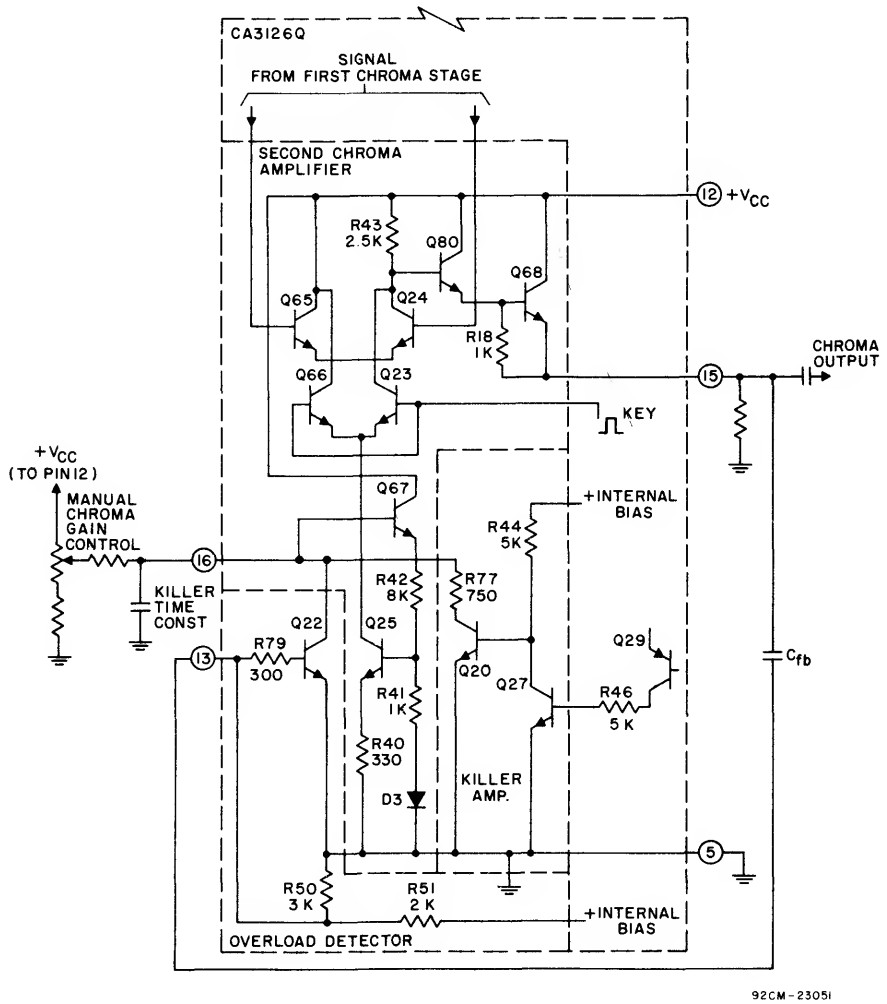


Fig. 6— Chroma output stage.

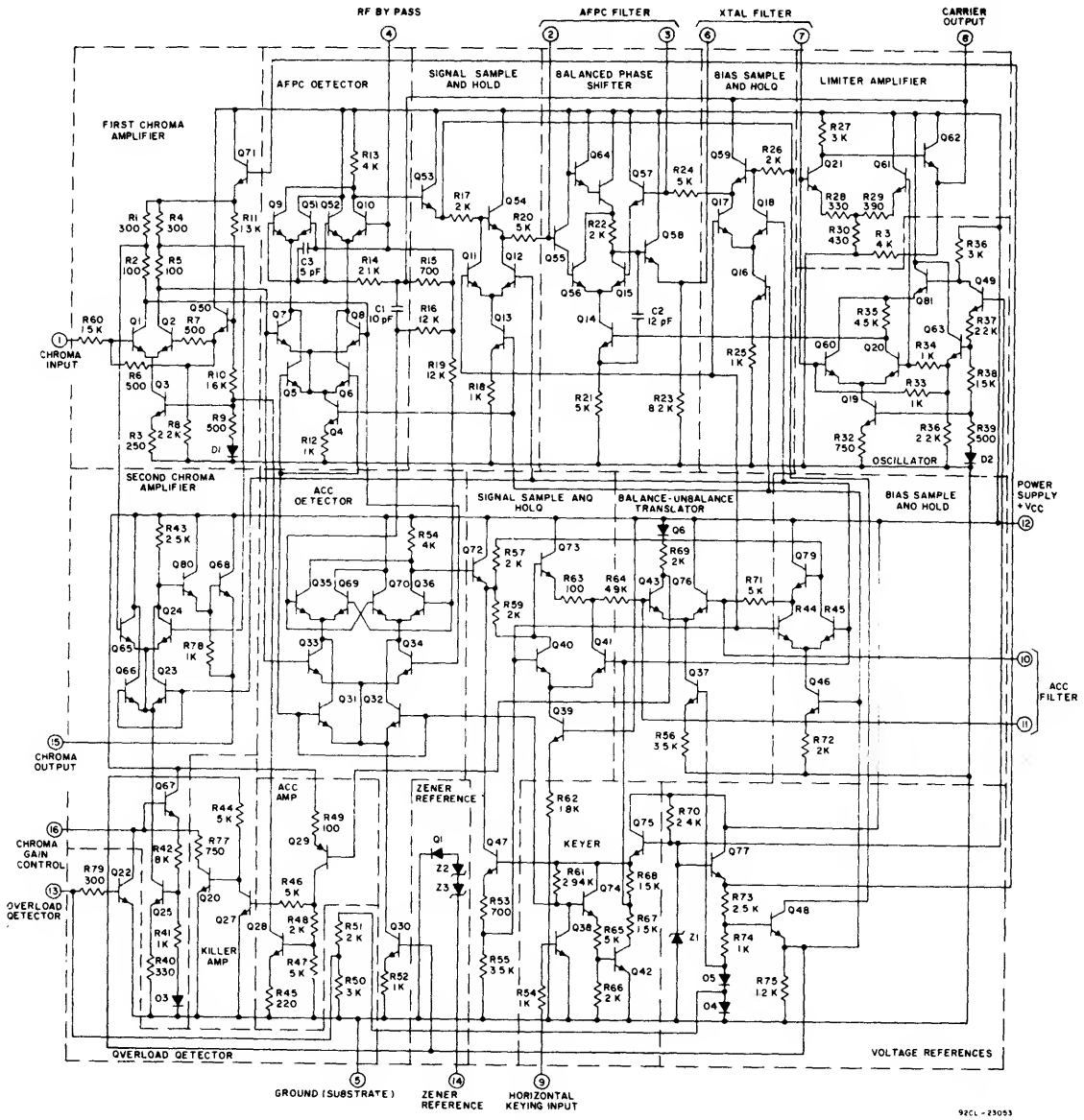


Fig. 7– Complete circuit diagram showing details of the keying circuit and internal bias circuits.

The interfacing of IC's with external control circuits usually presents problems due to the large tolerances associated with both components. The circuit used here overcomes these difficulties. The transistor follower Q_{67} exhibits negligible loading on the bias set by the manual chroma control. Thus, the gain of the second chroma amplifier is uniquely determined by the rotation of the gain control potentiometer and is relatively independent of its resistance value.

The killer operation is also performed on the second chroma amplifier. The amplified output from the ACC-killer detector is applied to the killer switch Q_{20}. In the presence of a burst signal, transistor Q_{20} is off and the chroma amplifier remains undisturbed. In the absence of a burst signal, the collector current in Q_{20} reduces the potential on the base of the transistor Q_{67} so as to cut off the second chroma amplifier.

The Overload Detector

The ACC and the manually operated saturation control provide the essential means to maintain the proper chrominance level to the picture tube. Under certain conditions, however, the presence of the ACC is detrimental. As previously stated, the ACC servo loop maintains a constant output level of the burst signal regardless of the chroma information. Transmitter variations in burst-to-chroma ratios are improperly corrected by the ACC action and, on signals with low burst-to-chroma ratios, the excessively amplified chroma can exceed the dynamic range of the picture tube.

Similar overload problems are experienced when receiving weak signals. The Synchronous ACC detector produces a control signal proportional to the average value of the burst interval signal, and noise does not contribute to the output. Although this type of noise-immune detection is necessary for reliable operation of the killer circuits, it is less desirable for the ACC action because the noise-peaks plus signal tend to produce undesirable over-saturation effects.

The overload detector operating on the second chroma stage eliminates both these overload problems. The chroma signal from the output terminal of the second chroma amplifier is coupled, by means of the coupling capacitor C_{fb} to overload detector Q_{22}. Transistor Q_{22} is biased by means of an internal bias supply to 0.5 V, and remains off until its base potential is raised to approximately 0.7 V. Thus, detection takes place whenever the chroma signal plus dc bias is equal to or exceeds 0.7 V. The detected and filtered signal lowers the bias potential on the base of transistor Q_{67} and reduces the gain of the output stage.

KEYING CIRCUITS

Details of the keying circuit and of the internal bias circuits are shown in the complete diagram of the CA3126Q in Fig. 7. A positive horizontal rate keying pulse applied to terminal 9 activates the keying circuit. This circuit maintains the AFPC and ACC detectors, with the corresponding sample-and-hold circuit, in the ON position during the keying interval, and disables the chroma output stage at the same time.

CONCLUSION

The new chroma processing circuit improves the performance of a color television receiver. The use of synchronous detection and sampling results in excellent signal stability and fewer external components and adjustments. An overload detector prevents over-saturation of the picture tube, and the improved manual control simplifies the adjustment of the chroma level.

Application of the CA3089E FM-IF Subsystem

by L. S. Baar

The RCA-CA3089E, shown in Fig. 1, is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC.[1] This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

Circuit Description

The three-stage direct-coupled amplifier-limiter uses a cascode input stage to reduce input noise and provide better stability. The peak-to-peak swing of approximately 300 millivolts is developed across the 390-ohm resistor, R31, at pin 8. The operating-point stability is provided by dc feedback to the input stage. The input voltage for an output 3 dB below limiting is typically 12 microvolts rms.

The detector is a doubly balanced circuit driven symmetrically by the output of the if amplifier. The voltage at pin 8 is coupled through a reactance to the tuned circuit at pin 9. The detector output is taken from both sides and combined differentially to produce an audio output and automatic-frequency-control voltage. The audio output may be attenuated by a current driving pin 5. The current is

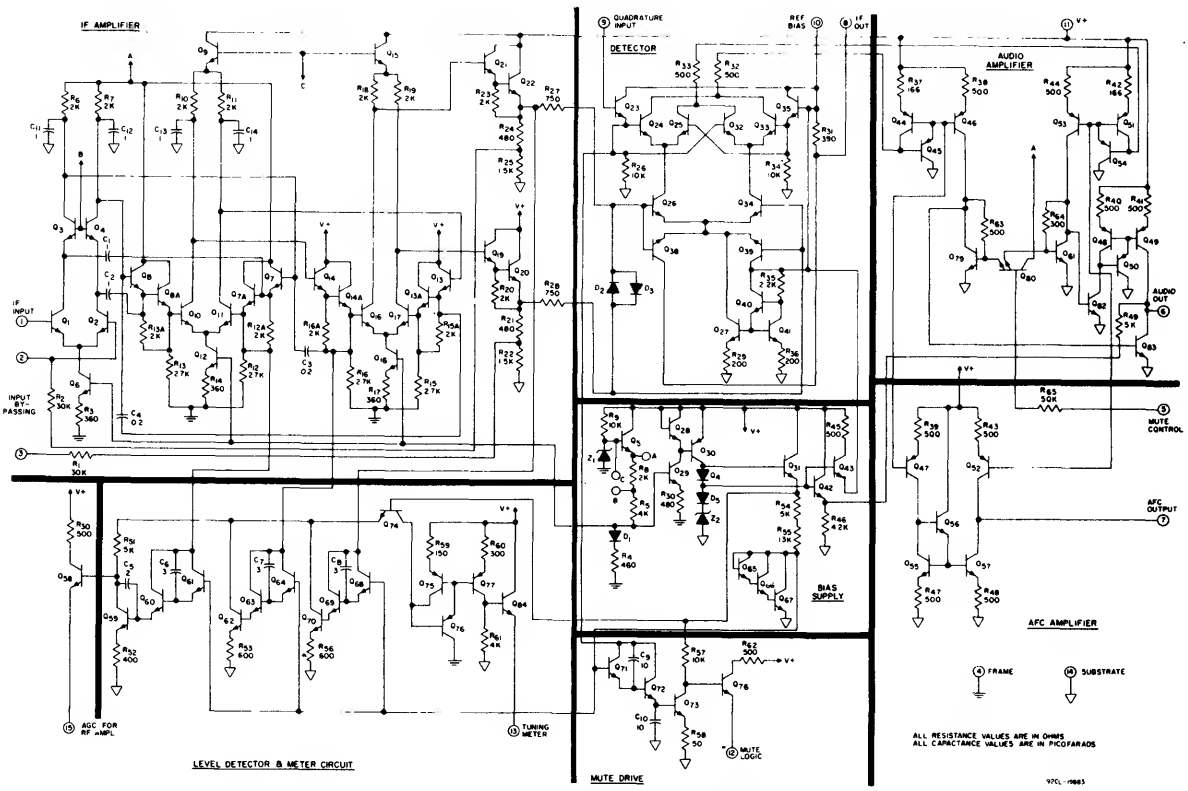


Fig. 1— Schematic diagram of the CA3089E.

normally provided by the mute drive, which reduces the level by more than 50 dB. Fig. 2 shows the detector and audio-AFC translator circuits redrawn to illustrate the balanced circuitry. The audio output is developed across a 5,000-ohm resistor, R49, Fig. 1. The AFC output can be used either as a current or voltage source.

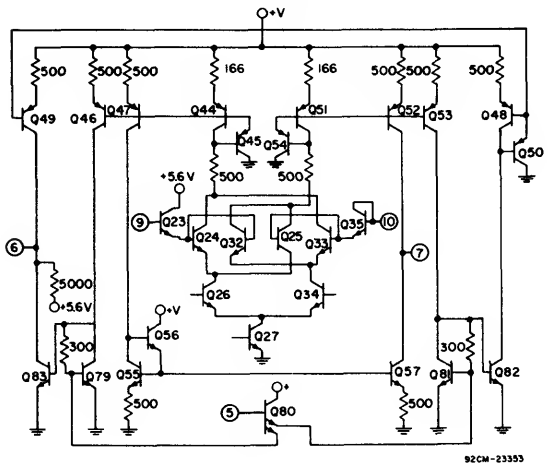


Fig. 2– Detector, audio, and AFC circuits.

The meter output and rf-AGC circuits are driven by three level detectors which detect the output levels of each of the if amplifier stages. The tuning-meter circuit sums these levels and provides a voltage which is a function of the input signal. The rf-AGC circuit is driven by the level detector connected to the output of the first amplifier stage, which provides the delay. The mute logic output is developed from the output of the third limiter. With a large signal, the if envelope is detected, and drives the mute logic voltage low. As the signal-to-noise ratio deteriorates, "holes" are created in the envelope; these "holes" are detected, and provide the voltage to drive pin 5.

The bias supply maintains the device current drain virtually constant from a supply voltage of 16 volts to approximately 8 volts over a temperature range of –40°C to +100°C while maintaining the performance of the device virtually unchanged. The typical curves in Figs. 3 through 7 illustrate these characteristics. A reference voltage brought out to pin 10 may be used in conjunction with the AFC, if desired.

Stability Considerations

Because the CA3089E is a very high gain device, the external circuit must be laid out carefully to eliminate or reduce any feedback path.[2] Fig. 8 shows a 10.7-MHz printed-circuit-board layout of the circuit in Fig. 9(a). The ground-plane layout was devised to prevent large rf currents at the output terminals from returning to the input grounds. Bypass-capacitor grounds also were selected to achieve the same purpose. It is recommended that bypass capacitors be placed on terminals of the auxiliary functions since most of

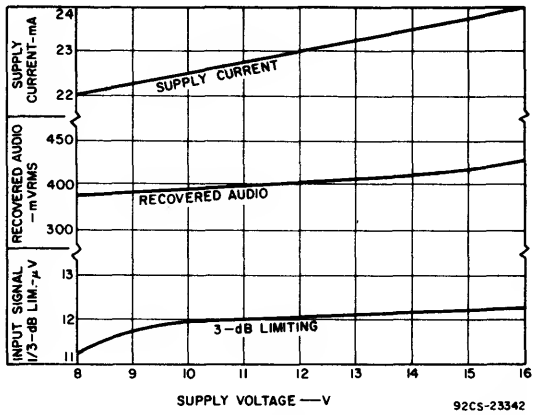


Fig. 3– Supply current, recovered audio, and input limiting as a function of supply voltage.

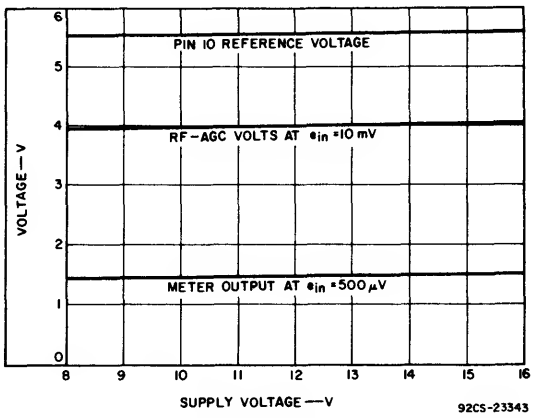


Fig. 4– Reference voltage, rf-AGC, and meter output as a function of supply voltage.

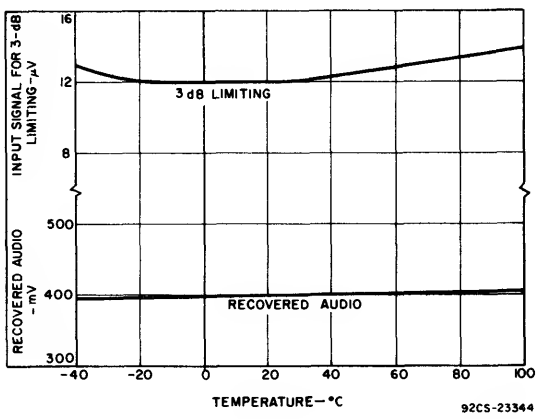


Fig. 5– Input limiting and recovered audio as a function of temperature.

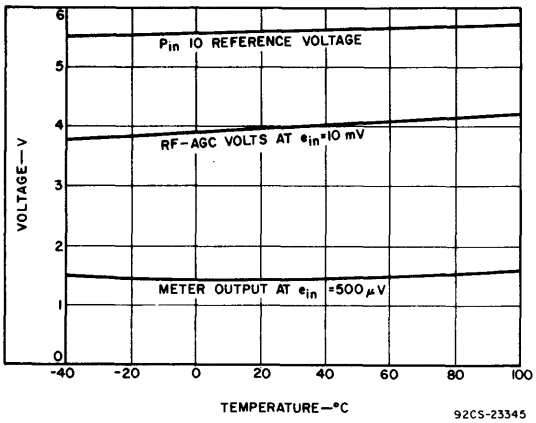


Fig. 6— Reference voltage, rf-AGC, and meter output as a function of temperature.

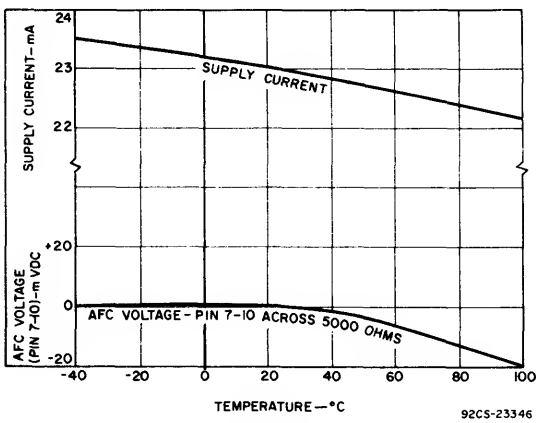


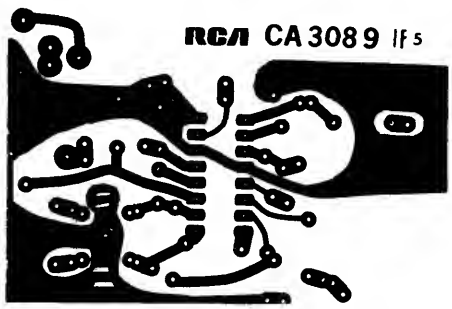
Fig. 7— Supply current and AFC voltage as a function of temperature.

them are connected to rectifier circuits which are not completely filtered within the device. Capacitors of the disc ceramic type with a 0.01- to 0.02-microfarad value are usually good bypass capacitors at 10.7 MHz. Larger values may exhibit a self-resonance below 10.7 MHz, and actually exhibit inductive reactance at their terminals. The nominal input impedance of the CA3089E is approximately 9,000 ohms, and it is not recommended that an impedance match be attempted. Most commercial receivers use ceramic-filter frequency-selective elements that normally have source impedances of 500 ohms or less. When these filters are properly terminated with loading resistors, the typical source impedance is further decreased to 250 ohms or less. Higher levels of source impedance are possible with very careful circuit layout; however, the maintenance of stability could be difficult.

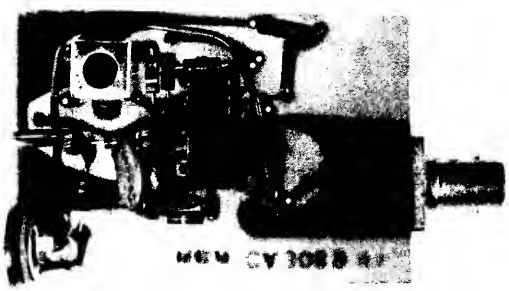
The CA3089E has a frequency response that is typically flat to 20 MHz; consequently, the device can provide useful gain well above that frequency. If the device is used at lower frequencies, the larger-value bypass capacitors required may not be adequate to bypass the higher frequencies. Double bypassing with lower-value capacitors can overcome such a problem. Another means of alleviating the problem is to externally reduce the frequency response by using a small capacitance across the output load of the device.

Quadrature-Detector Circuits

The quadrature-detector tuned circuit is connected between pins 9 and 10. The signal voltage at pin 8 is normally coupled to pin 9 through a choke. The circuit values for the detector network are determined by several factors, the primary one being distortion at a particular level of recovered audio. Distortion is determined by the phase linearity of the quadrature network and is not influenced by the device unless excessive, recovered audio overdrives the audio circuit. With a single tuned network, the phase linearity improves as the bandwidth increases; however, recovered audio decreases. A satisfactory compromise for most FM-receiver applications is reflected in the circuit of Fig. 9(a). This circuit typically provides 400 millivolts rms of recovered audio with less than 0.5-percent distortion. Because a double-tuned circuit has better phase linearity over a wider bandwidth, distortion figures of less than 0.1-percent are attainable with the network used in the circuit of Fig. 9(b). Proper alignment and coupling adjustment of the double-tuned circuit are most easily accomplished while viewing the resulting S curve. Initial adjustment of the primary tuning slug to the proper crossover is made with the secondary slug removed. The secondary tuning slug is then

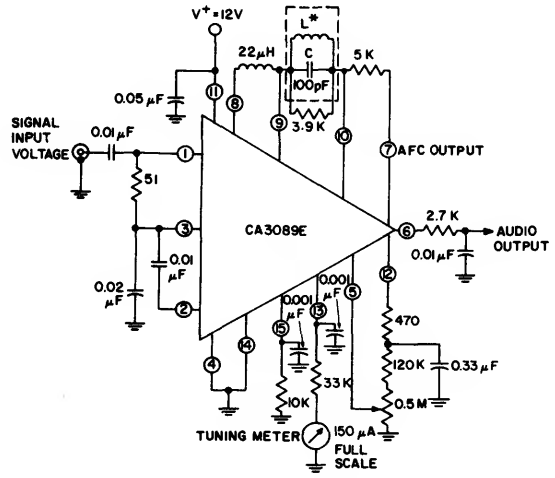


a) Bottom view of printed-circuit board.



b) Component side — top view.

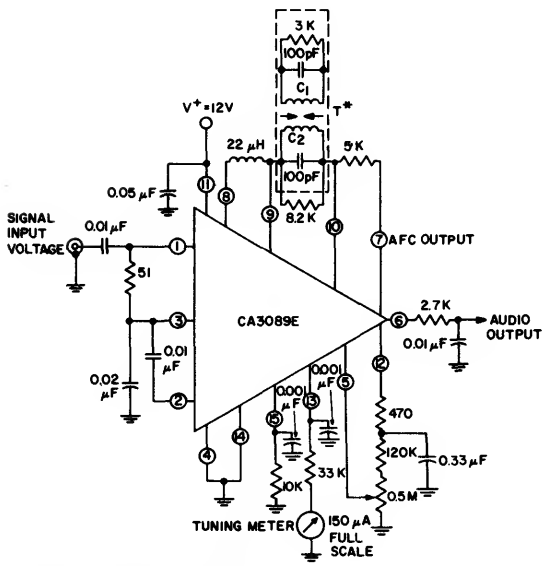
Fig. 8.—Actual-size photographs of the CA3089E and outboard components mounted on a printed circuit board.



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED)≅75. (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19040RI

(a)



ALL RESISTANCE VALUES ARE IN OHMS
* T: PRI.-Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM
SEC.-Q_0(UNLOADED)≅75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM
kQ (PERCENT OF CRITICAL COUPLING)≅70%
(ADJUSTED FOR COIL VOLTAGE V_C)=150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4mm

92CM-19041RI

(b)

Fig. 9– (a) Test circuit for the CA3089E using a single-tuned detector coil, (b) test circuit for the CA3089E using a double-tuned detector coil.

adjusted until a slight "ripple" is observed moving along the S curve. If the ripple is excessive (enough to distort the S curve) the coupling is too tight. If no ripple is observed, the coupling is too loose. As the ripple moves through the crossover point, it will be observed that the S curve becomes more linear near the center frequency. Slight readjustment of both slugs may be necessary for final alignment. The best performance can then be achieved by slight adjustment while measuring distortion. The coupling may be varied by either moving the coils or by changing the value of the secondary load resistor.

Various circuit values can be used to obtain the same recovered audio, but the basic conditions of circuit bandwidth and phase linearity must be maintained. The detector circuit also sets up conditions which are required for proper operation of the mute circuit. The rf voltage on pin 9 must be held at approximately 175 millivolts rms, ±25 millivolts. The reason for this requirement is discussed subsequently in connection with the mute logic circuit. The approximate voltage at pin 9 is determined from the equivalent circuit shown in Fig. 10.

The peak-to-peak voltage on pin 9 is:

$$|V_9| \cong |V_8| \frac{R1}{\omega L_{ch}}$$

where R1 is the total parallel resistance and V8 is approximately 300 millivolts, peak-to-peak.

The Q of the tuned circuit between pins 9 and 10 may be affected by the effective Q of the choke between pins 8 and 9 and the series resistor R31 in the CA3089E. All of the above factors should be considered in selecting circuit values. Table I lists some typical combinations of component values under various conditions.

A choke is normally selected to equalize delays in the signal path and in the limiter–quadrature path. It also reduces the if harmonic content across the quadrature circuit. In some cases, such as in narrow-band applications, it may become necessary to use a capacitor as the coupling component where large values of inductance with high Q's are difficult to obtain. If a capacitor is used, the phase of the recovered audio and AFC voltage will be reversed, some asymmetry of the S curve may result, and the distortion may be adversely affected to a small degree.

As indicated above, the inductance between pins 8 and 9 tends to equalize delays in the detector signal paths. The matching of elements of the IC in the balanced detector

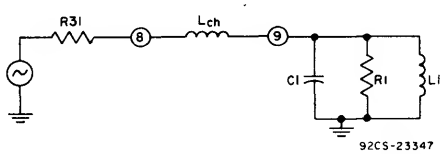


Fig. 10– Equivalent circuit used to determine approximate voltage on pin 9 of the CA3089E in Fig. 9.

TABLE I – FIG. 10 COMPONENT VALUES AND CHARACTERISTICS AS A FUNCTION OF FREQUENCY

Freq. (Hz)	L_1 (H)	QL_1	C_1 (pF)	R1 (ohms)	X (pin 8 to pin 9)	Deviation (kHz)	Recovered Audio (mV)
10.7M	2.2μ	75	100	3900	22μH	±75	400
10.7M	2.2μ	120	100		120μH	±5	280
10.7M	2.2μ	120	100		1.3pF	±5	290
455k	0.1m	65	1000	68k	1 mH	±5	400

circuit results in an AFC output with a very small offset when referred to the voltage at pin 10. For most applications, the inherent offset variation is well within tolerances, and does not affect circuit performance. In some narrow-band applications, however, the offset becomes more critical because of the very narrow bandwidth. In such situations, the combination of normal production variations of the device and the external circuit components results in receiver detuning when the AFC loop is closed. This detuning results in an increased distortion of the recovered audio. This distortion can be corrected with the addition of a variable capacitor from pin 8 to ground to provide phase compensation. The capacitor can be adjusted to provide zero AFC offset with minimum distortion. Generally, the offset is in one direction for a given set of conditions. The addition of a fixed capacitor will minimize variations sufficiently to satisfy many applications. A value of 5 picofarads is an effective value for the circuit of Fig. 9(a) with the recommended PC-board layout. Conversely, the offset created by using a capacitor between pins 8 and 9, as mentioned earlier, may be compensated by placing an inductance between pins 8 and 10.

Audio and AFC Circuits

The audio and AFC circuits are very similar, and both develop the same audio signal at their respective output terminals. The audio output voltage on pin 6 is developed across an internal, nominal, 5,000-ohm resistor (R49) connected to the 5.6-volt reference. In addition, the audio signal level can be attenuated by providing a direct current into pin 5 without any shift in its dc level. The audio output, as shown in Fig. 11, is uniform to a frequency of more than 1 MHz when measured in the circuit shown.

The AFC output at pin 7 is a current source and, if terminated with 5,000 ohms, will provide an audio output identical to that at pin 6. The AFC output may be referenced to a wide range of voltages, from near ground potential to near supply voltage. However, because of the balanced circuit configuration, the best AFC sensitivity and offset will occur at, or near, the 5.6-volt internal reference. An AFC voltage developed across a load tied back to pin 10 is recommended. As a consequence of this connection, variations in the AFC voltage as a function of operating voltage and temperature are minimized because the voltage on pin 7 tends to follow changes in the reference voltage.

Mute Circuit

The signal to the mute logic circuit is taken from the emitter follower connected to pin 9. This signal drives a peak

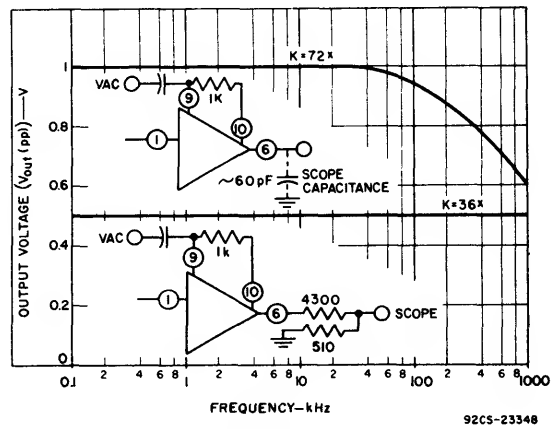


Fig. 11—Audio response at pin 6.

detector followed by an inverter such that the mute logic developed is zero volts with an input signal level sufficient to develop a fully limited output signal. As the input signal level is reduced below limiting, noise becomes significant, and creates "holes" in the if envelope. The detected drive voltage decreases and causes the mute logic voltage at pin 12 to increase. This voltage, in turn, is fed to pin 5 to provide the current to attenuate the audio. If the if level at pin 9 is too high, the "holes" created by the noise are insufficient to drive the mute logic voltage high enough to attenuate the audio. If the pin 9 voltage is too low, the mute drive voltage never reaches zero, and the external mute-threshold control behaves like a volume control. It is for this reason that the mute logic circuit requirements influence the selection of detector circuit values.

Another condition affecting proper mute performance is excessive gain in the tuner or preceding if stages. High gain ahead of the CA3089E under a condition of low signal-to-noise ratio results in the noise being clipped by the limiting amplifiers. The clipping has the effect of reducing the number of "holes" in the if envelope, and limits the mute drive voltage at pin 12 to values insufficient to attenuate the audio. If high gain is a system requirement, an externally derived mute logic voltage is necessary to drive pin 5.

The external circuit on pin 12 in Fig. 9(a) serves to filter the output, and provides a variable potential for mute-threshold adjustment. The 470-ohm resistor in series with pin 12 reduces the effective Q of the filter capacitor and prevents the circuit from setting up on noise current

transients as the mute circuit begins to function. The voltage divider, composed of the 500 kilohm potentiometer and 120 kilohm resistor, controls the threshold point. These values are suggested ones, and may be altered to suit the user. Curve A in Fig. 12 shows the change in audio output level as a function of input signal with the mute-threshold control circuit (also shown in Fig. 12) at its maximum-voltage setting. Because of the more shallow slope and the larger circuit time constant involved, a "soft" mute action results. Curves B and C illustrate the change in the curves resulting from adjustment of the values of the threshold control circuit. These latter circuits provide a faster acting mute. The fixed resistor, R1, in addition to controlling the slope of the mute characteristic, limits the voltage appearing at pin 5. The use of this resistor is recommended to prevent a latch-up at the attenuating circuit, which, if it occurs, maintains the circuit in muted condition until the supply voltage is removed.

The curves in Fig. 12 show that the muting action cannot be initiated under any condition until some noise is present in the output signal. In this respect, the mute performance of the CA3089E differs from that of some other systems which are activated by signal level. Such systems can be adjusted to allow noise-free signals to be processed further. When the CA3089E circuit operates under small-signal conditions, noise may be audible before muting action occurs. The threshold-level adjustment only permits more or less noise to appear at the output; a listener can use the control to adjust the interstation hiss to the level of his preference.

Tuning Meter and RF-AGC Circuit

The tuning-meter circuit sums the output of three peak detectors connected to successive stages of the if amplifier-limiter. These circuits detect not only the carrier, but also harmonics developed when successive stages go into limiting and eventually form a square wave. The result is a logarithmic dc output as a function of input signal, as shown by the curve in Fig. 13. The circuit developing the delayed

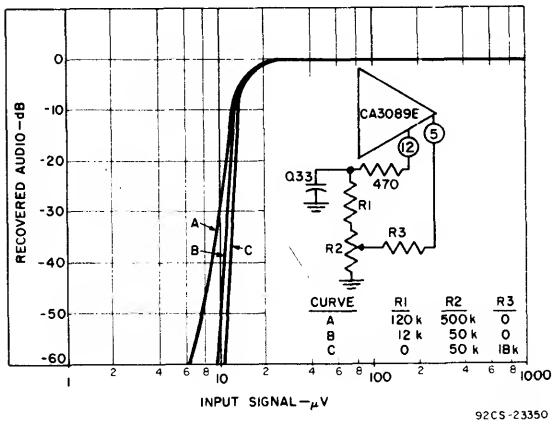


Fig. 12—Mute curves.

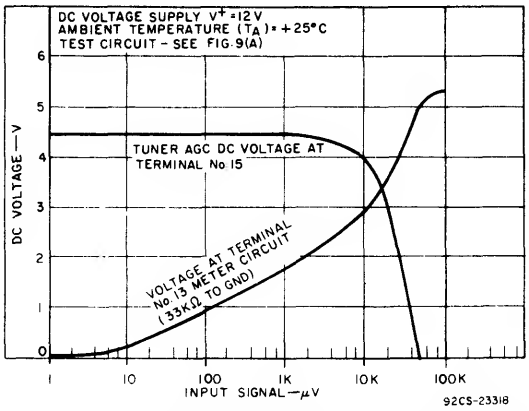


Fig. 13—Tuner AGC and tuning-meter output as a function of input signal voltage.

rf-AGC voltage is driven by the level detector connected to the first if stage. As a result, no output is detected until the input signal is large enough to drive the peak detector; the result is a delayed AGC action. The curve of rf-AGC voltage as a function of input signal is also shown in Fig. 13.

IF Amplifier/Detector System and Stereo Decoder

Fig. 14 shows the circuit diagram of a complete FM-if detector system driving a stereo decoder. Using the selectivity of two ceramic filters, the CA3089E in conjunction with the CA3090AQ stereo decoder provides the basic signal processing between the tuner output and the audio amplifiers. The gain of the silicon n-p-n bipolar-transistor stage is adjusted to make up the losses of the two filters. In addition to driving a tuning meter, the voltage at pin 13 of the CA3089E may be used to drive a "stereo defeat" circuit in the CA3090AQ, thereby holding the decoder in a monaural condition to improve the signal-to-noise ratio under weak signal conditions. A suggested PC-board pattern and parts layout are shown in Fig. 15.

Operation at Frequencies Other Than 10.7 MHz

Because the CA3089E was designed for use in FM broadcast receivers, its circuits are optimized for use at 10.7 MHz. Nevertheless, the device performs equally well over a wide range of frequencies both above and below 10.7 MHz. The if amplifier response is essentially flat from dc to more than 20 MHz. The operation of the detector circuit is dependent only on the external components. The operation of the auxiliary sections—rf-AGC, meter output, and mute logic – depend on internal peak detectors, and, as a consequence, their performance at lower frequencies is limited. The internal capacitors were optimized for 10.7 MHz operation, and are too small to operate effectively at lower frequencies. The detector efficiencies begin to deteriorate at about 2 MHz, and the detectors are essentially unusable at 455 kHz without the use of external circuitry. The rf-AGC and mute logic circuits do not develop sufficient dc voltage

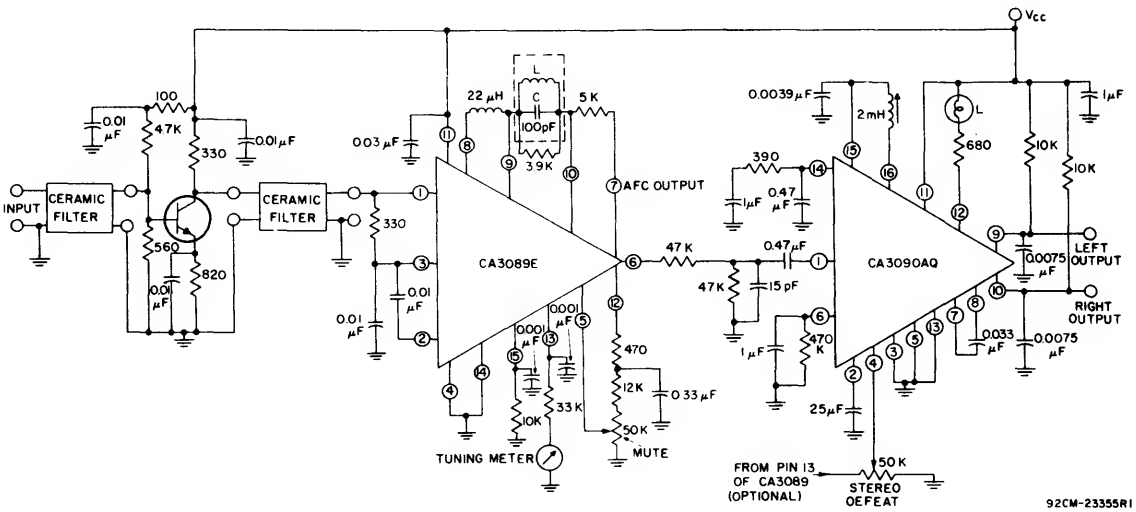
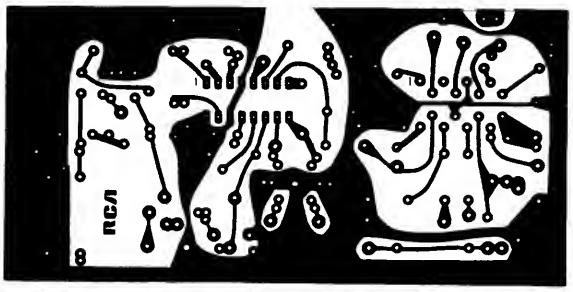


Fig. 14—IF amplifier/detector system and stereo decoder.

to perform their functions, and the meter output signal loses its logarithmic characteristic and exhibits peaks and valleys as input signal is increased. Operation of the rf-AGC and mute logic circuits may be enhanced by the addition of a dc amplifier and inverter to each circuit. A simple example using a CA3096E IC transistor array is shown in Fig. 16.[3]

The CA3089E may be used effectively in narrow-band communication receivers. In double-conversion receivers, some of the functions of the CA3089E are negated at a 455-kHz intermediate frequency. However, if a 10.7-MHz intermediate frequency is used, all of the auxiliary features



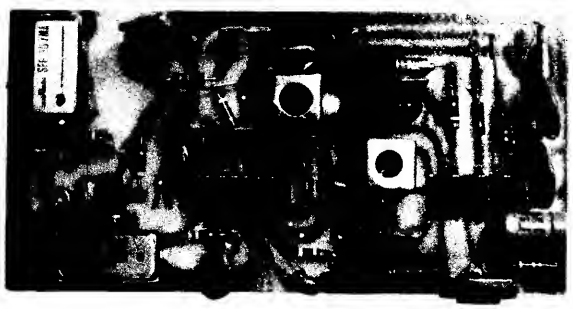


Fig. 15—Suggested PC-board pattern and parts layout for the circuit of Fig. 14.

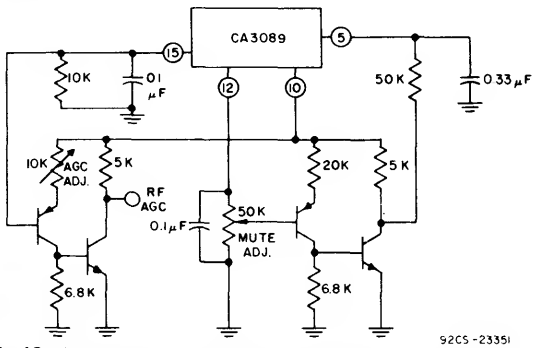


Fig. 16—External mute and rf-AGC drive circuits for the CA3089E operating at 455 kHz. External transistors are parts of the CA3096E n-p-n/p-n-p transistor array.

may be used, but another set of problems is encountered. The small deviation signals encountered in narrow-band systems require the use of high-Q circuits in the quadrature detector, as indicated in Table I. However, variations in external-component parameters with temperature changes may cause the tuned frequency of the detector to drift out of the if pass band. Normally temperature-compensated components are necessary. The CA3089E, operating in conjunction with an inexpensive operational transconductance amplifier,[4,5] provides means of locking the tuned circuit to the incoming frequency. Fig. 17 shows the block diagram of such a system. The AFC output voltage developed across the resistor between pins 7 and 10 is amplified by the op-amp and drives a varactor to maintain the tuned frequency on the incoming-signal frequency.

The CA3089E may also be used as the core of an ultra-linear FM generator; Fig. 18 shows the circuit. The carrier is generated by the CA3089E with the introduction of feedback from the output terminal, pin 8. The carrier is

modulated by the varactor connected across the tuned circuit at the input of the CA3089E. The varactor is driven by the output of the differential amplifier, A1, using a CA3028 IC.[6,7] This differential-amplifier stage is driven at one of its input terminals by the audio modulating signal. Negative feedback of the audio signal is provided by driving the other differential-amplifier input from the recovered audio output of the CA3089E at pin 6. The detector circuit uses a double-tuned transformer to produce audio with very little distortion at pin 6. This feedback technique results in a very low distortion modulation. The rf output of the CA3089E at pin 8 is essentially a square wave, and is fed to a tuned-amplifier stage to buffer the signal and restore the sine-wave-shaped rf output signal.

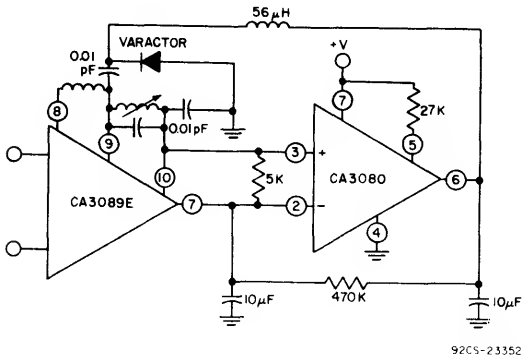


Fig. 17—Detector frequency-stabilization circuit.

Acknowledgments

The author thanks Jack Craft for his aid and suggestions in many discussions and Frank Curley for his aid in circuit construction and collection of data.

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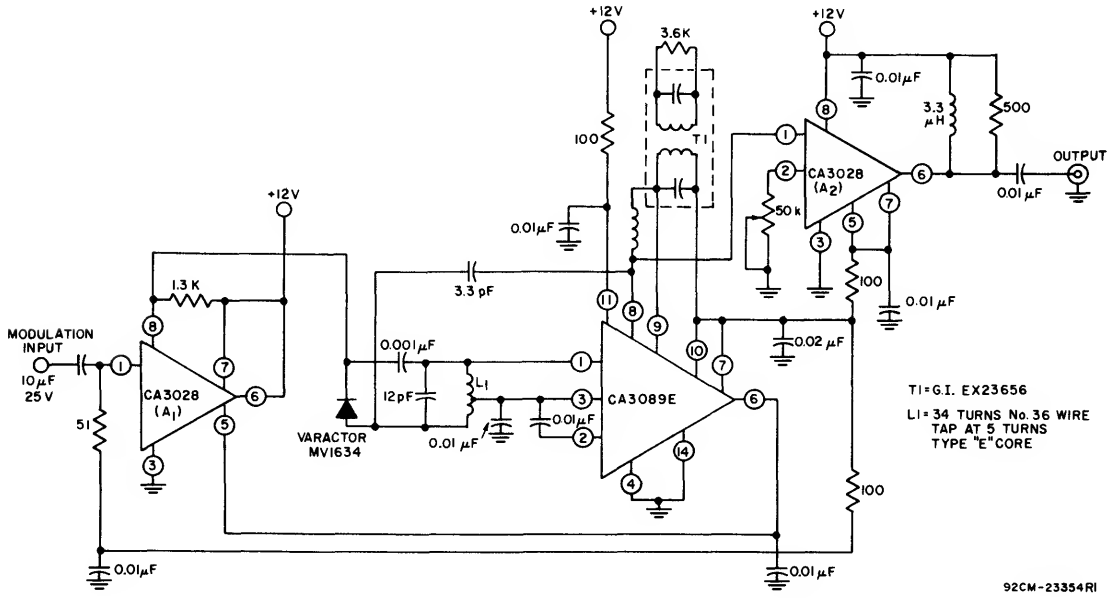

Fig. 18—FM generator circuit.

Integrated-Circuit Stereo Decoder Using The CA3090AQ Stereo Multiplex Demodulator

by L.A. Kaplan and A.L. Limberg

The demodulation of FM stereo broadcast information may be accomplished very simply by use of no more than three transistors, four to six diodes, and two small transformers as major system components. All of these components may be very inexpensive with minimal specifications. However, accurate demodulation of FM stereo broadcast information, particularly when the signal to noise ratio of the incoming signal is poor and when the performance must be achieved over a wide ambient temperature range such as, for example, in the automobile radio, is an entirely different matter.

The system shown in Fig. 1 was built by RCA's Transistor Applications Laboratory to demonstrate a high-performance demodulator system. Some of the design considerations will be discussed later, but the complexity of the filtering included and the bulk of the system is evident.

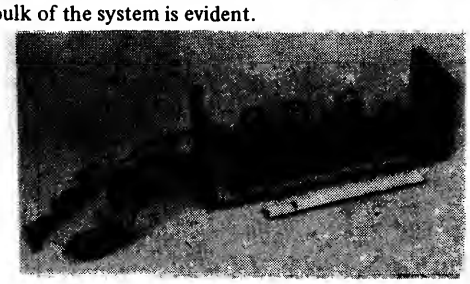

Fig. 1 – Multiplex stereo decoder using discrete components.

By contrast, the integrated-circuit system described in this Note*, Fig. 2, performs all the functions of its predecessor, and does them better. Performance of the IC system is summarized in Table 1.

* This Note supersedes RCA Technical Publication ST-4700, "Integrated-Circuit Stereo Decoder Does Everything," by L.A. Kaplan, H.M. Kleinman, A.L. Limberg.

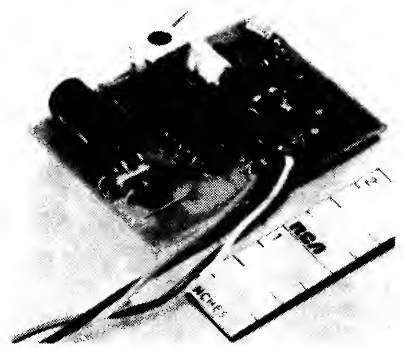

Fig. 2 – Integrated-circuit multiplex stereo decoder.

Table I – Performance Data

SEPARATION		40 dB
DISTORTION	2nd Harmonic	<0.2%
	3rd Harmonic	<0.1%
	4th Harmonic	<0.1%
	5th Harmonic	<0.1%
CAPTURE (% of CENTER FREQUENCY)		10%
SCA REJECTION		–55 dB
MONAURAL GAIN (75 μs DE-EMPHASIS, 1 kHz)		6 dB
GAIN BALANCE BETWEEN CHANNELS		<0.5 dB
STERO/MONAURAL GAIN BALANCE		<0.5 dB
INPUT IMPEDANCE		50 kilohms
TEMPERATURE COEFFICIENT OF LOCAL OSCILLATOR		–16 Hz/°C
LAMP DRIVER CURRENT		100 mA

DESIGN REQUIREMENTS AND OBJECTIVES

The stereo multiplex demodulator has simply defined tasks. First, it must reconstruct the 38-kHz carrier which was suppressed in forming the stereo signal. This reconstructed carrier must be properly phased to accomplish the demodulation process. Second, it must be substantially noise free to avoid further significant degradation of the signal-to-noise ratio of the output. This signal has already been degraded from that achieved in monaural transmission because of the wider system bandwidth of the stereo transmission.

A further function which demands narrow bandwidth in each channel is the stereo indicator which detects the presence of the 19-kHz pilot and energizes a lamp to inform the listener that stereo is being transmitted. If the bandwidth of the 19-kHz filters is too wide, noise energy in the pass-band of the filter can be sufficient to cause the light to blink during tuning between stations. This effect is undesirable in a high-quality system.

In essence, the demodulator must use the reconstructed carrier to demodulate the composite signal without introducing objectionable distortion. It must also have provisions for inhibiting the demodulation function when poor signal-to-noise conditions exist and, finally, must ignore completely the SCA signal transmitted by some stations. This signal is a second subcarrier bearing FM information modulated at about 67 kHz. Unless care is taken, the intermodulation products of the 38-kHz subcarrier (stereo) and the 67-kHz subcarrier (SCA) form audible beats.

These requirements of phase fidelity and low noise are difficult to achieve simultaneously in a compact, inexpensive system using traditional techniques because of the method of carrier synchronization. The 19-kHz pilot signal must be selected, amplified, and doubled without disturbing its phase relationship with the 38-kHz difference-signal (L-R) information. When conventional LC filtering techniques are used, conflicts are established. If noise is to be reduced in the subcarrier regeneration process, narrow bandwidth is needed in that channel. Narrow band filters, unless they are both accurately designed and precisely tuned, can cause substantial phase shift.

Analysis shows that 26 degrees of phase shift of the 38-kHz subcarrier relative to the 38-kHz sidebands will degrade the separation of an otherwise perfect system from infinity to 26 dB. Because a degradation of 20 dB would cause the system to fail most instrument specifications and would be detectable by critical listeners in some situations, it is reasonable to demand that phase shift in the subcarrier not consume all of the permitted degradation.

If each transformer were to have a 9-degree phase shift at 38 kHz, the reactance factor X for the 38 kHz trans.=0.158, where $X = 2\Delta f Q/f_0$. This condition is obtained when the attenuation in that transformer is computed from $X = \tan^{-1}\theta$ and the attenuation (ρ) = $\sqrt{1+X^2}$ so that $\rho = \sqrt{1+(.1582)^2} = 1.012$ or less than 0.1 dB. Because only 4.5 degrees are permitted in each of the 19-kHz transformers, the attenuation for permissible phase shift will be less than 0.1 dB.

This analysis clearly shows that manual tuning of the subcarrier channel cannot be achieved by the traditional peaking methods, rather, it must be aligned by measuring channel separation characteristics. Further, once correct tuning is achieved, the permissible mistuning resulting from mechanical or environmental conditions must be low. If quality factors (Q's) of 25 are assumed, the permissible mistuning of a 19-kHz transformer is given by

$$\frac{\Delta f}{f} = \frac{\tan 4.50^\circ}{2Q} = \frac{0.08}{50} \text{ or } 0.16\%$$

and for the 38-kHz coil:

$$\frac{\tan 9^\circ}{50} = \frac{0.16}{50} \text{ or } 0.32\%$$

These values represent a mistuning of 30 Hz at 19 kHz and 120 Hz at 38 kHz, respectively. If the mistuning is due only to temperature over a ±50°C ambient temperature range, the following temperature compensation is required:

$$\frac{\Delta f}{f} \Big/ \Delta T = \frac{0.0016}{50} = \frac{0.0032}{100} = 0.000032$$

or 32 PPM/°C for the 19-kHz transformer and 64 PPM/°C for the 38-kHz one. Finally, if higher Q coils are used to improve selectivity and to reduce noise in the subcarrier, the stability of the circuits must be even better.

Non-distorting demodulation and stereo disabling can be accomplished easily, but care must be taken to insure that the latter be accomplished in a manner that eliminates transient level shifts when the switching occurs. Rejection of the SCA channel is generally guaranteed to some extent by LC filtering at the input to the demodulator which removes signal components above 60 kHz. This method requires either expensive pretuned components, or an additional alignment, and runs the risk of causing phase shift of the higher subcarrier sideband frequencies, thereby degrading separation for the highest frequency components of the program.

There are three specific problems which the designer of a stereo multiplex demodulator must consider if he has to achieve an economical high performance design:

1. Provide a narrow band carrier regeneration channel with negligible phase shift over the ambient temperature range and life of the equipment. This setup should preferably be alignable with a single simple adjustment.
2. Develop a system which inherently rejects the 67-kHz SCA subcarrier so that an LC filter is not required for that purpose.
3. Provide stereo-monaural switching without audio "plops".

In addition to these rather difficult problems, the designer must not ignore distortion which must be kept well below 0.5 precent, and, of course, he must minimize the cost of external components.

Description of the RCA CA3090AQ Stereo Multiplex Demodulator IC

Fig. 3 shows the CA3090AQ as it is used in a typical FM receiver. From this illustration, the solutions to the problems

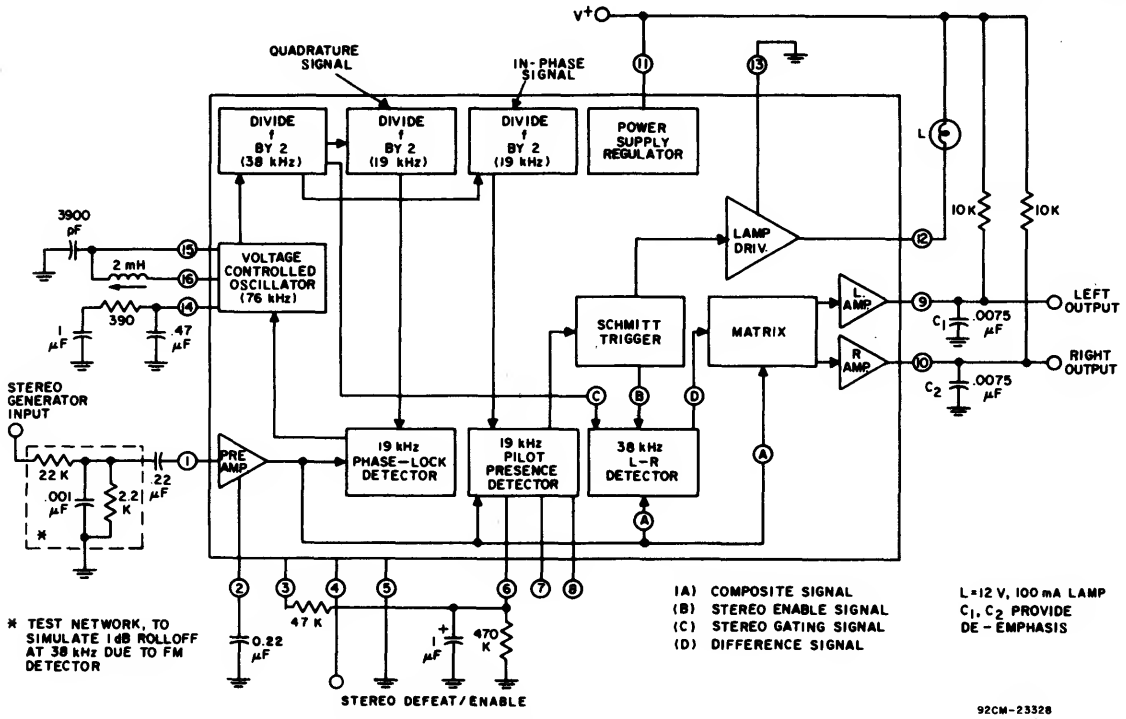

Fig. 3 – Block diagram of the RCA CA3090AQ system.

posed previously will be studied. In this circuit, carrier regeneration is accomplished by use of a phase-lock automatic frequency and phase control (AFPC) loop made up of a voltage-controlled oscillator operating at 76 kHz, a series of flip-flops to obtain the required signals needed in the system, and a synchronous detector the DC output of which is proportional to the relative phase angle between the frequency-divider output and the 19-kHz component of the composite signal. Bandwidth of the loop is determined by an external RC filter and, as will be shown later, the steady-state phase error is only indirectly related to the bandwidth of the phase-locked loop.

The voltage-controlled oscillator (VCO) used in this circuit is an LC oscillator. This type was chosen over the apparently simpler RC oscillator on the basis of its superior long-term and temperature stabilities. It is noted that the oscillator operates at 76 kHz, while the maximum frequency required by the signal processing circuits is 38 kHz. The higher frequency is used at the expense of extra chip complexity to insure that the reinserted 38-kHz carrier is perfectly symmetrical, because any loss of symmetry will impair audio-channel separation. By starting at 76 kHz and dividing by two to get the required 38 kHz, symmetry is guaranteed, though the phase of the 38 kHz may shift relative to the 76-kHz voltage. This shift, however, is not significant.

Fig. 3 also shows that the switching input to the phase-detector (AFPC) is not in phase with the pilot frequency but is displaced by 90 degrees. This condition will exist when there is no phase error, because the demodulator is a multiplier whose output is proportional to the cosine of the angle between the inputs. Because the output of this detector may be considered as an error voltage in a feedback loop, the system will attempt to make it zero, hence, the 90° displacement so that the required 38-kHz signal is of the proper phase. And because the output of the AFPC detector is zero when both the uncontrolled frequency of the oscillator is correct and when there is no 19-kHz pilot, and extra detector, the pilot presence detector, is needed to signal the presence of a stereo broadcast. The 19-kHz output from the frequency-divider is in phase with the pilot signal and will, therefore, provide a signal to the stereo-mono switch to enable stereo reception. An external RC network sets the threshold sensitivity and time constant of this detector. This filtering, along with the hysteresis in the stereo-mono switch, eliminates all interstation flicker of the stereo indicator lamp.

The L-R synchronous detector is a fully degenerated doubly-balanced detector. Great care is taken to guarantee that the composite signal currents fed to it are as nearly distortion-free as possible to preserve both fidelity and SCA rejection. Should significant distortion exist, intermodulation products of the sidebands of the 38-kHz and 67-kHz subcarriers would be formed before demodulation. Many of these spurious signals will be within the 23- to 53-kHz bandwidth of the demodulation and would therefore show up in the output as audible whistles and beats.

The outputs of the L-R detector are added to the composite signal in summing networks where precisely matched resistors provide the proper scale factors. Theoretically, the sum signal (L+R) channel must be attenuated by the ratio $2/\pi$ to obtain perfect separation. This ratio holds true only for perfect

composite inputs. Experinece has shown that nearly all commercial FM tuners attenuate the high-frequency components of the composite signal by some amount, usually in the order of 1 dB and 38 kHz. Therefore, the L+R is attenuated slightly more than $2/\pi$ to compensate for this degradation of the input signal. (See Fig. 12 for a curve of error caused by imperfect detector response.) If the CA3090AQ is called upon to process a "perfect" composite signal, audio-channel separation will be in the order of 26 dB because of this deliberate deviation.

The phase-splitter, post-amplifiers, and the stereo-mono switch which contains an enabling circuit capable of responding to an external DC voltage to permit stereo reception complete the integrated circuit. This latter circuit may be connected at the users option and can inhibit stereo reception until a positive going DC voltage exceeds 1.6 volts. As in the case of the primary stereo-mono switch, hysteresis is provided to reduce the flicker of the stereo indicator under weak signal conditions.

Phase Lock Loop (AFPC Loop) Operation

The operation of phase-lock loops (PLL) is well documented in the literature and is treated mathematically at some length in the Appendix section. It will be discussed briefly here to indicate the degree to which the phase-lock can provide superior performance to that achievable by conventional filter methods.

The functional blocks of the PLL are shown in Fig. 4. The multiplier is the phase-detector with the reference signal $E_2 \sin\omega_0 t$ and the VCO signal $A\cos(\omega_0 t - \theta)$ (θ is the phase error in radians) applied to it. The output of the detector is K $\cos\theta$ in which K is a function of E_2 as well as the parameters of the multiplier. The phase error output is proportional to $\sin\theta$ because of the phases of the angles selected. It is noted that, if the frequency of the VCO differs from that of the input, θ will

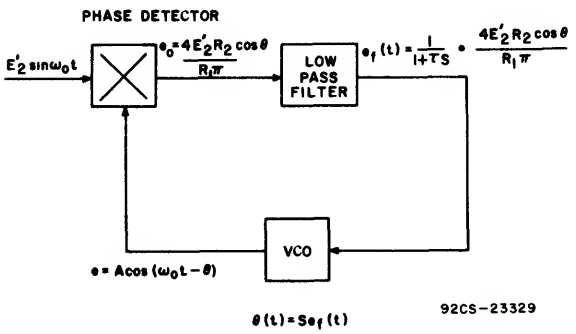

Fig. 4 – Block diagram of a phase-locked loop (PLL).

equal $+\omega_d t$ in which $\omega_d t$ is 2π times the frequency difference between the two oscillators. This condition will occur before frequency-lock is achieved. The error voltage, K sin θ; is passed through a low-pass filter and applied to the control terminal of the VCO. Once the VCO is locked in frequency to the input signal, θ will become a constant and the output of the detector will be a DC voltage which is proportional to the phase-error. It can be reasoned, without resorting to mathematics, that this resultant voltage must be just the voltage required to change the frequency of the VCO from its natural frequency to that of the input frequency, i.e.:

$$K \sin\theta = \frac{\omega d}{S}$$

where ωd is the previously noted difference frequency and S is the sensitivity of the VCO. This equation can be expressed in easily measured terms and solved for θ, where

$$\theta = \frac{\omega d}{KS} \text{ for small angles.}$$

In this case, f_d and S can be measured at any point along the frequency divider. Because the oscillator is available, measurement is taken at that point and it is found that S equals about 400 Hz per millivolt. The phase-detector output K is measured at 2 millivolts per degree of phase differential at 19 kHz, which is the equivalent of 1 millivolt per degree at 38 kHz. The resultant phase-error in the PLL is $f_d/400$ or, more usefully 1.9 degrees per percent in oscillator shift. In other words, if the VCO is adjusted to a nominal 76-kHz frequency and then shifted by 3.8 kHz because of aging, temperature effects, or other reasons, this frequency shift of 5 percent would cause a shift of 9.5 degrees in phase of the regenerated 38-kHz carrier. Curves (Fig. 13) show that such a 5 percent frequency-shift would cause the audio-channel separation of an otherwise perfect system to drop to 42 dB, virtually unnoticeably.

The degradation caused by a 5-percent frequency shift may be compared with the 26-dB separation characteristic resulting when the three coils of the classical filter-approach shift by only 0.3 percent. It is noted that the final phase-error is not a function of the filter placed in the loop (see Appendix B). That time constant is constrained by the stability of the VCO's unlocked natural frequency. In the present system, a filter with a 54-Hz bandwidth is used and provides a capture capability in excess of 4 kHz at 76 kHz. The classical filter-approach previously described has a 3-dB bandwidth or nearly 200 Hz at 19 kHz with proportionally poorer noise performance.

The LC Oscillator and Reactance Circuit

The LC oscillator is undoubtedly the most controversial portion of the CA3090AQ system. The demand for "inductorless designs" was not ignored during the development, but performance sacrifices were required to reliably implement such a design if low-cost external components were to be used. Comparisons were made on two levels, that of stability of the semiconductor portion of the oscillator circuit with both aging and temperature and stability of the oscillator frequency as the external components varied with both aging and temperature.

Tests on the CA3090AQ indicated oscillator sensitivity to temperature changes to be less than 1.5 percent for 50°C temperature changes. Data sheets for commercially available integrated-circuit voltage-controlled RC oscillators show changes of 4 to 7 percent for the same temperature change. These changes do not indicate that better RC oscillators cannot be built, but suggests that such designs will be an interesting challenge to the IC designer.

More compelling than the previous discussion is the problem of the external components. Because some method of tuning must be used if the nominal frequency is to be set accurately, either a tunable inductor, variable capacitor, or potentiometer must be used.

The resonant frequency for a general RC oscillator is $\omega = K/RC$ while ω for the LC oscillator is $1/\sqrt{LC}$. Differentiating each of these with respect to the assumed variable components (R or L) shows that:

$$\frac{d\omega}{dR} = -\frac{\omega_0}{R}$$ for the RC oscillator and

$$\frac{d\omega}{dL} = -\frac{\omega_0}{2L}$$ for the LC oscillator

In other words, it would take twice the parameter variation for the LC oscillator as it does for the RC oscillator to create the equivalent frequency shift.

The most attractive adjustment for an RC oscillator is the inexpensive carbon-composition trimmer. Available data indicate temperature coefficient of the order of 1000 PPM/°C and changes with humidity of 3 percent nominal value after exposure and drying. It is noted that this 3 percent change for an RC oscillator would generate a 2.3-kHz shift in frequency due to humidity alone. Trimmers with far more stable characteristics are available, but at a substantial cost preminum.

Stereo Defeat Circuit

In most modern FM receivers the RF/IF gain is high enough to cause limiting on noise alone. The signal-to-noise ratio increases as the incoming signal increases but it may be desirable to prevent stereo operation, with its attendant signal-to-noise degradation, until the input signal-to-noise is above a selected threshold.

A stereo defeat circuit has been incorporated into the CA3090AQ for this purpose as shown in Fig. 5. It is a fairly conventional Schmitt trigger which allows the unit to function in stereo when the voltage at pin 4 exceeds plus 1.6 volts. The hysteresis is about 0.1 volts, thereby assuring the continuance of stereo function despite small changes in signal level.

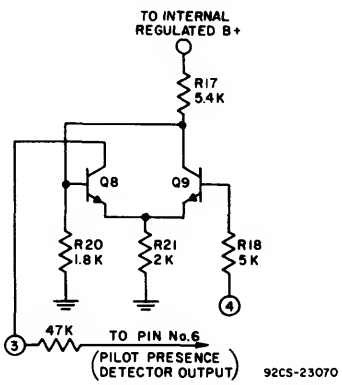

Fig. 5 – Stereo-defeat circuit.

DC Coupled Flip-Flop

It was apparent at the outset of the design that a direct-coupled flip-flop was required. If the capacitors needed for a conventional flip-flop were designed "on-chip", these capacitors would spread over very large amounts of chip area, and, if they were placed "off-chip", they would use up the limited number of package terminals.

The flip-flop design is shown in Fig. 6. Transistors Q1 and Q2 are connected as the storage flip-flop and Q3 and Q4 as the commutation flip-flop. The information stored in the storage flip-flop is coupled through diodes D1 and D2 to guide the biasing of the commutating flip-flop when Q5 is triggered into conducting by a positive pulse. When the commutating flip-flop is placed into conduction, diodes D1 and D2 are biased out of conduction. Current is coupled through one of the diodes D3 and D4 to cause the storage flip-flop to change state. At the end of the positive pulse triggering Q5 into conduction, the module is again ready to accept trigger to change the state of the storage flip-flop.

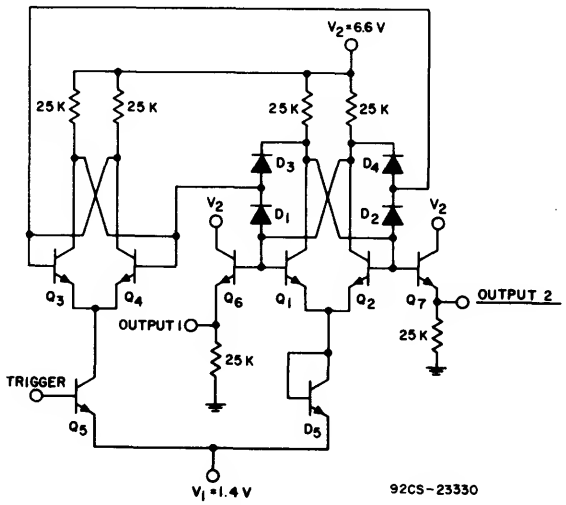

Fig. 6 – DC coupled flip-flop.

If the trigger pulses applied to Q5 have regularly timed leading edges, the outputs of the module taken from the storage flip-flop through emitter followers Q6 and Q7 are push-pull square waves between 1.4 and 2.1 volts.

Preamplifier Phase Splitter

The preamplifier phase splitter is illustrated in Fig. 7. The circuit is symmetrical, and is most easily analyzed by considering one half of it. In this case, Q78 is an emitter follower supplied by Q4, and Q6 is a shunt regulator stage; Q1 and Q2 are current sources. When current in Q4 and Q78 tends to increase, the potential at the base of Q6 rises and causes Q6 to draw more current. The increased current demanded by Q6 must come from the emitter of Q4. If Q4 passes a constant current, its base-emitter potential will not vary, and the base current will be constant. Thus, the input impedance to ac will be high and the signal will be passed with low distortion.

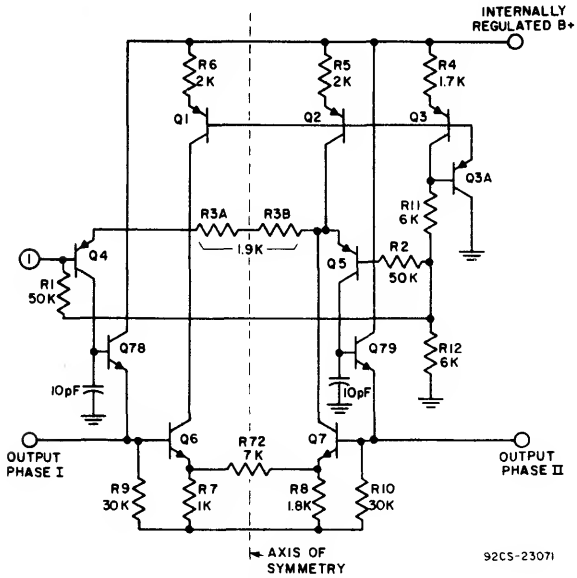

Fig. 7 – Preamplifier phase splitter.

The accurately reproduced input signal which appears at the emitter of Q4 then forces a current through the 1.9-kilohm resistor connected to the emitter of Q5. Because the emitter current of Q4 is held constant by the shunt regulator Q6, the collector current of Q6 must be complementary to the current in the 1.9-kilohm resistor and also proportional to the input signal.

Any transistors having identical geometry and emitter resistors with bases connected to the base of Q6 will have collector currents identical to that of Q6. By similar analysis, Q7 will have collector current exactly proportional to the current in the 1.9-kilohm resistor, and identical transistors connected in phase to those connected to Q6.

PERFORMANCE

Pertinent performance data for the CA3090AQ are summarized in Table I. The variation in capture range is shown in Fig. 8 as the phase-lock filter capacitor is varied (see Appendix C). The effects of the level of pilot on the capture range are illustrated in Fig. 9. In both graphs the clear areas represent sufficient conditions for "capture" into stereo operation, while the shaded areas indicate probable failure to "capture."

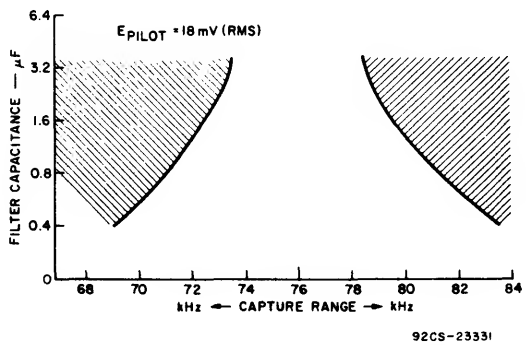

Fig. 8 – Capture range as a function of the filter capacitance.

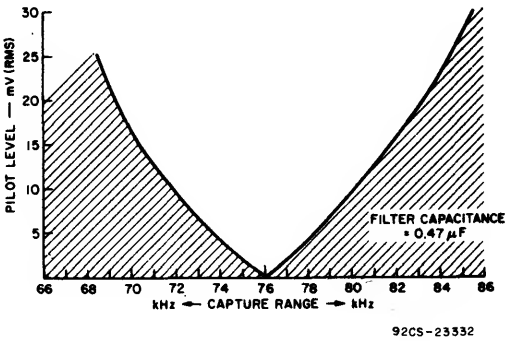

Fig. 9 – Capture range as a function of pilot level.

CONCLUSION

The RCA CA3090AQ integrated-circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment which reduces to a minimum the manual effort during assembly, while the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art.

APPENDIX A

Detector Response

Most practical FM receivers are designed so that the audio response at the second detector rolls off somewhere above the audio range for IF filtering and reduction of "tweet" effects. The voltage response V in the time domain is given by

$$V = \frac{\sin(\omega t - \tan^{-1}\omega/\omega_0)}{\sqrt{1+\left(\frac{\omega}{\omega_0}\right)^2}} \quad (1)$$

where t is the time, ω is the frequency, and ω_0 is the cutoff frequency of the detector.

A properly tuned phase-lock detector will lock to the 19-kHz pilot and reconstruct the 38-kHz gating signal at zero phase. The 38-kHz sidebands will be delayed in time with respect to the 19-kHz pilot-tone. The time-delay difference Δt between the two is given by

$$\Delta t = \frac{\tan^{-1}\frac{2\omega_1}{\omega_0} - 2\tan^{-1}\frac{\omega_1}{\omega_0}}{2\omega_1} \quad (2)$$

where $\omega_1 = 2\pi \times 19$ kHz

The corresponding phase angle Δ is given by:

$$\Delta = \tan^{-1}\frac{2\omega_1}{\omega_o} - 2\tan^{-1}\frac{\omega_1}{\omega_o}$$

A composite signal, S, is assumed in the form:

$$S = L + R + f(\omega_o)(L\text{-}R)\cos\phi + \text{Pilot} \quad (3)$$

where the gate signal is at reference phase θ and input signal is at phase ϕ separated from θ by the phase error Δ and

$$f(\omega_o) = \frac{1}{\sqrt{1+\frac{4\omega_1^2}{\omega_o^2}}} \quad \text{(amplitude error function)} \quad (4)$$

The gate signals G are given by

$$G^+ = \frac{1}{2} + \frac{2}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta$$

$$G^- = \frac{1}{2} - \frac{2}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (5)$$

The gated signals are

$$SG^+ = S \times G^+$$

$$SG^- = S \times G^- \quad (6)$$

The output signal S_{out} is given by

$$S_{out} = S + SG^+ + (-SG^-) \quad (7)$$

Substitution of Eqs 3, 5, and 6 into Eq. 7 results in the following:

$$S_{out} = \frac{2}{\pi}(L+R) + \frac{2}{\pi}f(\omega_o)\cos(\theta - \Delta) + \frac{4}{\pi}(L+R)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta + \frac{4}{\pi}f(\omega_o)(L-R)\cos(\theta-\Delta)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (8)$$

The signal separation L/R is given by

$$\frac{L}{R} = \frac{1 + f(\omega_o)\cos(\theta-\Delta) + 2\left[\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1+f(\omega_o)\cos(\theta-\Delta)\right]}{1 - f(\omega_o)\cos(\theta-\Delta) + 2\left[\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1-f(\omega_o)\cos(\theta-\Delta)\right]} \quad (9)$$

The decoded information is the integral of the output averaged over one cycle of carrier frequency and is given by

$$\frac{L}{R} = \frac{1 + f(\omega_o)\cos\Delta}{1 - f(\omega_o)\cos\Delta} \quad (10)$$

A curve of this function is shown in Fig. 10.

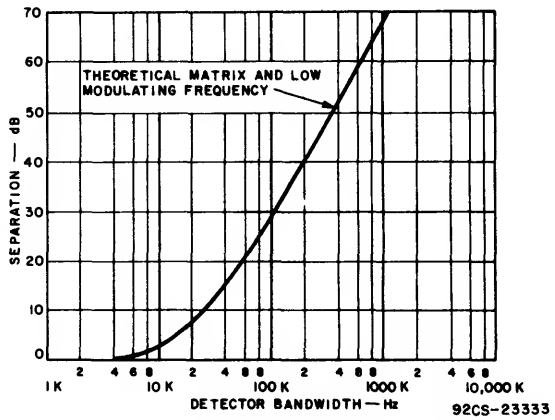

Fig. 10 — Theoretical separation as a function of detector bandwidth.

Matrix Error and Fixed Phase Error

When the oscillator has been incorrectly tuned and when the system has "captured" and locked to the pilot-tone, there will be a fixed phase error Δ which is a function of the original amount of detuning and the phase-lock loop gain discussed in Appendix B. This fixed phase error will produce a loss of audio-channel separation as will an error in the resistor ratios of the matrix. The equations are as above except that a fixed gain-error constant k is introduced into the signal term as follows:

$$S_{out} = kS + SG^+ + (-SG^-) \quad (11)$$

Substitution of Eqs. 3, 5, and 7 again yields the following:

$$S_{out} = k(L+R) + k(L-R)\cos(\theta-\Delta) + \frac{4}{\pi}(L+R)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta + \frac{4}{\pi}(L-R)\cos(\theta-\Delta)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (12)$$

The separation is then given by

$$\frac{L}{R} = \frac{k[1+\cos(\theta-\Delta)] + \left[\frac{4}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1+\cos(\theta-\Delta)\right]}{k[1-\cos(\theta-\Delta)] + \left[\frac{4}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1-\cos(\theta-\Delta)\right]} \quad (13)$$

Integrating and averaging as before reduces this equation to the following:

$$\frac{L}{R}=\frac{k+\frac{2}{\pi}\cos\Delta}{k-\frac{2}{\pi}\cos\Delta}$$

A new constant K is defined such that

$$\frac{L}{R}=\frac{K+\cos\Delta}{K-\cos\Delta}$$

Families of curves generated by this function are given in Fig. 11.

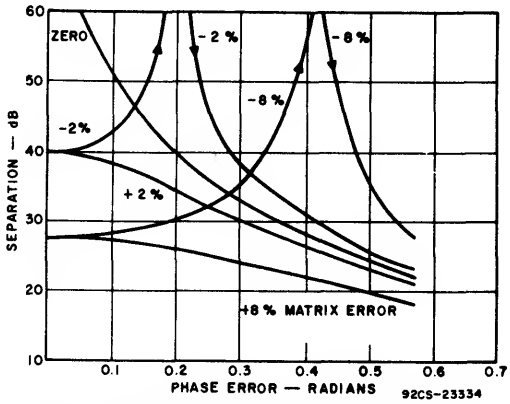

Fig. 11 — Separation as a function of static phase error and matrix error.

APPENDIX B

Doubly-Balanced Phase-Detector

A doubly-balanced phase detector is sketched in Fig. 12(a). The pilot-tone is present as the bases of the lower transistors Q19 and Q27, which are operating linearly. The bases are driven at opposite phases of the phase splitter (Fig. 7). The voltages E_1, and $\bar{E}_1$, are derived from the counter and are assumed large enough to gate transistors Q20, Q21, Q25, Q26 on and off. Thus, if the period is T and $E_2 = E_2' \sin(\omega_o t + \theta)$, emitter currents at half cycles are given by

$$\left[I_{Q20}\right]_0^{T/2}=\frac{E_2}{R_1};\ \left[I_{Q20}\right]_{T/2}^{T}=0;\ \left[I_{Q21}\right]_0^{T/2}=0;\left[I_{Q21}\right]_{T/2}^{T}=\frac{E_2}{R_1};$$
$$\left[I_{Q25}\right]_0^{T/2}=-\frac{E_2}{R_1};\ \left[I_{Q25}\right]_{T/2}^{T}=0;\ \left[I_{Q26}\right]_0^{T/2}=0;\left[I_{Q26}\right]_{T/2}^{T}=-\frac{E_2}{R_1} \quad (14)$$

where R1 is the effective value of the emitter resistor. The DC output (E_3 - E_4) is the average of the currents in the load resistors R2, integrated over one cycle as follows:

$$I_{Q20(AV)}=\frac{1}{T}\int_0^{T/2} I_{Q20}dt=\frac{E_2'}{R_1\pi}\cos\theta$$
$$I_{Q21(AV)}=\frac{1}{T}\int_{T/2}^{T} I_{Q21}dt=-\frac{E_2'}{R_1\pi}\cos\theta \quad (15)$$

and similarly

$$I_{Q25(AV)}=-\frac{E_2'}{R_1\pi}\cos\theta;\ I_{Q26(AV)}=\frac{E_2'}{R_1\pi}\cos\theta$$

Summing these currents, the detected output is given by

$$E_4-E_3=\frac{4E_2'R_2}{R_1\pi}\cos\theta \quad (16)$$

In this case, E_2 is the peak value of the 19-kHz pilot tone on the line. The effective value of the emitter resistor R_{eff} in the actual circuit (Fig. 12(b)) is given by:

$$R_{eff}=\frac{R_e R_{1\text{-}2}}{2R_e+R_{1\text{-}2}} \quad (17)$$

Loop Operation

Phase-locked loops, derivations and theory, are covered in the references 2, 3, and 4. Terminology used in this paper will conform to that in reference 2.

The differential equation governing the loop behavior is

$$\Delta\omega=\omega_P-\omega_{VCO}+F(s)\,S\,E_{3\text{-}4}\cos\theta \quad (18)$$

where $\Delta\omega$ is the difference between the free-running frequency of the controlled-oscillator, the reference signal θ is the phase difference between the reference signal and the instantaneous frequency of the controlled oscillator, ωp is the reference frequency; ωVCO is the VCO frequency; F(s) is the transfer function of the control network; E3-4 cos θ is the output of the phase detector and is $4E_2R2/R1\pi\cos\theta$; and S is the sensitivity of the VCO in radians/second/volt (see Appendix C).

The steady-state solution of the system is as follows:

$$\cos\theta = \frac{\Delta\omega R_1\pi}{4E_2'R_2S} \tag{19}$$

The steady-state phase error θ_{SS} is $\frac{\pi}{2} - \theta$ or

$$\sin\theta_{SS} = \frac{\Delta\omega R_1\pi}{4E_2'R_2S} \tag{20}$$

Because the maximum value that the sine can assume is one, the maximum hold-in is as follows:

$$|\Delta\omega_{hold\text{-}in}| \leq \frac{4E_2'R_2S}{R_1\pi} \tag{21}$$

In the case where the loop filter is a simple lag network, $\tau = RC$ and $F(s) = 1/1 + \tau s$, the capture range (pull-in) approaches the hold in range as τ becomes smaller. At the edge of the lock range pull-in is assured for[3]

$$\sqrt{\frac{1}{\tau}\cdot\frac{4E_2'R_2S}{R_1\pi}} \approx 1.2 \tag{22}$$

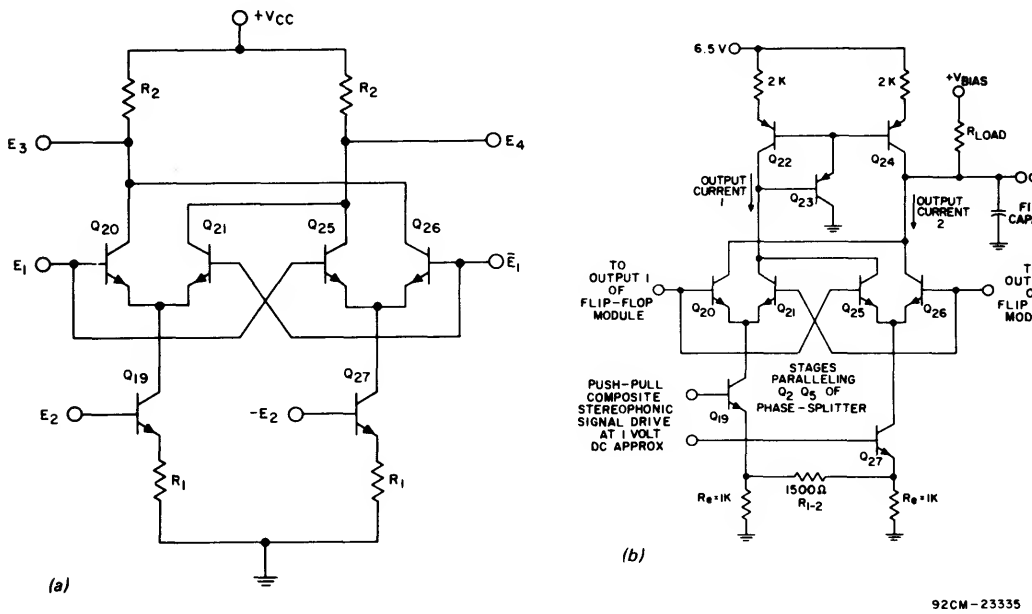

Fig. 12(a) – Doubly-balanced phase detector used for purposes of analysis and (b) actual IC phase detector.

APPENDIX C

VCO Sensitivity

By reference to the schematic representation of the reactance circuit in Fig. 13 the admittance Y at the collector of Q2 is found to be

$$Y = \frac{1}{j\omega L} + j\omega C + \frac{KA}{1 + A(1 - K)}\cdot\frac{1}{j\omega L} \tag{23}$$

From this expression the resonant frequency is found to be

$$\omega = \omega_o\left[\frac{1 + A}{1 + A(1 - K)}\right]^{1/2} \tag{24}$$

where ω_o is the resonant frequency of just the passive components, A is the loop gain of the internal circuit (α of transistor Q3 is assumed to be very close to one), and K is a fraction of the current from the current source Ail. The rate of change of ω with respect to K is given by

$$\frac{d\omega}{dK} = \frac{\omega_o A}{2(A + 1)}\left[\frac{1 + A(1 - K)}{A + 1}\right]^{-3/2} \tag{25}$$

The change in the frequency must be defined in terms of the control voltage from the phase detector, which is the differential voltage between the bases of Q1 and Q2.

The expression for K is found from the standard differential amplifier equations given as:

$$K = \frac{1}{1 + \exp.\left[\frac{V_{BE_1} - V_{BE_2}}{kT/q}\right]} \quad (26)$$

If $VBE_1 - VBE_2$ is designated as the differential control voltage, V and kT/q is set equal to 26 millivolts at 25°C, then the differentiated Eq. 26 becomes

$$\frac{dK}{dv} = \frac{-\frac{1}{26}e^{V/26}}{(1 + e^{V/26})^2} \quad (27)$$

At balance condition when V = 0, K = 1/2 and $\frac{dK}{dv} = -\frac{1}{104}$

The value of A may be calculated without direct measurement by solving Eq (24) knowing both ω and ω_o, as follows:

$$A = \frac{1 - \frac{\omega^2}{\omega_o^2}}{\frac{\omega^2}{\omega_o^2}(1 - K) - 1} \quad \text{and} \quad A = \frac{2\left(1 - \frac{\omega^2}{\omega_o^2}\right)}{\frac{\omega^2}{\omega_o^2} - 2} \quad \text{at balance} \quad (28)$$

The rate of change of ω with respect to v is given by

$$\frac{d\omega}{dK}\frac{dK}{dv} = \frac{\omega_o A}{2(A+1)}\left[\frac{1 + A(1 - K)}{A + 1}\right]^{-3/2} \times \frac{\frac{1}{26}e^{V/26}}{(1 + e^{V/26})^2} \quad (29)$$

By use of Eq 28 at balance and substituted into Eq 29, a typical unit in which the resonant frequency of the passive components equals 59-kHz (and f = 76-kHz), df/dv is found to be 442 Hz per millivolt. This value is the constant S of the Appendix B.

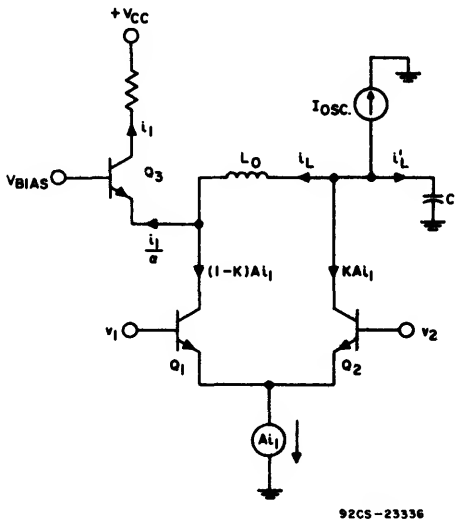

Fig. 13 – Reactance circuit.

ACKNOWLEDGEMENT

The authors acknowledge the work of Mr. B. Zuk, RCA Solid State Division, who is responsible for invention of the DC coupled flip flop and the preamplifier phase splitter described in this paper.

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Description and Application Of The RCA CA3120E and CA3142E Integrated-Circuit TV-Signal Processors

by W. Sensenig

The RCA CA3120E and CA3142E are 16-pin, dual-in-line, monolithic-silicon integrated circuits that process a video signal and provide the following outputs:

Non-inverted video output
Noise-processed, inverted video output
Dual-polarity, composite synchronization signals
Automatic gain-control signals:
- Undelayed forward agc for if amplifier
- Delayed forward agc for tuners with bipolar transistors
- Delayed reverse agc for tuners with FET's

The IC's, which can be used in color or monochrome TV receivers, require a single-polarity power supply (positive) and include impulse noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimum TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

CIRCUIT DESCRIPTION

Fig. 1 is a simplified block diagram of the CA3120E and CA3142E signal processor; the circuit consists of four major blocks:

1. Noise processor circuit
2. AGC circuit
3. Synchronizing separator circuit
4. Internal dc reference supplies

An emitter-follower output is also provided for the unprocessed video signal (non-inverted). The four circuits are used to generate the output sync and agc signals as described below.

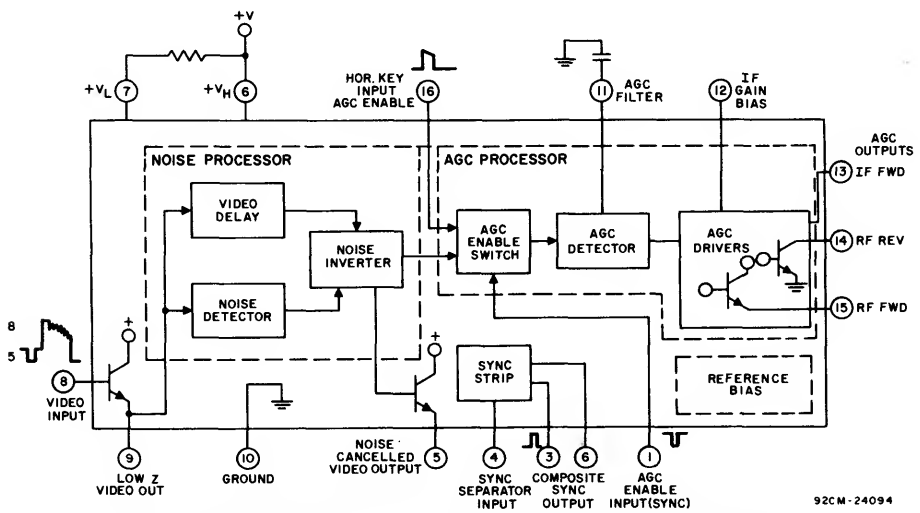

Fig. 1 – Simplified block diagram of the CA3120E and CA3142E signal processors.

Noise Processor

The function of the noise processor is to reduce the effect of impulse noise interference (from automobile ignition, etc.) on the agc and synchronizing circuits of the TV receiver. Fig. 2 is a simplified schematic diagram of the noise processor. The input video signal applied at terminal 8 is white, positive-going with sync tips at V_{TH} (the agc threshold-voltage level), which is approximately 5 volts. The unprocessed video output signal from the emitter of Q1 is available at terminal 9. The video signal from the emitter of Q1 is also connected to the base of Q2. In the absence of any negative-going noise pulse, Q2 functions as an emitter follower, and transistors Q3, Q5, and Q12 are cut off. The output of emitter-follower Q2 is connected to the video RC delay line consisting of R42 through R49 and the emitter base capacitors of multiple-emitter transistor Q6.

The delayed video signal (delay is approximately 300 nanoseconds) at the emitter of Q14 is shown in Fig. 3(b). If negative-going impulse noise crosses the noise threshold voltage (approximately 1.8 volts below V_{TH}), transistor Q3 conducts and turns on transistors Q5 and Q12. Transistor Q5 generates a noise-cancelling pulse whose duration is approximately 500 nanoseconds wider than the detected noise pulse, as shown in Fig. 3(d). Pinch resistor R7 limits the amplitude of the generated pulse. Transistor Q17 limits the amplitude of the impulse noise through the delay channel, as shown in Fig. 3(b).

The delayed video at the emitter of Q14 and the generated noise pulse are summed at the input to current amplifier Q15, Q16. Transistor Q16 inverts and amplifies the noise-processed video signal. Since the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been stretched approximately 500 nanoseconds, the output of the combined signal (at emitter follower Q57) no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise, as shown in Fig. 3(f).

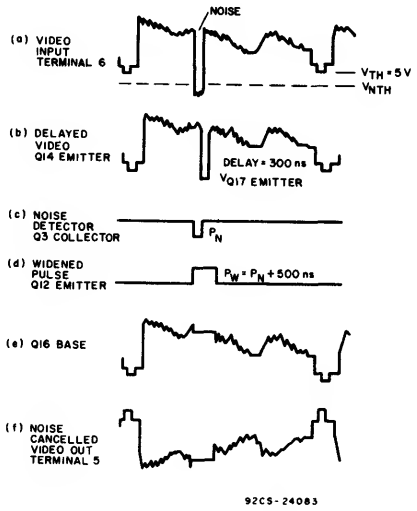

Fig. 3 — Operating waveforms for the noise processor.

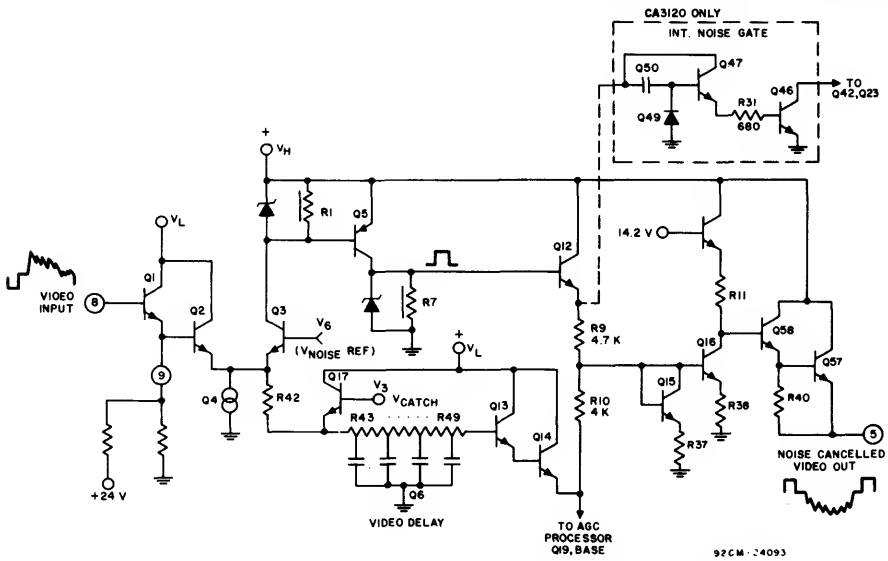

Fig. 2 — Simplified schematic diagram of the noise-processor section of the CA3120E and CA3142E.

After amplification, inversion, and buffering, the noise-processed video signal is available at terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the signal is approximately twice the amplitude of the video signal at terminal 8. The dc level of the sync tip at terminal 5 is approximately 8.5 volts. The agc generator uses the delayed video to generate the agc voltage. In the CA3120E only, an ac-coupled noise gate disables the agc generator for approximately 10 microseconds under heavy noise conditions. The noise gate from the emitter of Q12 is connected to transistor Q50, which acts as a monolithic capacitor. Q49 is used as a dc restorer. Emitter follower Q47 feeds control transistor Q46, which disables the agc generator for the duration of the noise gate pulse. AC coupling is used to prevent agc lockout.

AGC System

The function of the agc system is to provide control voltage to the if and tuner stages of the TV receiver, the amount of voltage is a function of the amplitude of the detected video signal; thus a constant-amplitude video signal is maintained.

The CA3120E and CA3142E agc amplifiers use a sample and hold system to develop the required agc bias voltages. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. A coincidence-gate circuit is included to compare the timing of the synchronizing pulse with a horizontal keying pulse derived from the horizontal flyback transformer.

Fig. 4 is a simplified schematic diagram of the agc generator. The delayed video signal from the emitter of Q14 is connected to the base of the agc-gated comparator-amplifier Q19, Q20. In normal operation, Q21 is turned on during the horizontal retrace period, thus enabling the comparator, and the dc level of the sync tip is compared to reference voltage V5. The difference between the sync and reference voltages is amplified and fed to current amplifiers Q24, Q25. The output of Q25 is used to charge the external agc filter capacitor connected to terminal 11. Transistor Q23 is also gated on during the retrace interval, and provides a constant rate of discharge to the agc filter capacitor connected to terminal 11. The net capacitor charge is the difference between the charge current and the discharge current for a given offset voltage condition at the comparator. If the antenna signal

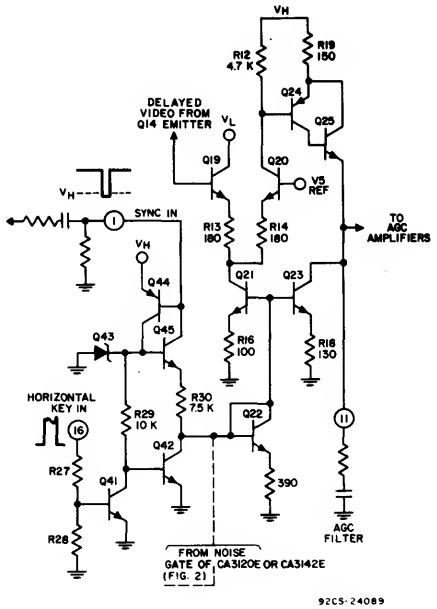

Fig. 4 — Simplified schematic diagram of the agc generator.

decreases to a lower level and is held constant, the detector output voltage will decrease; this decrease in the voltage causes the charge current to decrease. As the capacitor is discharged, the TV-system gain is increased to the value where equilibrium is reached, and the charge current again equals the constant discharge current. Since the discharge current is constant, the same offset voltage will appear at the comparator. By this action, the offset between the sync tips and the agc threshold is held nearly constant.

To provide noise immunity for the agc system and to assure that only the delayed-video sync tips are sampled, agc strobing is employed. This technique prevents the detected video from being sampled by the agc comparator when the TV system is out of horizontal sync, as a result of changing channels for example. If the video were sampled with the TV system out of horizontal sync, the detector output would contain picture modulation components which would cause horizontal-synchronization problems. This effect grows worse as the agc time constant is reduced to provide the rapid agc action required to counteract doppler modulation of the TV signal resulting from multipath reflections of aircraft.

The agc coincidence strobing system is also shown in Fig. 4. Negative sync signals are ac coupled to the latch circuit con-

sisting of Q44, Q45, and Q43. The tip of the sync signal is clamped at the base potential of Q44, which is one V_{BE} below the supply voltage V_{CC}. During the sync period when Q44 is turned on, the base potential of Q45 is increased to the zener voltage of Q43 (approximately 7 volts). A current of approximately 0.8 milliampere then flows from the emitter of Q45 through R30. If the horizontal key pulse is not simultaneously present, this current is bypassed through transistor Q42 to ground, and the agc comparator remains off. The agc filter capacitor remains at its original potential.

Under conditions of synchronization, transistor Q41 is turned off, and the current from Q45 through R30 is diverted to current mirror Q22. Constant-current transistor Q21 and Q23 are turned on, thus enabling the agc comparator and the filter-capacitor charge/discharge current generators. To prevent agc lockout during turn-on or channel changes, ac coupling must be employed to sync input terminal 1.

The agc output stages are shown in Fig. 5. The agc filter-capacitor voltage at terminal 11 is connected to Darlington transistors Q28 and Q29. A bias voltage applied at the base of transistor Q26 (terminal 12) will set the minimim voltage on the filter capacitor connected to terminal 11. The potential at terminal 11 (minus $1V_{BE}$) is transferred to the emitter of p-n-p transistor Q31 and terminal 13, the forward agc output terminal for the if amplifier. The potential at terminal 12 is selected by the TV receiver designer to provide the "no-signal", maximum, if gain bias. As the TV input-signal amplitude increases, the potential at terminal 11 rises, and forward bias is applied to the receiver if amplifier from the emitter of Q31 at terminal 13. Tuner delay bias is also applied to the emitter of Q31 at terminal 13. As shown in Fig. 6, no change in output voltage occurs at terminal 14 or 15 at the low and intermediate signal-level conditions represented by abscissa points A and C. The tuner(s) will operate at maximum gain and provide good signal-to-noise ratios at these equivalent input-signal levels.

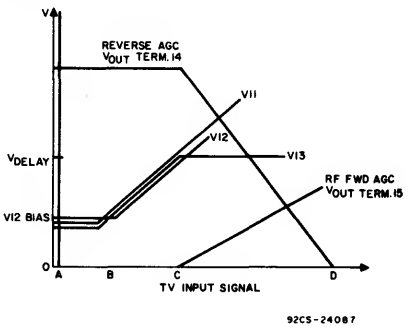

Fig. 6 – AGC transfer curves.

Point C, Fig. 6, is a turnover point determined by the open-circuit potential of the tuner delay-bias voltage divider. As shown in Fig. 5, the voltage divider acts as a load for emitter follower Q31. As long as the emitter of transistor Q29 is at least one V_{BE} drop less than the open-circuit delay-bias voltage, transistor Q31 performs as an emitter follower, and forward-if control voltage is developed. At higher signal levels, the voltage at the emitter of Q29 increases and Q31 turns off; further

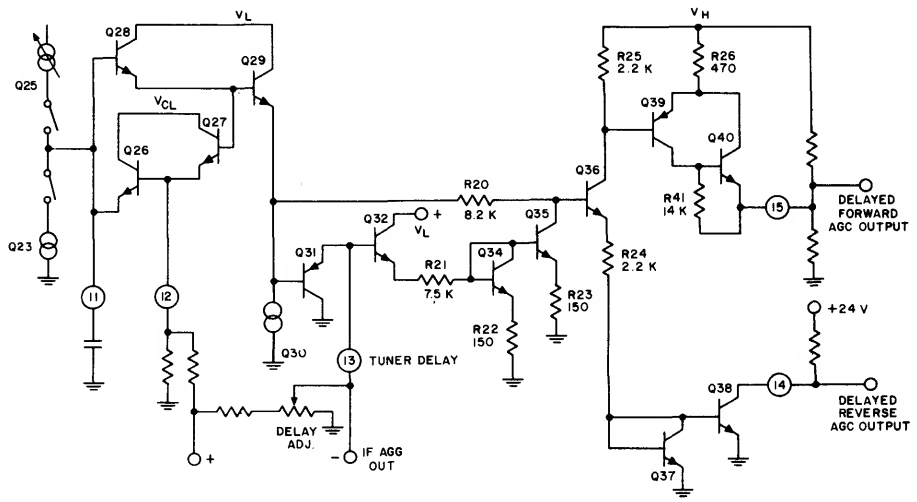

Fig. 5 – AGC output stages.

change in the if agc output is inhibited (for good dynamic range) and the forward and reverse agc outputs of the turner are activated (represented by points C and D in Fig. 6). As shown in Fig. 5, at signal levels below the turnover point, the emitter potential of Q32 is equal to and follows the emitter potential of Q29. Above the turnover point, the emitter potential of Q32 is fixed by the tuner-delay voltage divider, and consequently the current of transistor Q35 is fixed, as determined by mirror-transistor Q34. Further increases in signal level turn on amplifier Q36, which in turn drives the two agc output amplifiers in the tuner. Transistors Q39 and Q40 provide the delayed forward agc output at terminal 15 for use with tuners using n-p-n transistors. Transistors Q37, Q38 provide the reverse agc output at terminal 13 for use with tuners using MOSFET's or vacuum tubes. Note that in forward-type agc systems, increased signal into the tuner results in increased agc voltage. The increased agc voltage decreases the gain of the amplifier by reducing the collector-to-emitter voltage of the amplifier as a result of the increased base-to-emitter potential. In reverse-type agc systems, increased signal into the tuner results in decreased agc voltage. The decreased voltage reduces the transconductance of the amplifier, thus reducing its gain.

Sync Separator

The schematic diagram of the sync separator is shown in Fig. 7. The sync-separation stage Q56 clamps the sync tips

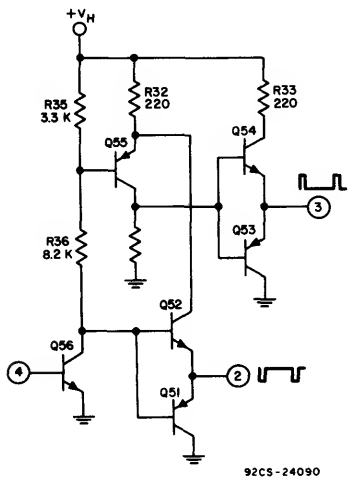

Fig. 7 – Schematic diegram of the sync separator.

to the forward bias reference potential (approximately 0.7 volt) of the base-emitter junction, and amplifies the stripped portion of the sync signal to provide dual-polarity sync-signal outputs at terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance, complementary, emitter-follower stages. Full-amplitude sync signals are generated if the input signal current at terminal 4 is 100 microamperes.

Reference Bias

The excellent performance of the CA3120E and CA3142E is based upon matching of V_{BE} voltage drops and control of voltage references and resistance ratios. Fig. 8 is a simplified schematic diagram of the reference-bias supplies.

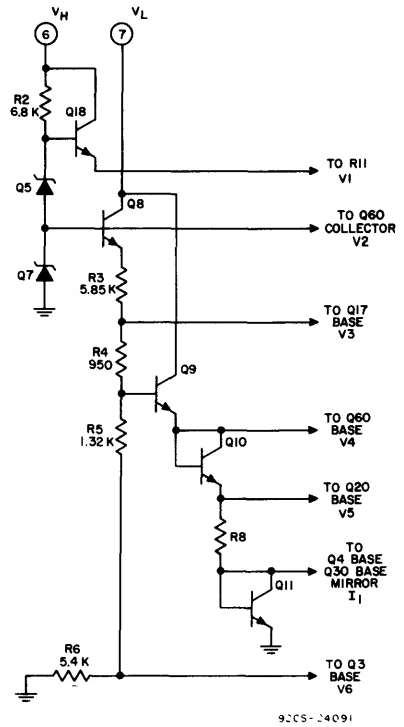

Fig. 8 – Simplified schematic diegrem of the reference-bias supplies.

APPLICATION OF THE CA3120E AND CA3142E

Fig. 9 shows a typical application for the CA3120E and CA3142E. The video input at terminal 8 is direct coupled to the second detector of the TV receiver. The video signal should be white positive and

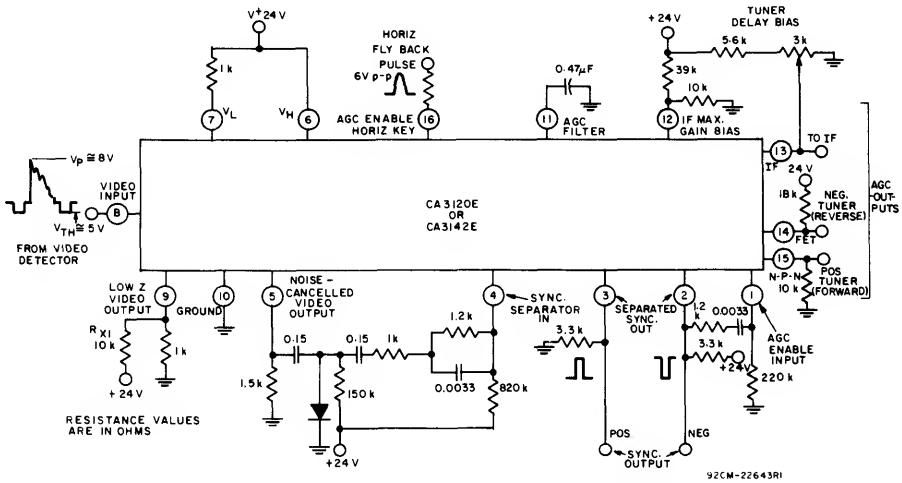

Fig. 9 — Typical application of the CA3120E and CA3142E.

have an amplitude of approximately 3 volts peak-to-peak. The dc level of the sync tips, agc threshold voltage (V_{TH}), is approximately 5 volts. This level will be maintained by the closed loop of the agc system which includes the CA3120E and the receiver rf and if amplifiers.

Fig. 6 illustrates the operation of the agc circuits. Under very-low amplitude (or zero amplitude) signal conditions, terminal 12 is biased to approximately 4.9 volts by the voltage-divider network at terminal 12. The agc filter capacitor (at terminal 11) is charged to a potential one V_{BE} below the bias potential. The if-agc output level at terminal 13 is two V_{BE} drops (approximately 1.4 volts) below the bias voltage on terminal 12. This bias voltage represents the maximum receiver-gain condition. As the input signal is increased (represented by line-segment BC in Fig 6) the capacitor is charged to a higher potential and the if-agc control potential at terminal 13 also increases, thus applying forward agc to the if amplifier, as shown in Fig. 10. The rf stage of the tuner operates at maximum gain for best signal-to-noise ratio as the if stage gain is reduced by forward bias. Point C in Fig. 6 is the agc-delay turnover point determined by the open-circuit potential of the voltage divider connected to terminal 13. At this potential, further reduction in the if-agc gain is inhibited (for good dynamic range) and the tuner agc is activated (represented by line segment CD in Fig. 6).

The agc output at terminal 14 is used for tuners employing reverse agc, such as those incorporating MOSFET's, as shown in simplified form in Fig. 10. The agc at terminal 15 is used for tuners employing n-p-n bipolar transistors requiring forward bias for the agc gain reduction, also as depicted in Fig. 10. The value of the agc filter capacitor is determined by the maximum rate of gain change desired; a typical value is 0.47 microfarad. The detector must be pre-biased, as shown in Fig. 10. With no signal (no carrier) the bias potential should be approximately 8 volts.

The available ratio of charge current to discharge current for the agc filter capacitor during the keying intervals is approximately 12 to 1. The nominal peak charging current available is 20 milliamperes. The voltage applied to terminal 12 should not exceed 5.2 volts; the maximum open-circuit delay-bias voltage applied to terminal 13 should not exceed 10 volts. In typical designs, V12 is operated at approximately 2 to 5 volts, and the open-circuit bias voltage at terminal 13 is set to approximately 6 volts.

Transistor Q38, (Fig. 5), connected to terminal 14 (reverse agc output for tuners), can typically sink 3.5 milliamperes. The typical forward agc current available at terminal 15 (supplied by Q40) is 10 milliamperes.

Sync Separator

Fig. 11 shows a simplified schematic diagram of the sync separator and its equivalent circuits. The choice of the coupling network from the noise-cancelled video output at terminal 5 to the sync-separator input at terminal 4 is a user option. Fig. 12 shows three typical coupling networks. The choice of the

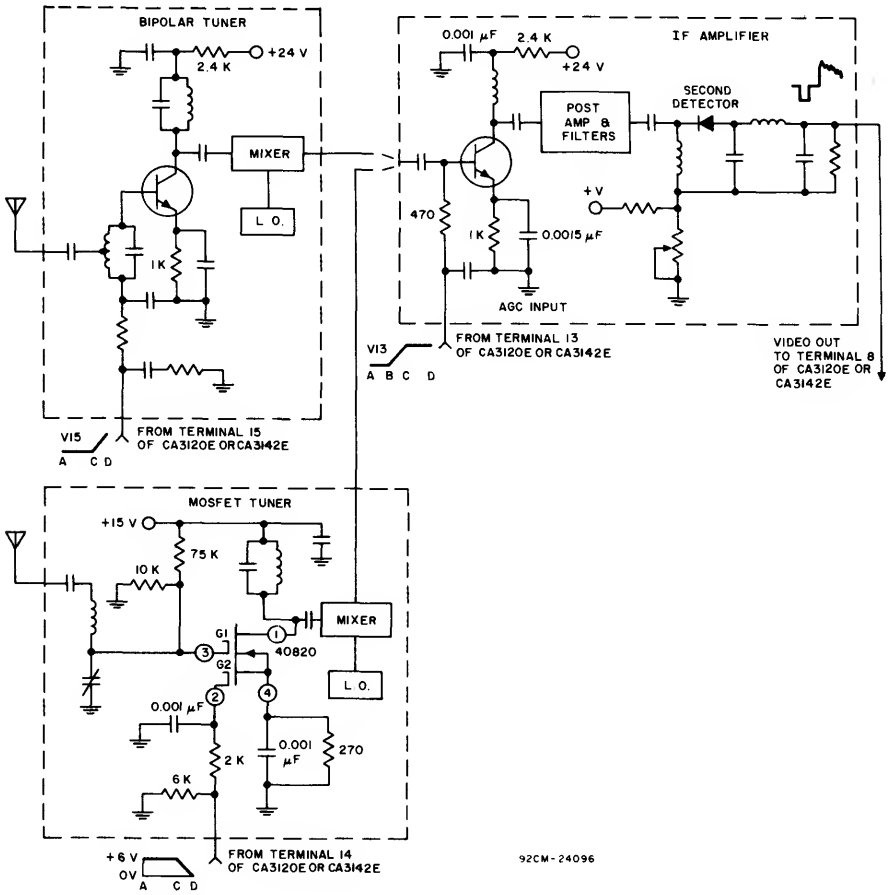

Fig. 10 – Interface of if amplifier with bipolar and MOS FET tuners.

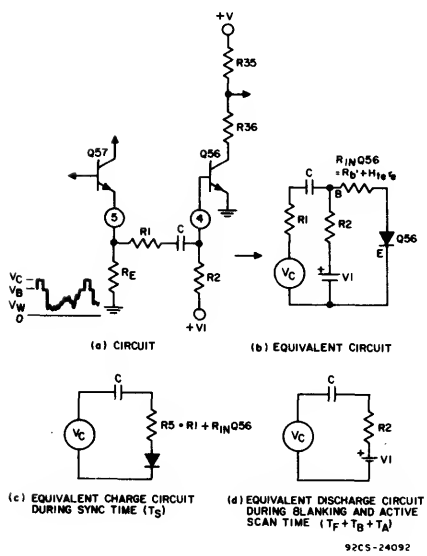

Fig. 11 – Simplified schematic diagram of the sync separator and its equivalent circuits.

network depends on the anticipated input signals. In an NTSC TV signal (see Fig. 13) the sync tips are at peak voltage (and power). Blanking level is at 75 percent, black level is approximately 70.3 percent, and white level is 12.5 percent. The gray level varies between black and white levels.

The function of the sync separator is to take a portion of the sync signal at a level between the sync tips and the blanking level and generate a local sync signal for the deflection circuits of the TV receiver. By choosing the proper portion of the sync signal, the effect of thermal noise or distortion on the sync tips is minimized, and the sync signal is freed of contamination by the video signal.

As shown in Figs. 7 and 11, the sync separator is the base-to-emitter junction of transistor Q56. Base current flows when the application of a positive sync signal from terminal 5 produces a charge on the external coupling capacitor. During the remaining period of time, the base current

ceases and the capacitor discharges through the bias and source resistors. The ratio of the charge current to the discharge current sets the bias potential (i.e., sync clamp level).

During the sync period, the transistor should be saturated (i.e., removing noise existing at sync tips); during the remaining blanking and active scan period, the transistor should be cut off, thus removing video contamination from the amplified sync pulse. To prevent a large shift in the bias level during the vertical sync interval, the time constants must be large.

Other factors affecting the design of the sync separator are the effects of doppler flutter of the input signal caused by aircraft. If the time constant is excessive, some of the sync pulses may be clipped off; if the time constant is too short, the vertical sync can cause trouble. This problem may be solved by connecting a multiple-time-constant network between terminals 4 and 5 of the CA3120E or CA3142E, as shown in Fig. 12. These

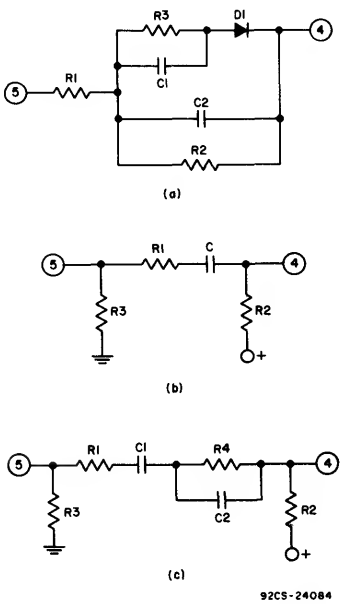

Fig. 12 – Typical coupling networks.

networks also reduce the effect of impulse noise from hand drills, etc. The short time-constant section of the network allows rapid recovery after a noise burst of long duration, while the long time-constant prevents degradation resulting from short, individual noise pulses. As shown in Fig. 12(a) diodes may also be used to improve the performance of the separator: the diode is used to isolate the coupling capacitors and enhance the operation of the double-time-constant coupling network. In closed-circuit TV systems in which impulse noise or aircraft doppler flutter is not a problem, the simple network described above and shown in Fig. 12(b) may be used.

The optimum clamp level is usually chosen as 30 to 60 percent of the actual sync amplitude (C-B in Fig. 13) to prevent thermal noise on the sync tip from degrading the derived sync signal. The

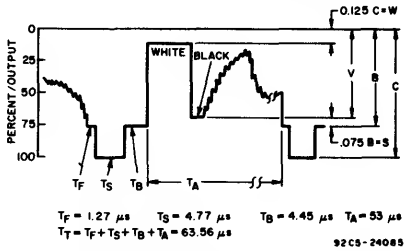

Fig. 13 – Video waveforms.

amplitude of the sync signal at terminal 5 is approximately 1.5 volts for a 2-to 3-volt peak-to-peak video signal at terminal 8. This choice also prevents overshoots on blanking from generating spurious sync pulses. Since, in most cases, thermal noise is more tolerable than video contamination, it may be preferable to place the clamp level nearer to the sync tip. This arrangement reduces the susceptibility of of the system to any residual color-burst signals, and is more suitable for use with some industrial TV-camera systems which may not include any set up (blanking level to black level) in the video. The clamp level will shift somewhat as a result of scene changes; but the shift can be minimized by returning the external bias resistor R2 to V_{CC} (Fig. 11), since this results in a much higher ratio of discharge to charge resistance. For example, if V1=0, the resistance ratio is only 120; if the bias resistor is returned to V1=+24 volts, the ratio is greater than 1100. As can be deduced from the above, the change in clamp level for white to black scenes is greatly reduced by returning R2 (Fig. 11) to the 24-volt supply, provided the supply is relatively stable.

If the clamp level is to be set for an all-white signal at 50 percent (CL=0.5) down from the sync tip, then, in Fig. 11, $R5 = [0.5(V_C-V_B)-V_{4on}]/I_4$. Since I_4 is typically 70 microamperes, V_{4on} is approximately 0.7 volt, and V_C-V_B at terminal 5 is approximately 1.5 volts; therefore:

$R5 = [0.5(1.5) - 0.7] / 70(10^{-6}) = 714$ ohms

This value of resistance includes the output resistance of emitter-follower Q57 and the input resistance of Q56. The output resistance of Q57 is low, approximately 5 ohms. The input resistance of Q56 at the threshold of saturation is approximately 500 ohms. An additional series resistance of 100 to 200 ohms may be used. Using the value of R5 calculated above, the value of R2 returned to +24 volts may be calculated (Figs. 11, 13):

$$\frac{R2 + R5}{R5} \cong \frac{T_T}{T_S} \times \frac{V_1}{CL(V_C - V_B)} \cong 13.3 \times \frac{24}{0.5(1.5)}$$

R2 ≅750 kilohms.

Video Application of the CA3120E and CA3142E

A sync stripper is often required when the CA3120E or CA3142E is used in industrial-TV (ITV) applications. Fig. 14(a) indicates a method of direct coupling the sync input terminal to the video signal. Note that in this arrangement the sync output polarities are opposite to those used in normal operation. Fig. 14(b) indicates the opposite phase video signal applied to terminal 5. The maximum negative potential applied to terminal 4 should not exceed 5 volts. AC coupling may be used, of course; the design of the ac coupling is the same as previously discussed.

Other video applications for the CA3120E and CA3142E include a method of reinserting the dc component of the video signal (this method is often used in "Stab-Amps"). Fig. 15 shows a possible method of using the CA3120E or CA3041E for this purpose. In the circuits, the clamp voltage is derived by the internal comparator, Q19, Q20 in Fig. 4.

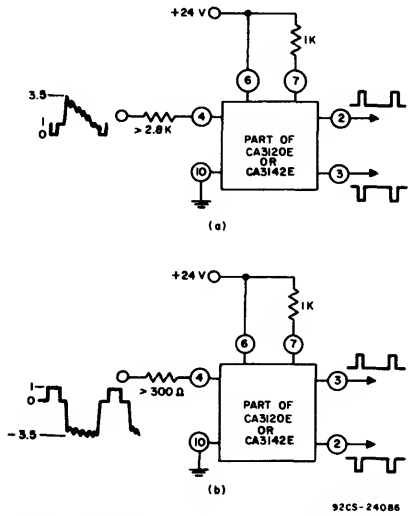

Fig. 14 – Methods of direct coupling sync input terminal to video signal: (a) white, positive; (b) white, negative.

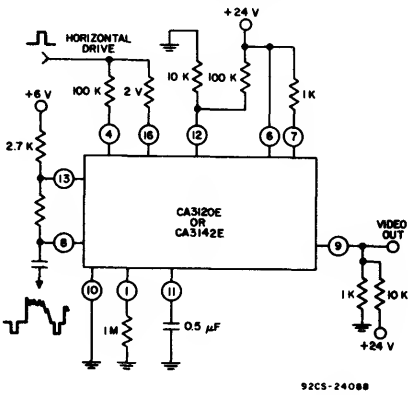

Fig. 15 – Video dc reinsertion amplifier.

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ICAN-6303

A Single IC for the Complete PIX-IF-System in TV Receivers

The RCA-CA3068 linear integrated circuit is a PIX-IF-subsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-if-system for a TV receiver. This Note* describes the receiver functions performed by the CA3068, and its application to color and monochrome TV receivers.

Specifically, the receiver functions performed by the CA3068 are:

- Video if amplification
- Linear video detection
- Noise-limited amplification of detected video
- Keyed agc, with noise-immunity circuits
- AGC delay for tuner rf stage
- Buffered output signal to drive Automatic-Fine-Tuning (AFT) circuits
- Amplification of intercarrier frequencies
- Sound-carrier detection
- Sound-carrier amplification
- Zener reference diode for voltage regulation.

The only external components required for the operation of this if subsystem are bandwidth shaping networks, biasing networks, and a power supply. A functional block diagram of the signal portion of a typical color-TV receiver is shown in Fig. 1. A detailed block diagram of the CA3068, together with its peripheral tuned-circuits, is provided in Fig. 2.

This Note contains a detailed description of circuit functions within the integrated circuit, together with examples of the use of the CA3068 in PIX-IF amplifier PC-boards for color and monochrome TV.

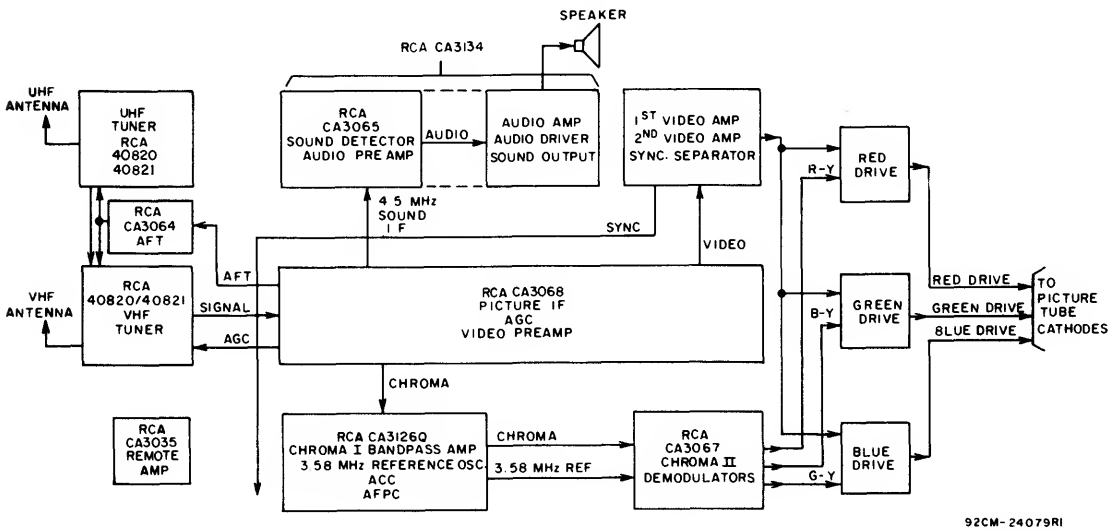


Fig. 1. Block diagram of typical color-TV signal circuits using the CA3068.

*This Note, revised by Maurice Caputo (Solid State Division), was orginally prepared by S. Reich and R. T. Peterson.

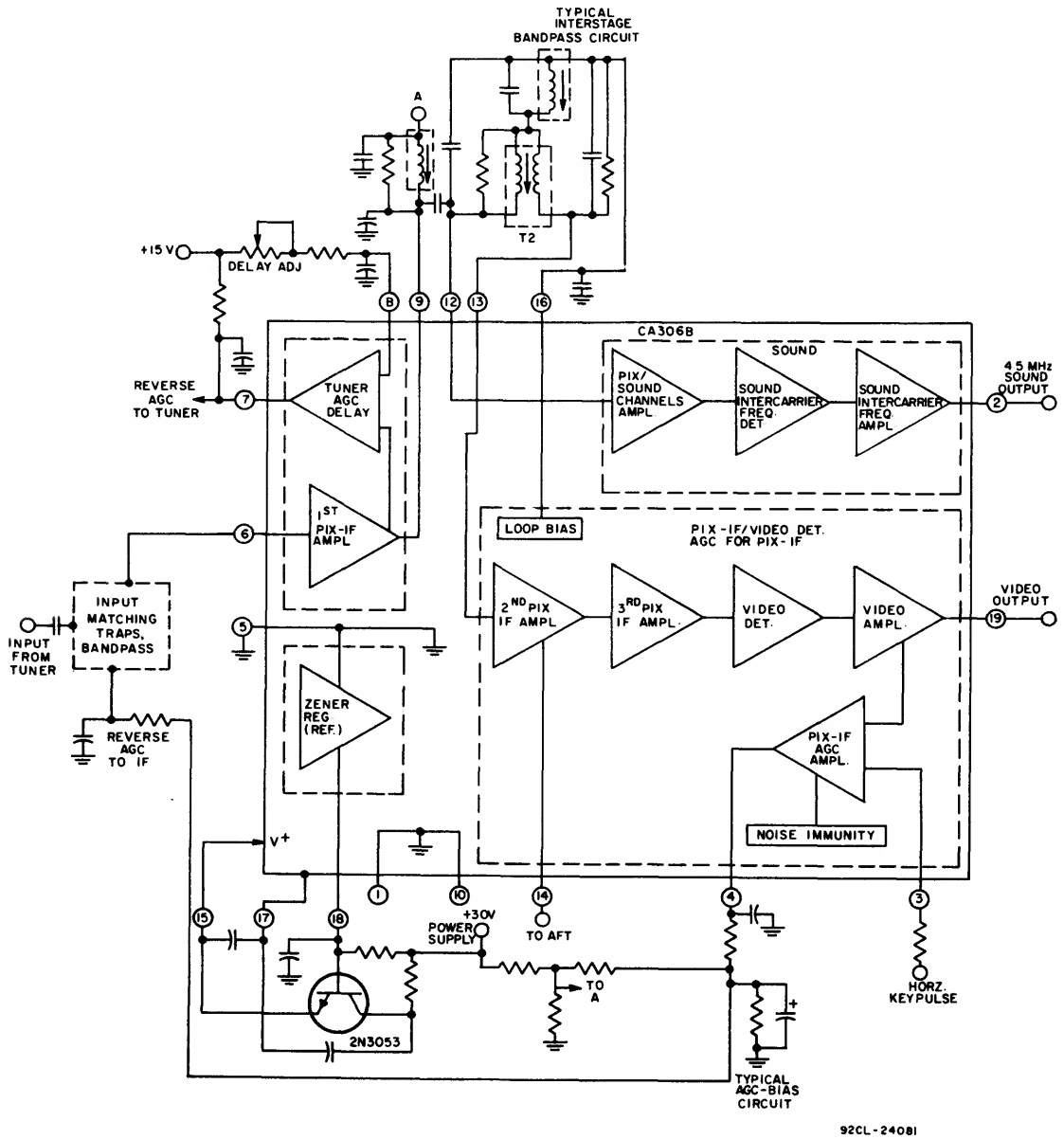


Fig. 2. Detailed block diagram of the CA3068 together with its peripheral tuned circuits.

GENERAL DESCRIPTION OF CIRCUIT FUNCTIONS IN THE CA3068

As shown in the block diagram of Fig. 2, the if signal from the tuner is applied to the input (terminal 6) of the cascode if amplifier. Output from the cascode amplifier is then coupled to a wideband amplifier at terminal 13 through the interstage transformer (T2). Under maximum-gain conditions, the over-all gain of the CA3068 is typically 75 dB at PIX-IF frequencies. This signal is then applied to a linear video detector whose output signal is fed to a video amplifier having a gain of 12 dB.

Bandpass shaping is accomplished by means of tuned-circuits preceding the input stage (terminal 6) and at the interstage circuit comprising input and output terminations via terminals 9, 12 and 13, as shown in Fig. 2. Terminal 16 is tied in at this point to provide loop bias for the input stages of the amplifiers connected to terminals 12 and 13. The agc voltage developed within the CA3068 is applied to its input stage by an external path from terminal 4 to terminal 6 through the input circuitry, as shown in Fig. 2. The developed agc is gated by a keying pulse applied to terminal 3 from the horizontal sweep circuit of the TV

receiver. Delayed agc for the rf amplifier in the tuner is obtained from terminal 7; the delay is variable by adjustment of a resistance (25 kilohms) in series with the supply to terminal 8.

The zener reference voltage for the power-supply regulating pass-transistor is developed at terminal 18 when this terminal is connected to a voltage supply through a current-limiting resistor. This resistor value should be selected to provide a quiescent current into the zener of 0.5 to 1.5 milliamperes (excluding the base current for the pass transistor).

Terminal 15 is the dc input terminal that provides power for most of the CA3068 and should be connected to the 11.2-volt regulated supply as shown in Fig. 2. The CA3068 package has a 20-lead configuration with 18 active terminals. Terminals 11 and 20 have been omitted from the package; their corresponding leads are internally connected to the shield. Terminals 1, 5, and 10 are grounding terminals. In addition, terminal 17 is at ground potential. Additional information relative to dc grounding is given in the section concerning if design.

DETAILED CIRCUIT FUNCTIONS

Fig. 3 is a schematic diagram of the CA3068. The diagram is partitioned to facilitate the explanation of the circuit configuration and its functions.

The cascode input amplifier (first if) is a unique circuit designed for dual-mode operation. At low-level input signals, the buffer stages formed by Q3 and Q4 drive the base of the cascode-if amplifier composed of Q7 and Q6. Negative-going agc applied to Q3 (through an external connection to terminal 6) increases in proportion to the increase of the input signal level. After approximately 40 dB of gain reduction is reached in this operational mode, Q7 is cut off, and its function is assumed by Q5. Emitter degeneration in Q5 increases the dynamic input range of the cascode amplifier sufficiently to cope with the higher range of input signal level. The point at which Q5 assumes the input amplifier function is sensed by Q11. It should be understood that transistors Q11, Q4, and Q7 approach cut-off at essentially the same signal level. As Q11 approaches cut-off, it draws less shunting current from terminal 8, and base current drive to Q8 is increased. The point at which sufficient base current is available to drive Q8 into conduction is determined by an external-delay agc potentiometer connected in series with the V+ supply-lead and terminal 8. As Q11 cuts-off, the voltage increases at terminal 8, and current flowing into terminal 8 is diverted to the base of Q8. When Q8 starts to conduct, it turns on Q9 and Q10, thereby causing the open-circuit voltage at terminal 7 to drop and produce a negative-going agc voltage for the rf

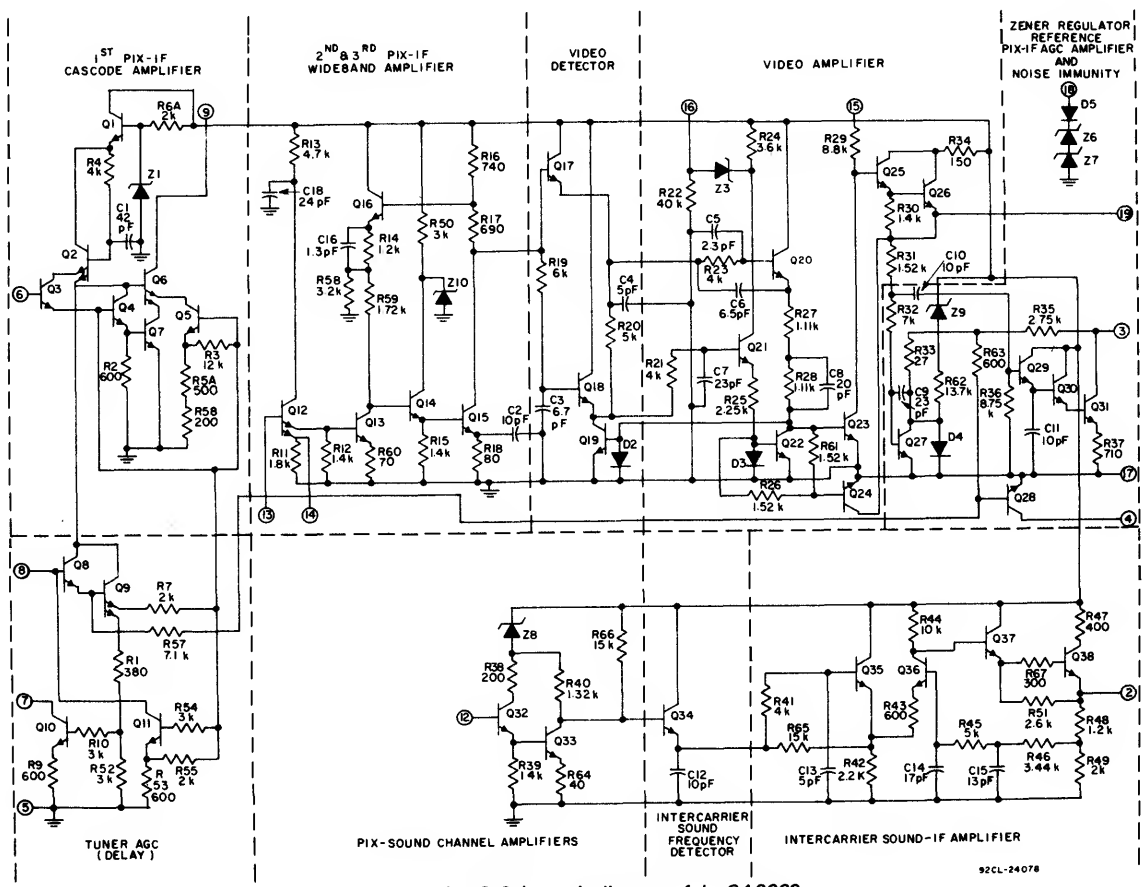


Fig. 3. Schematic diagram of the CA3068.

stage of the tuner. Q8 is also part of the if-agc feedback loop, and provides an increase in agc loop-gain. This increase compensates for the decrease in agc loop-gain that occurs when the cascode if amplifier is transitioned to its modified cut-off characteristic. After tuner gain reduction has reached its maximum, an additional 10 dB of gain reduction can be obtained in the cascode-amplifier under this modified cut-off condition.

This reverse-agc system is used for the cascode input stages because the stability achieved under maximum-gain conditions is maintained throughout the range of agc functioning.

The wideband if amplifier consists of transistors Q12, Q13, Q14 and Q15. Q12 serves as a buffer stage between the interstage tuned-circuits and the automatic-fine-tuning (AFT) output-signal terminal. The actual if signal amplification takes place in Q13, Q14 and Q15, which effectively serve the function of second and third PIX-IF stages. Transistor Q15 is the driving source to Q17, the video detector. This driving source impedance is approximately 500 ohms as a result of the degenerative feedback loop through Q16. The feedback network also extends the 3-dB-down frequency response to beyond 70 MHz. It is this low detector-driving-point impedance and the absence of a tuned-circuit at this interstage point that contribute to the superior performance of the detector system. In most conventional detection systems, the detector is driven from a high-impedance source involving a double-tuned interstage transformer with unequal primary and secondary Q's. In such a system, variations in detector impedance (caused by normal video excursions) can produce significant phase shifts that adversely affect color fidelity. In the CA3068, the untuned, low-impedance detector drive circuit produces a nearly optimum condition for the detector circuit.

The detector circuit consists of transistor Q17 and its biasing network Q18, Q19 and R20. Q18 is biased to the same potentials as Q17 because the bases are tied together through the resistance element of the low-pass filter that consists of R19 and C3. R20 and C4 form a conventional peak detector in which the time constants are selected for optimum detector efficiency and desired video bandwidth. This system detects chroma subcarrier without introducing differential phase errors as a function of the video signal, and detects the video signals with a minimum of amplitude distortion. The low signal-level requirements for the detector, the absence of tuned-circuits in the detector drive circuit, and the low source impedance for the detector, all contribute to the superior detector performance.

The video detector is direct-coupled to the video amplifier. Consequently, a dc input voltage above the level of one V_{be} (0.7 volt) drop at the input to Q23 determines the condition for white level (dc) at the output (terminal 19). It is necessary, therefore, to bias Q23 to the threshold of conduction in the absence of detected video. This function is accomplished by the differential-amplifier circuit arrangement consisting of transistors Q20 and Q21. In the absence of signal, the dc potentials at the emitters of Q20 and Q21 are identical. The current through Q20 must equal the current through Q21 because R25 is similar in value to (R27 + R28). This current also flows through D3 (which has the same geometry as Q22). Consequently, Q22 carries all the current supplied by Q20, and no current is available for the base of Q23, so that Q23 is held on the edge of conduction. When an rf carrier is present, the current in Q20 increases in direct proportion to the carrier level; however, the current in Q21 remains fixed. When the current increases in Q20, this increase can only flow to the base of Q23. Since the current in Q23 is directly proportional to its base current flow, a corresponding increase in current through Q20 as a result of rf carrier detection produces a video output at terminal 19.

As the video carrier signal increases, the dc level at the base of Q23 increases, and there is an accompanying decrease in the dc level at the base of Q25 and, consequently, at terminal 19. With a sufficiently strong rf signal, the current through Q23 and R29 increases such that the base voltage of Q25 is driven toward dc ground. The "bottoming" level at terminal 19 under nominal signal conditions is locked to about 0.8-volt as a result of the high loop gain of the agc system. Any further increase in the signal, after "bottoming" is reached, will be clipped. This operational feature serves as a highly effective mechanism to limit impulse noise.

When a signal is present at the input, the composite video signal at the base of Q25 appears at terminal 19 through the Darlington connection to the emitter of Q26. The sync tips in this composite waveform drive the keyed agc amplifier Q27, which in turn drives Q28. Without a video rf signal there is no video signal output, and Q27 conducts during the keying intervals (the horizontal pulse is connected to terminal 3). As the detected signal level increases in amplitude and the output voltage at terminal 19 approaches its typical operational level of 7 volts peak-to-peak, the peak potential at the base of Q27 begins to fall below 0.8 volt. Under these conditions, the keying current formerly channeled through Q27 is diverted through diode D4. As the signal level rises even higher, a greater portion of the Q27 collector current is diverted through D4, and the base current to Q28 is proportionately increased. A 10-microfarad capacitor is normally connected between terminal and ground and is, by this connection, put in shunt with Q28. The charge on this external capacitor is maintained through a bleeder resistor to V+. As the base current to Q28 increases, Q28 discharges the capacitor at a rate that is proportional to the base current of Q28. Integration of the total charge on the capacitor over the keying interval yields a dc level (agc voltage) that is inversely proportional to the incoming signal level; i.e., agc voltage approaches zero as the signal increases.

Any high-performance agc system must have noise-immunity characteristics in order to avoid the establishment of false agc levels. AGC voltage developed from random noise can produce "wash-out", "blank raster" and/or a momentary "loss of sync". The CA3068 is designed with an improved noise-immunity circuit that essentially removes the keying current during periods of high noise input. The active devices responsible for providing protection against this deleterious effect of the impulse noise are the "noise detector", Q29, and the "noise clamp" Q31, which is driven by Q30. Impulse noise is channeled through the high-pass filter network consisting of C10 and R36 to the detector input Q29. Q29 and C11 comprise a conventional peak detector. The dc level across C11, which is proportional to the

level of impulse noise, turn on Q30 and Q31, thereby clamping the keying supply voltage (terminal 3) to ground. In actual operation, the terminal-3 supply has a series resistance that is large enough to limit the peak current into the zener diode (Z5) to approximately 0.8 milliampere. When Q31 conducts, it shunts this current to ground.

The sound-if-channel and PIX-IF-channel signals whose "carrier" frequencies are 41.25 MHz and 45.75 MHz, respectively, are applied to terminal 12. Q32 functions as a buffer between the interstage-tuned-circuits associated with terminal 12 and the PIX/sound-channels amplifier, Q33. The intercarrier frequency (the difference frequency between the PIX and sound "carrier" frequencies) is detected by the peak detector Q34 and C12. The resultant 4.5 MHz FM sound-intercarrier signal is fed to transistor Q35. This transistor and Q36 form a differential pair that provides an amplified intercarrier sound-if signal to the base of Q37. A feedback system through the RC networks in the Darlington emitter-follower output of Q37 provides bandpass shaping in the region of 4.5 MHz while maintaining a low dc gain. The low level of dc gain is desirable because the circuit receives its bias in an open-loop manner from terminal 16. The bandpass of this amplifier system is fairly broad, and even though it is optimized for 4.5 MHz operation, there is relatively high output at other intercarrier frequencies, as shown in the curve in Fig. 4.

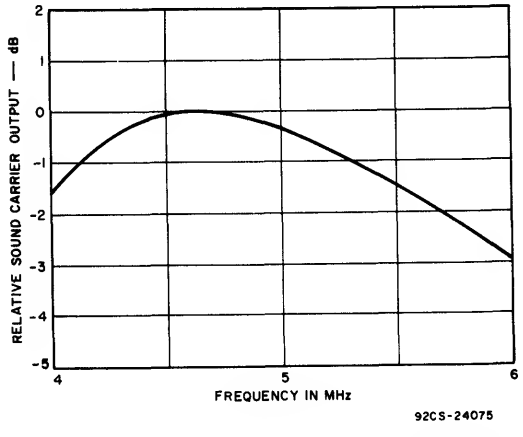


Fig. 4. Relative sound-carrier output as a function of frequency.

The internal zener reference-diode consists of the series diode arrangement shown connected between terminal 18 and the substrate in Fig. 3. A regulator-circuit configuration showing the pass transistor interconnected with the reference diode is given as part of the color and monochrome if amplifier circuits that are discussed in the following paragraphs. Similarly, the regulation curves shown in Figs. 5 (a) and 5 (b) are discussed below in more detail. It should be noted that (with a heat sink for the 2N3053 and a lower value for the resistor in series with the collector) the regulated voltage from this supply may be used to provide power to other circuits in addition to the CA3068.

The distribution of tuned circuits around the CA3068 amplifier circuit is a matter of preference of the circuit designer. In general, a total of five tuned circuits will be required subsequent to the mixer for proper selectivity and bandpass shaping. In addition, at least one 47.25 MHz adjacent sound-channel and one 41.25 MHz sound-channel trap will be required. The systems to be discussed in this Note are designed to be driven from a single tuned circuit connected to the mixer output. In addition, both the color and monochrome if systems described subsequently utilize tuned circuits at the input and output to the cascode amplifier. The second transformer is used to couple

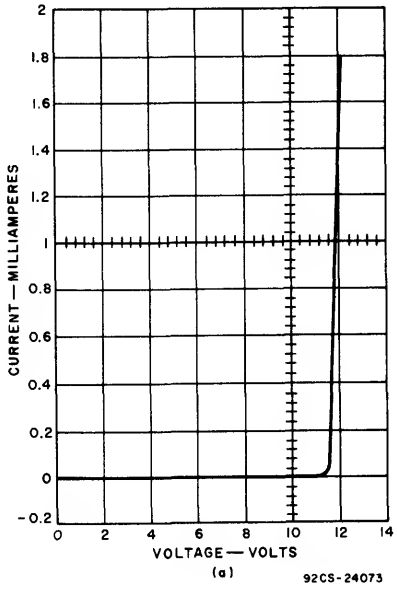


Fig. 5. Regulated supply of the CA3068: (a) voltage-versus-current for zener reference diode of CA3068; (b) voltage-versus-current for regulated supply of CA3068.

output from the cascode if amplifier to the wideband if amplifier (i.e., the output from terminal 9 to input terminal 13 for the PIX-channel and input terminal 12 for the sound-channel). All of the if transformers are synchronously tuned.

PIX–IF SYSTEM DESIGNS

The use of the CA3068 in the two major categories of PIX-IF application, PIX-IF for color-TV receivers and PIX-IF for monochrome receivers, is described below. To illustrate the use of the CA3068 in a tuner requiring "reverse" agc action, the rf-stage of the tuner employed in the PIX-IF for color-TV receiver contains a MOSFET. In contrast, the rf-stage of the tuner employed in the PIX-IF for the monochrome receiver makes use of a bipolar transistor in a "forward" agc arrangement.

COLOR TV

A block diagram of a color-TV receiver is shown in Fig. 1. In the design to be described, the input to the if system is intended to be coupled through a 50-ohm cable from the TV mixer; the mixer employs a single tuned-output coil having an impedance transformed down to 50 ohms. The if input circuit drives a cascode if amplifier with a gain capability of 35 dB. The input impedance to the cascode if amplifier is greater than 4000-ohms at minimum signal levels and increases with agc action. The source impedance as seen by the CA3068 should be approximately 500 ohms to dominate the input-circuit conductance node. Similarly, the output impedance of the cascode amplifier should be loaded by a tuned circuit with an impedance of approximately 3000 ohms to dominate the output node. The if amplifier stability is then unaffected by the IC impedance variations, but is a function of the feedback component. This feedback component consists of coupling within the IC packaging, PC-board stray capacitances, and PC-board common impedances. It can be shown that with the maximum device feedback capacitance the amplifier is stable. For example, with circuit bias conditions of I9 = 2 mA, Y21 = 50 mmhos, and C_{fb} (max) = 0.005pF, the maximum usable gain (MUG) is 42 dB (which allows for a 20 percent skew factor). The fact that this value of MUG is greater than the actual circuit gain (35 dB) substantiates the stability.

Although these calculations show the device to be stable, it must be recognized that poorly controlled external feedback mechanisms may raise the level of feedback in a high-gain, physically small rf amplifier so as to produce instabilities. For this reason, the PC-board layout is extremely important, and any high-gain if amplifier design should include a board layout.

As mentioned previously, the interstage transformer should load the cascode amplifier with approximately 3000 ohms, and should provide a 500-ohm source impedance to input terminal 13 (the wideband if amplifier section). The impedance at terminal 13 is approximately 5000 ohms. The driving-point impedance to sound-if terminal 12 should be about 1000 ohms, this terminal looks into a 5000-ohm input circuit. The 41.25 MHz trap is a rejection filter for the video amplifier and allows the carrier to pass into the sound system.

The circuit design in Fig. 6 shows a typical cable-link circuit which includes a 47.25 MHz bridged "T" adjacent-sound-channel trap at the input circuit. It also includes a 39.75-MHz trap for an adjacent video carrier for operation in CATV systems or in areas where adjacent channels are available. This trap may consist of a 39.75-MHz bridge "T" connected in parallel directly across the 47.25-MHz trap. Both traps provide the additional selectivity necessary for attenuation of the undesired frequencies by more that 40 dB.

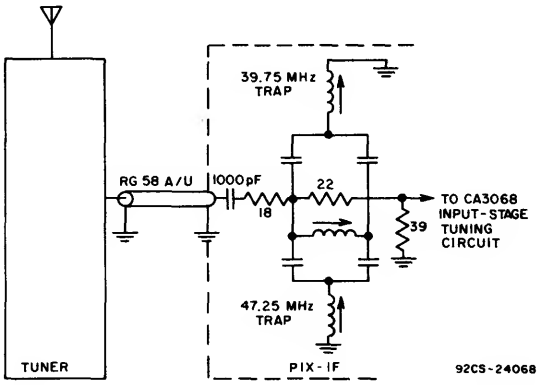


Fig. 6. Schematic diagram of a typical tuner-to-PIX-IF link circuit.

The second and third PIX-IF amplifier stages provide two extra stages of gain (approximately 40 dB). The stages present a very low driving-point impedance to the linear detector, as described earlier. The detected signal then undergoes an additional 12 dB of video amplification. The video output at terminal 19 is nominally 7 volts (peak-to-peak). AGC is developed when the input signal reaches and exceeds the magnitude necessary to produce this video output level. Fig. 7 (a) shows the developed agc bias (terminal-4 voltage) as a function of signal level at terminal 6. Fig. 7 (b) shows the delayed agc voltage at terminal 7 (for application to the tuner) with R1 adjusted so that this delay-bias is generated whenever the input signal at terminal 6 exceeds 8 millivolts.

Fig. 8 shows the RCA CA3068 coupled to a tuner that uses an RCA type 40820 MOSFET in the rf-amplifier stage. AGC voltages are applied (shown in Fig. 8) to optimize over-all TV-receiver performance, so that, when maximum receiver sensitivity is required (such as during the reception of weak signals from the antenna) the tuner will operate at optimum noise factor and maximum gain. As the input signal level increases, it is still desirable to operate the rf stage at optimum signal-to-noise ratio until the signal level is of sufficient magnitude to override any tuner noise degradation brought about by the application of agc. Therefore, the gain-reduction voltage to the tuner should be delayed until the signal level builds up. Fig. 7 (b) shows that this agc is delayed until the if signal level reaches an 8-millivolt level. Then the tuner-gain-reduction mode is initiated. After the tuner gain reduction is expended, at least another 10-dB gain reduction is still available in the cascode portion of the if amplifier.

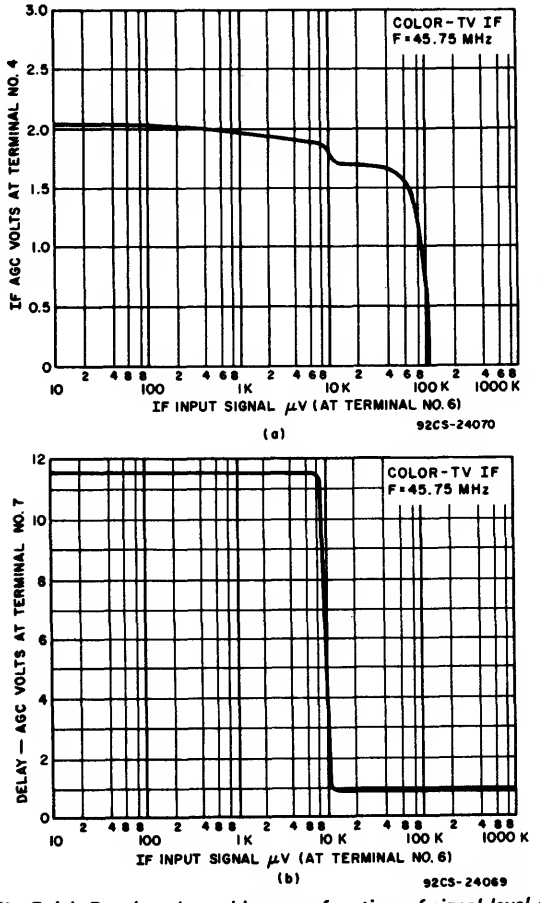


Fig. 7. (a) Developed agc bias as a function of signal level at terminal 7; (b) delayed agc voltage at terminal 7.

An output signal is available at terminal 14 to drive an automatic-fine-tuning (AFT) subsystem-IC, such as the RCA CA3064. This connection is a buffered output from an emitter follower as described earlier. The level of signal at 45.75 MHz to drive the AFT circuit is nominally 15 millivolts.

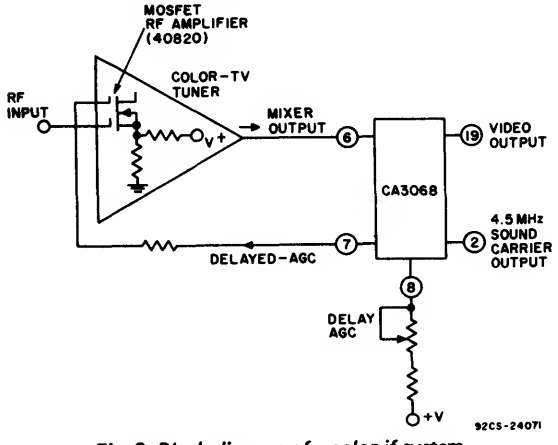


Fig. 8. Block diagram of a color if system.

As shown in Fig. 2, the agc system is, for the most part, self-contained. An optimized agc response characteristic can be achieved by use of a high-quality tantalum 10-microfarad capacitor connected between terminal 4 and ground. An RC decoupling network smooths the agc ripple associated with the charge and discharge of the 10-microfarad capacitor at the horizontal-oscillator frequency rate. The agc system is normally keyed from the horizontal-output circuit in the TV system. This keying pulse should be applied to terminal 3. The magnitude of the pulse should be sufficient to supply a nominal peak current value of 0.8 milliampere into terminal 3. The value of the series resistor R_S associated with terminal 3 may be computed as follows: During the conduction period (with keying applied), the constant-voltage components within the integrated circuit account for:

$V_k = 8.2$ V

(It is assumed that I3 = 0.8 mA)

If the keying-pulse magnitude, V_p, is 15 V, then:

$$I3 = 0.8 \text{ mA} = \frac{15 - V_k}{R_S} = \frac{(15 - 8.2)\text{ V}}{R_S}$$

$R_S = 8.5$ kilohms

The sound output is derived from terminal 2 at a level compatible with the input requirements of a TV-sound-if-subsystem IC, such as the RCA CA3065. There is also a dc component of approximately 6.7 volts present at terminal 2. Coupling networks to subsequent circuits must contain a suitable dc-blocking capacitor.

Small chokes located in the sound and video outputs (terminals 2 and 19) should be self-resonating at the intermediate frequencies to prevent if leakage into subsequent stages.

The CA3068 if subsystem has an internal zener reference-diode that permits operation of the subsystem with an external voltage-regulator pass transistor. A suggested circuit arrangement is shown as part of the over-all if schematic diagram in Fig. 5 (b). The voltage-regulator pass-transistor has a nominal output voltage of 11.2 volts. Bypassing of the V+ supply with reference to the if subsystem is important, and the suggested arrangement shown in the application circuit (Fig. 10) should be used. Specifically, terminal 15 should be bypassed to terminal 17 on the CA3068. Even though terminal 17 is at dc ground potential, it should not be tied to ground but rather should be bypassed in the manner shown to avoid mutual impedance coupling within the CA3068.

MONOCHROME TV

The delayed-agc circuits used in the CA3068 were originally intended to control a MOSFET in the rf-stage of the TV tuner. This arrangement permits direct application of the delayed-agc voltage from the CA3068 to the tuner. In monochrome receivers, however, it is common practice to employ a bipolar transistor in the rf-stage of the tuner, and a circuit with a "forward"-agc characteristic is required to control the rf-stage. This

characteristic is easily established by means of an inverter network utilizing a p-n-p transistor, as shown in the circuit of Fig. 9.

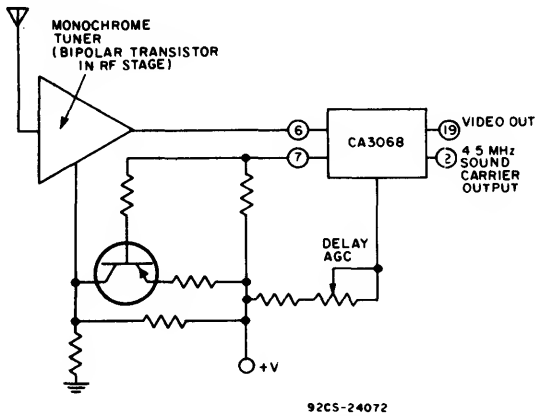


Fig. 9. Block diagram of an if system for a monochrome receiver showing peripheral agc circuit.

As the input signal level increases, the forward-agc delay voltage is developed at the tuner when the voltage at terminal 7 of the CA3068 decreases. The agc voltage applied to the rf-stage of the tuner (Fig. 9) is derived from the collector of the p-n-p transistor. As the delay-agc voltage is generated at terminal 7 of the CA3068, the base of the p-n-p inverter is driven into conduction, which causes more current to flow through the collector circuit, so that a positive (or forward) agc potential is generated for the bipolar transistor in the tuner.

TV RECEIVER PIX--IF CIRCUIT APPLICATIONS

In this section, the application of the CA3068 integrated circuit in a color and a monochrome TV receiver is described. The circuits shown were constructed on single-sided copper PC boards.

As previously noted, because of the high gain encountered in PIX-IF design, positive feedback must be avoided if the amplifier is to remain free of spurious oscillation. To this end, the optimization of printed board layout and component placement is essential. The proper choice of bypassing components and signal-path layout is necessary to avoid feedback through ground loops.

IF CIRCUIT FOR COLOR TV RECEIVER

The schematic diagram of an if system for a color-TV receiver is shown in Fig. 10. A parts list and illustrations showing the PC-board component layout (top view) and the actual printed circuit (bottom view of board) are shown in Appendix A. Since most current color-TV receivers employ automatic-fine-tuning (AFT) systems, an AFT system using the CA3064 has also been included on the same board; Fig. 10 includes the AFT circuit.

The if-response is determined by the triple-tuned circuit, which consists of three traps: two preceding the IC and an interstage double-tuner circuit with one trap. In the tripled-tuned circuit, the two bridge-T traps are used to provide attenuation of the adjacent-channel picture carrier (frequency 39.75 MHz) and adjacent-channel sound carrier frequency (47.25 MHz). A

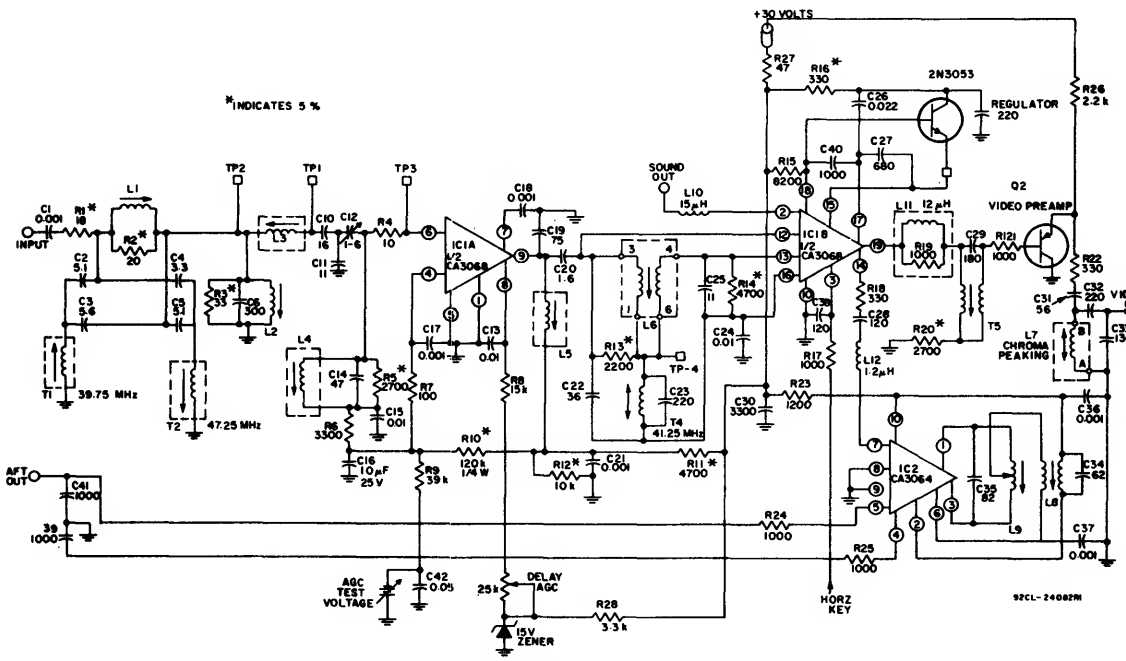


Fig. 10. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a color-TV system. A template of the printed circuit board used to construct this circuit, a diagram of the position of all components on the board, a block diagram of the location of major components on the board, and a circuit parts list are given in Appendix A.

common bridge impedance consisting of parallel-connected L1 and R2 is used. Adjustment of L1 for best null of the 47.25 MHz trap assures the desired 60-dB minimum attenuation.

The triple-tuned circuit provides, at center frequency, a source resistance to the IC of 800 ohms and a voltage gain of three from the input to pin 6 of the IC. The first section of the triple-tuned circuit consists of L2 and C6. Capacitor C6 is in parallel resonance with coil L2 at 44 MHz. The third section of the triple-tuned circuit consists of coil L4 and capacitor C14. Coupling and voltage-gain from L2 to L4 are provided by the second section, coil L3 and capacitors C10, C11, and C12. The inductive reactance of L3 is made 75 times larger than that of L2 to provide a high degree of tuned-circuit isolation for ease of alignment.

The circuit provides protection against interference resulting from a strong rf signal which might inadvertently be introduced between the tuner and the if stage. Parasitic resonance and couplings have been minimized to maintain a high degree of attenuation at frequencies remote from the if-resonance frequency.

The interstage double-tuned bandpass circuit, with a bifilar T-trap at 41.25 MHz, is similar to that commonly used in the third stage of color-TV receivers. The sound and picture carriers are present at the input (terminal 12) to the 4.5 MHz sound-if detector circuit. Trapping action removes the 41.25 MHz sound carrier at terminal 13 to prevent a difference-frequency beat of 0.92 MHz with the chroma subcarrier at 42.17 MHz. The picture carrier and chroma subcarrier entering terminal 13 are amplified, detected, and additionally amplified as detected video signal. If the sound carrier is not attenuated by the 41.25 MHz trap, the carrier will be detected as a large 4.5 MHz difference-signal in the video output. A 4.5 MHz trap (T5) is included to prevent interference of a residual 4.5 MHz intercarrier signal in the chroma and luminance circuits.

The chroma peaking circuit compensates for the slope of the video response, as shown in Figs. 11 (a), 11 (b) and 11 (c). The actual slope and shape of the video response between 3.08 MHz and 4.08 MHz will vary because of normal component tolerance. The chroma-peaking coil, L7, has two cores, one to adjust inductance to center the response at 3.58 MHz, and the other to adjust chroma output level and bandwidth. The latter core controls circuit Q with little effect on over-all inductance.

Photographs of the detected sweep-response characteristics are shown in Fig. 12. The sweep-response of Fig. 12 (f) shows the interstage alignment from TP3 (of Fig. 10) to terminal 9 of the CA3068. The sweep-response curves in Figs. 12 (a) through 12 (e) show 60 dB of agc range from a level of 100 microvolts (Fig. 12 (e)) to 100 millivolts (Fig. 12 (a)).

The alignment procedure for the color-TV PIX-IF system using the CA3068, Fig. 10, is given in Appendix A.

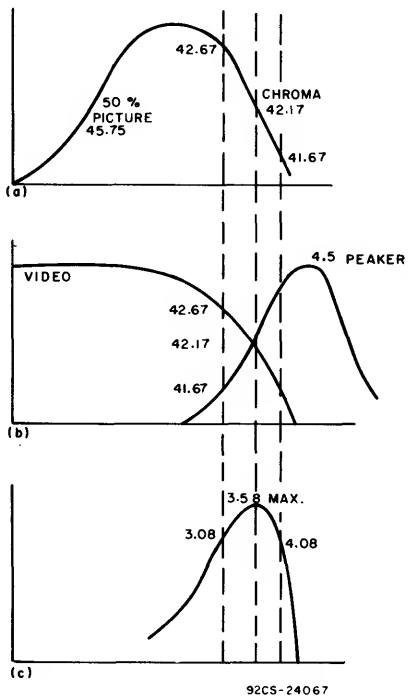


Fig. 11. (a) Over-all if response, (b) video and peaking circuit response, (c) chroma response for the circuit of Fig. 10 (frequency values in MHz).

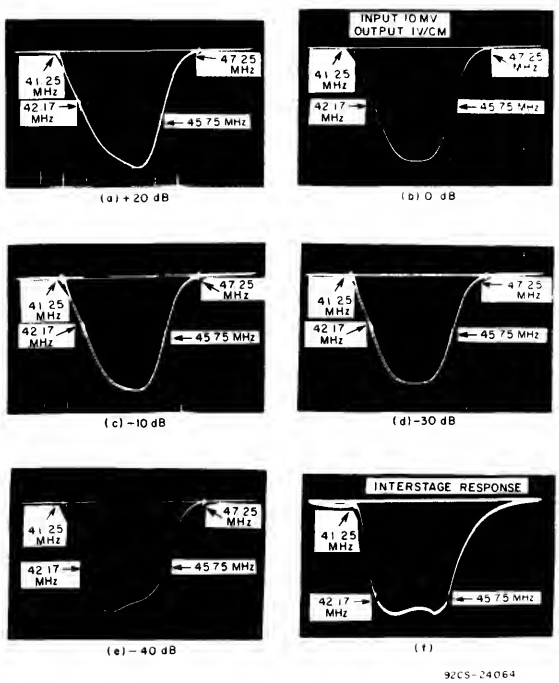


Fig. 12. Detected sweep-response characteristics for the circuit of Fig. 10.

IF CIRCUIT FOR MONOCHROME TV RECEIVER

The schematic diagram for a PIX-IF system for a monochrome TV system that employs the CA3068 is shown in Fig. 13. A PC-board component-layout diagram (top view), the actual printed circuit (bottom view of board), and a circuit parts list are shown in Appendix B. A sound-if system using the CA3065 has been included to show the simplicity with which it can be used in conjunction with the CA3068.

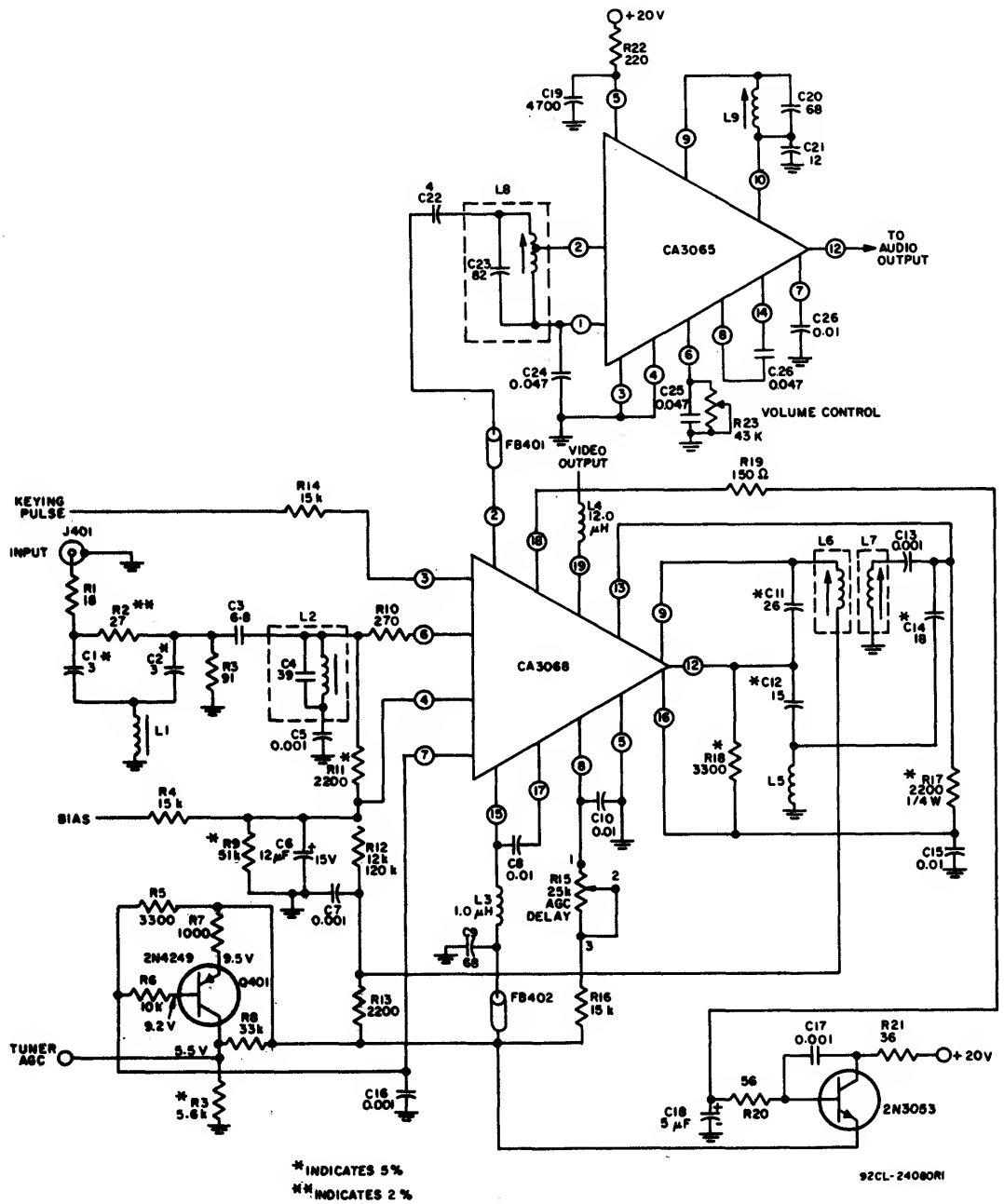


Fig. 13. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a monochrome-TV system. A template of the printed-circuit board used to construct this circuit, a diagram of the position of all components on the board, and a circuit parts list are given in Appendix B.

The selectivity is provided in two sections, an input single-tuned circuit with trap, and a double-tuned interstage circuit. The resistive pad, R1, R2, and R3 of Fig. 13, is used to terminate the link-cable and isolate cable effects from the high-Q input circuit. The bridge-T trap-circuit is used to give maximum attenuation to the adjacent-channel sound carrier. Precision components (R2, C1, C2) achieve a good null at 47.25 MHz without the need for additional components. The circuit Q is controlled by R11 and the resistive input network to yield a 3-dB bandwidth of 3 MHz centered at 44.5 MHz. The "T"-equivalent circuit is used for interstage coupling to realize a miniature, precision, double-tuned transformer. The mutual coupling element, L5, is an air-core, spring-winding coil which is actually calibrated by physical dimensions. If necessary, this coil may be "knifed" to provide a simple and effective coupling adjustment. The circuit Q's are each set at 21, and are controlled by R17 and R18, which also feed bias for the broadband amplifier and sound channels, respectively. The picture-carrier at 45.75 MHz is set at 50 percent to yield proper reception of the vestigial sideband. The color subcarrier at 42.17 MHz is placed comparatively low on the response curve, since the resulting beat with the 41.25 MHz is placed at greater than 5 percent but less than 10 percent to produce an adequate sound-if intercarrier signal at 4.5 MHz, and yet maintain low intermodulation. Typical over-all sensitivity of the if circuit is approximately 150 microvolts for full video output.

Interference from the 45-MHz high-level signals and harmonics is prevented by care in passing and filtering. A 12-microhenry choke (L4 of Fig. 13), self-resonant at the fourth harmonic, is used in the video output lead; the sound output contains a ferrite bead. The B+ supply must be bypassed to provide a low-impedance source for the video driver stages and to provide high-frequency filtering. The 1-microhenry choke (L3 of Fig. 13) is made very lossy to prevent resonance with C8. The ferrite bead and C9 provide high-frequency filtering for harmonics of the 45-MHz signal.

Typical sweep-response characteristics are shown in Fig. 14. The alignment instructions for the monochrome, PIX-IF circuit are given in Appendix B.

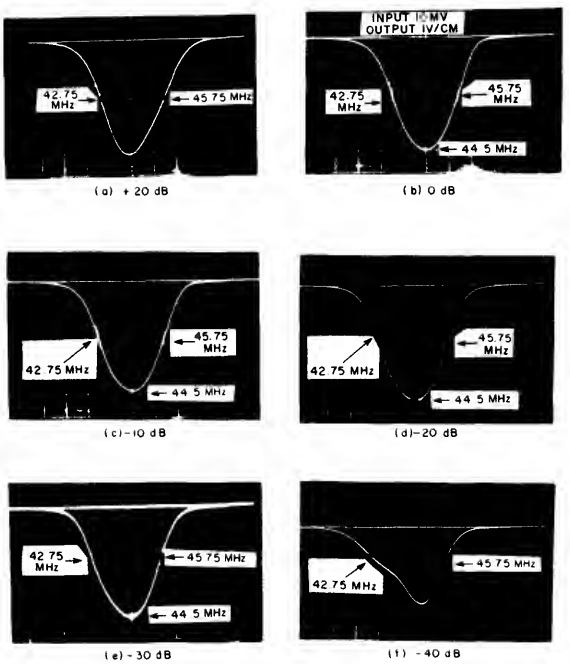


Fig. 14. Typical sweep-response characteristics for the circuit of Fig. 13.

SUMMARY

A complete if subsystem has been described for use in both color and monochrome TV receivers. The only signal inputs required by the CA3068 are if signals from the tuner and a keying pulse from the horizontal circuitry. The CA3068 provides all outputs needed to drive the video output stage, delay line, sync-separator circuitry, RCA CA3065 sound if subsystem, RCA CA3064 AFT subsystem, and delayed-agc voltage for the rf stage in the tuner. Additionally, circuits for noise immunity and signal overload protection are an integral part of the CA3068 design. These subsystems have typical input sensitivities of 100 microvolts for a 4-volt, peak-to-peak video output. A unique video detector arrangement provides extremely linear output throughout the 7-volt, peak-to-peak, video-output range of the system.

Although this Application Note describes subsystem designs in TV receivers, the CA3068 is also applicable in AM communications systems requiring performance at frequencies within the range of 10 to 70 MHz.

REFERENCES

1. RCA Data Bulletin File No. 396 concerning the CA3064 and CA3064E, "TV Automatic Fine Tuning Circuit", or the RCA DATABOOK, 1975 Series SSD-201C.
2. RCA Data Bulletin File No. 412 concerning the CA3065, "TV IF Sound System", or the RCA DATABOOK, 1975 Series SSD-201C.
3. RCA Data Bulletin File No. 467 concerning the CA3068, "Television Video IF System", or the RCA DATABOOK, 1975 Series SSD201C.

APPENDIX A – THE COLOR CIRCUIT

ALIGNMENT PROCEDURE FOR THE COLOR CIRCUIT

Preliminary Adjustments and Calibration

1. Adjust delay-agc (noise pot) fully cw.
2. Connect supplies as indicated on schematic diagram (Fig. 10), set bias to zero.
3. Set sweep generator to 10 millivolts as indicated on Boonton 91DA meter with 56-ohm termination.

Step 1 - IF Interstage Alignment

a. Ground TP1 with short clip lead.
b. Connect sweep generator with 56-ohm termination and 1000-picofarad decoupling capacitor to TP3.
c. Connect oscilloscope to video output.
d. Adjust bias for 5-volt peak-to-peak response on oscilloscope.
e. Adjust bottom core of T4 for minimum at 41.25 MHz.
f. Adjust L5 and L6 for symmetrical response with PIX and color markers equal (Fig. 12 (a)): L5 controls markers and L6 controls tilt.
g. Adjust top and bottom cores of T4 simultaneously, top core for maximum rejection of 41.25 MHz and bottom core to maintain minimum 41.25 MHz.

Step 2 - IF Overall Alignment

a. Leave ground clip lead on TP1.
b. Remove sweep input from TP3.
c. Connect TP2 through a 1000-picofarad capacitor to TP3.
d. Connect sweep generator to input.
e. Readjust variable bias to maintain 5-volts peak-to-peak response on oscilloscope.
f. Adjust T1 for minimum 39.75 MHz.
g. Adjust T2 for minimum 47.25 MHz.
h. Adjust L2 for equal height of PIX and color markers.
i. Remove ground-clip lead from TP1 and 1000-picofarad capacitor from between TP2 and TP3.
j. Maintain 5-volts peak-to-peak response on oscilloscope by re-adjusting bias.
k. Adjust L3 and L4 simultaneously for symmetrical response with PIX and color markers equal: L4 controls markers and L3 controls tilt.
l. Adjust bandpass trimmer, C12, to place PIX and color markers at 40 percent while readjusting L3 and L4 (Fig. 12 (b)).
m. Re-adjust T1 for minimum at 39.75 MHz if necessary.
n. Re-adjust T2 for minimum at 49.25 MHz. Then adjust L2 to maximize the rejection at 47.25 MHz.

AFT Alignment

a. With oscilloscope on AFT output, adjust bias for 10-volts peak-to-peak response.
b. Adjust L8 for maximum 45.75 MHz.
c. Adjust L9 for crossover at 45.75 MHz.
d. Re-adjust L8 and L9 to obtain symmetry.
e. Adjust L8 to obtain maximum width.

Color-Circuit Parts List

Capacitors		Resistors (All values in ohms)	
C1	0.001μF	R1	18
C2	5.1pF	R2	20
C3	5.6pF	R3	33
C4	3.3pF	R4	10
C5	5.1pF	R5	2.7k
C6	300pF	R6	3.3k
C10	16pF	R7	100
C11	11pF	R8	15k
C12	1-6pF	R9	39k
C13	0.01μF	R10	120k
C14	47pF	R11	4.7k
C15	0.01μF	R12	10k
C16	10μF	R13	2.2k
C17	0.001μF	R14	4.7k
C18	0.001μF	R15	8.2k
C19	7.5pF	R16	330
C20	1.6pF	R17	1k
C21	0.001μF	R18	330
C22	3.6pF	R19	1k
C23	220pF	R20	2.7k
C24	0.01μF	R21	1k
C25	11pF	R22	330
C26	0.022μF	R23	1.2k
C27	680pF	R24	1k
C28	120pF	R25	1k
C29	180pF	R26	2.2k
C30	0.022μF	R27	47
C31	56pF	R28	3.3k
C32	220pF	R29	25k
C33	130pF		
C34	62pF		
C35	82pF		
C36	0.001μF		
C40	1000pF		
C41	1000pF		
C42	1000pF		

Inductors	RCA Stock No.
L1	132159
L2	132161
L3	132839
L4	132658
L5	137126
L6	132146
T1	132839
T2	132157
T4	132150
T5	132135

APPENDIX B – THE MONOCHROME CIRCUIT

ALIGNMENT PROCEDURE FOR THE MONOCHROME-CIRCUIT

Step 1 -

1. Connect +20 volts to appropriate points on board.
2. Connect sweep generator to input
3. Connect dc bias voltage to appropriate point on board.
4. Adjust sweep generator for 10-millivolt input.
5. Adjust bias voltage for 5-volt, peak-to-peak output.

Step 2 -

1. Adjust LT for minimum response at 47.25 MHz.
2. Adjust L2 for maximum at 44.5 MHz.
3. Adjust L6, L7 for bandpass shown in Fig. 14 (b). The curve should have 3-MHz bandwidth centered at 44.5 MHz.

Monochrome-Circuit Parts List

Capacitors

C1	3.0pF
C2	3.0pF
C3	6.8pF
C4	3.9pF
C5	0.001μF
C6	12μF
C7	0.001μF
C8	0.001μF
C9	6.8pF
C10	0.01μF
C11	20pF
C12	15pF
C13	0.001μF
C14	18pF
C15	0.01μF
C16	0.001μF
C17	0.001μF
C18	5μF
C19	4700pF
C20	68pF
C21	12pF
C22	4pF
C23	82pF
C24	0.047μF
C25	0.047μF
C26	0.01μF
C27	0.047μF

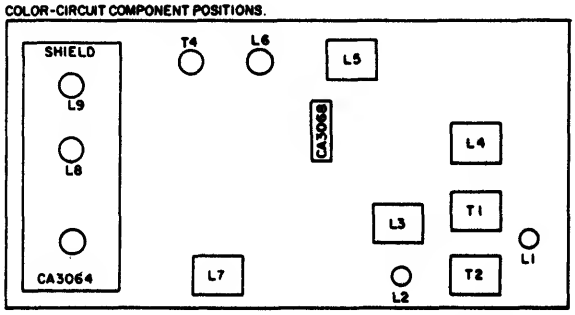
Inductors	RCA Stock No.
L1	131655
L2	133463
L3	1.0μH
L4	12.0μH
L5	134754*
L6	131465
L7	133546
L8	130120
L9	130121

*(9 turns No. 23 wire; use 1/2 W resistor to form coil)

Resistors (All values in ohms)

R1	18
R2	27
R3	91
R4	15k
R5	3.3k
R6	10k
R7	1.0k
R8	33k
R9	51k
R10	270
R11	2.2k
R12	120k
R13	2.2k
R14	15k
R15	25k
R16	8.2k
R17	2.2k
R18	3.3k
R19	150
R20	56
R21	36
R22	220
R23	5.6k

COLOR-CIRCUIT COMPONENT POSITIONS.



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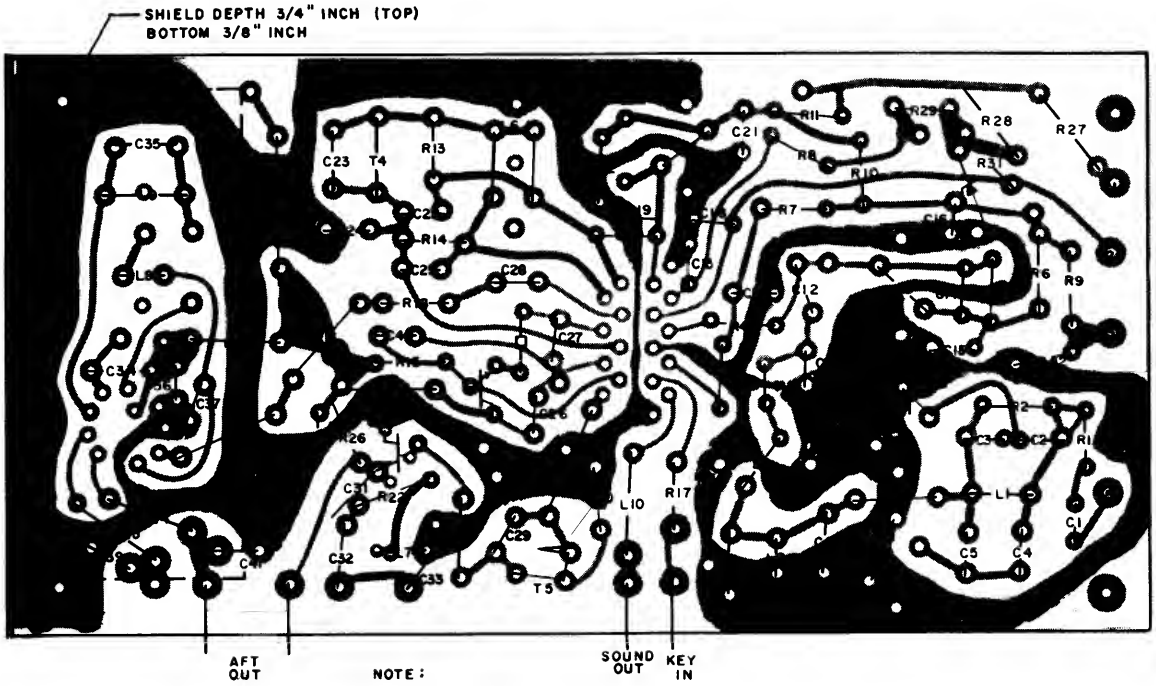
THE COLOR CIRCUIT



NOTE :

(1) + 30 VOLTS
(2) TUNER AGC
(3) CONTROL AGC
(4) GND
(5) INPUT

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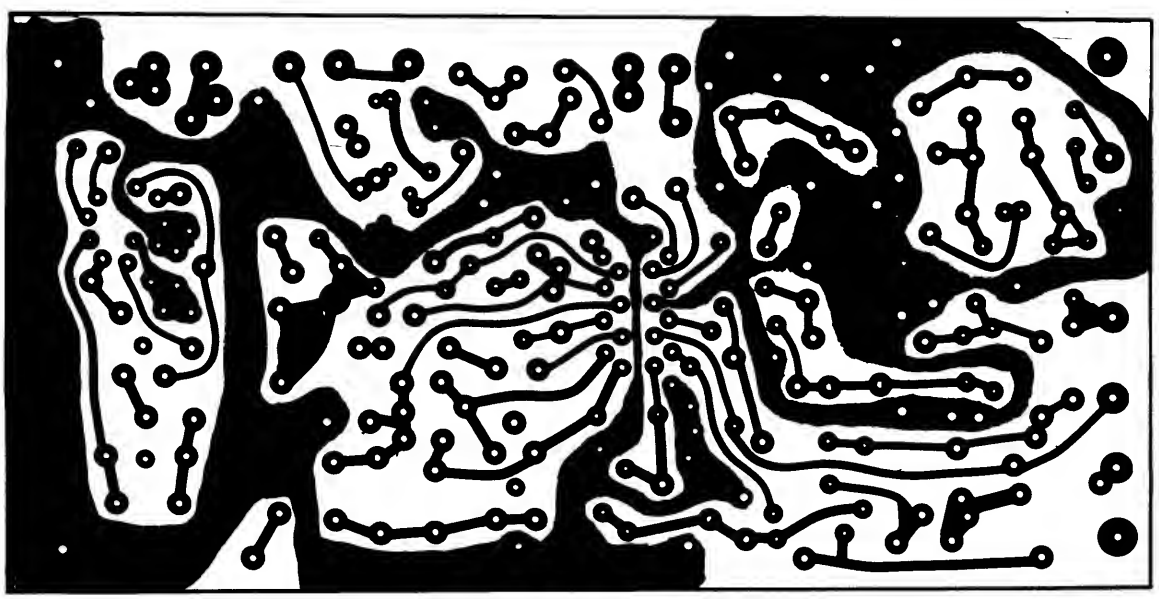
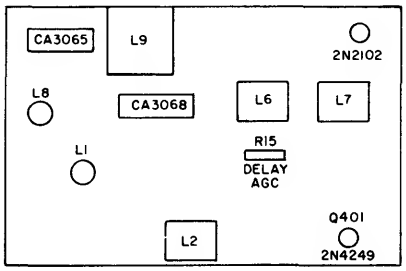


THE MONOCHROME CIRCUIT



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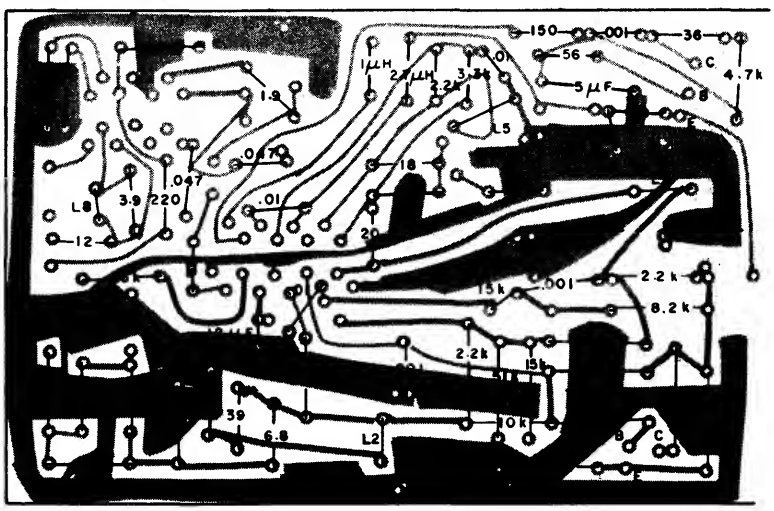
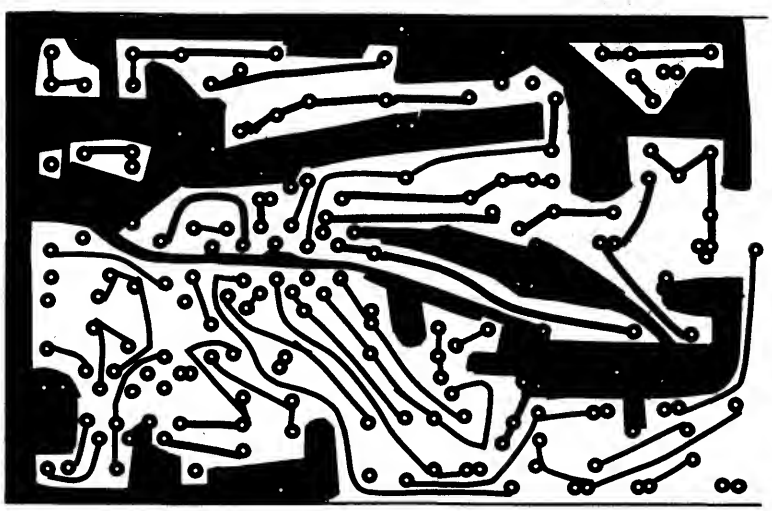




Understanding and Using the CA3130, CA3130A and CA3130B BiMOS Operational Amplifiers

by H. A. Wittlinger

The introduction of the CA3130 BiMOS Op-Amp marked another milestone in the continuing evolution of the ideal monolithic IC Op-Amp. Its characteristics and unique design features are reviewed in order to convey an appreciation of the universality with which it can be employed in circuit applications. Table I contains a tabulation of some electrical performance characteristics for the CA3130B, the premium version in a series of three types:[1] CA3130, CA3130A, and CA3130B. Many of the characteristics provided by the CA3130 series of devices offer performance improvements of almost an order of magnitude over currently popular op-amp types.

CIRCUIT DESCRIPTION

The schematic diagram of the CA3130-series BiMOS Op-Amp, Fig. 1, portrays the simplicity of its three-stage circuit design; each stage is of unique design and provides characteristics of advantage to the user.

Table I — Summary of Characteristics of CA3130B BiMOS Op-Amp

Parameter	Test Conditions (25°C)	CA3130B Min.	CA3130B Typ.	CA3130B Max.
Input offset voltage (mV)	$V^+ = \pm 7.5$ V	—	0.8	2
Input offset current (pA)	$V^+ = \pm 7.5$ V	—	0.5	10
Input current (pA)	$V^+ = \pm 7.5$ V	—	5	20
Large single voltage gain (dB)	$V_o = 10\ V_{pp}$, $R = 2$ k, $V^+ = 15$ V, $V^- = 0$ V	100	110	—
Common-mode rejection ratio (dB)	$V^+ = 15$ V, $V^- = 0$ V	86	100	—
Common-mode input-voltage range (V)	$V^+ = 15$ V	0	−0.5 to 12	10
Power supply rejection ratio (μV/V)	$V^+ = \pm 7.5$ V	—	32	100
Output voltage (V)				
Max.	*$R_L = 2$ k	12	13.3	—
Min.	*$R_L = 2$ k	—	0	0.01
Max. output current (mA)*				
Source	$V_o = 0$	12	22	45
Sink	$V_o = 15$ V	12	20	45
Supply current (mA)*	$V_o = 7.5$ V	—	10	15
($R_L = \infty$)	$V_o = 0$ or $V_o = 15$ V	—	2	3
Input resistance (Teraohms)	†	—	1.5	—
$\Delta V_{IO}/\Delta T$(μV/°C)†	($V^+ = \pm 7.5$V), $R_L = 2$ k, $T_A = -55$ to $+125$°C	—	5	15
Unity-gain crossover frequency†	$C_c = 0$	—	15	—
(f_t = MHz)	$C_c = 47$ pF	—	4	—
Slew rate (V/μs)†	Open loop, $C_c = 0$	—	30	—
	Closed loop, $C_c = 56$ pF	—	10	—

*$V^+ = 15$ V; $V^- = 0$ V. †$V^+ = \pm 7.5$V.

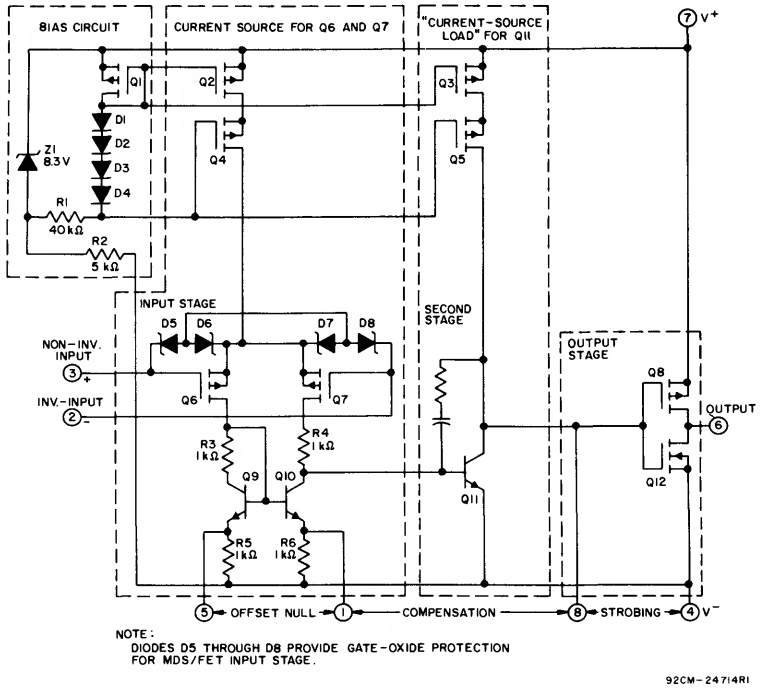


Fig. 1. Schematic diagram of the CA3130-series BiMOS op-amps.

Input Stage

The differential-input stage uses PMOS field-effect transistors (Q6,Q7) that work into a mirror-pair[2] of bipolar transistors (Q9,Q10) functioning as load resistors together with resistors R_3 through R_6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q11). When desired, offset nulling can be effected by connecting a 100 kilohm potentiometer across terminals 1 and 5, and the potentiometer slider arm to terminal 4. Cascode-connected PMOS transistors Q2 and Q4 are the constant-current source for the input stage, and are biased by the bias-circuit shown. Small diodes (D5 through D8) provide gate-oxide protection for Q6 and Q7 against high-voltage transients, including static electricity during handling.

The use of PMOS transistors (Q6,Q7) results in ultra-high input resistance (approximately 1.5 teraohms, i.e., 1.5×10^{12} ohms) and ultra-low input current (5 picoamperes, typical). Additionally, the use of the PMOS transistors permits common-mode range operation down to approximately 0.5 volts below the negative supply-rail potential. While operating in this region there is no "phase reversal" of the output signal.

Second Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. These transistors are biased from the same potentials used to bias PMOS transistors Q2 and Q4, respectively. This circuit design permits Miller-Effect compensation (roll-off) by the use of a single low-value external capacitor. For example, a 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors (PMOS Q8 and NMOS Q12) operating in the linear Class A mode.[3] Consequently, the small-signal "cross-over" distortion of the output signal frequently encountered in op-amps is eliminated. The non-linearity in the output stage of the CA3130 with large signal excursions requires the use of feedback for good waveform reproduction. As a voltage-follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

The use of CMOS transistors in the output stage of the CA3130 permits the output signal to be swung within millivolts of either supply rail when the IC is operating into very-high-resistance loads. In Fig. 1, terminals 4 and 8 are designated for use when it is desired to strobe the output stage into quiescence. Strobing is accomplished by external switching circuitry which pulls terminal 8 down to the potential of terminal 4, thereby shutting off current flow in the output stage and forcing terminal 6 up to approximately the potential of terminal 7 (assuming very high output-load resistance at terminal 6).

The CMOS transistor output stage offers yet another advantage in that the transistors provide short-circuit protection; their channel resistances increase with increasing temperature so that they can protect against excessive current-flow under short-circuit conditions.

Although the CMOS output stage in the CA3130 can typically sink and source current of about 20 milliamperes, greater current-handling capability is easily provided by paralleling auxiliary CMOS transistor-pairs (e.g., CA3600E transistors)[3] at terminals 4, 5, 7 and 8.

APPLICATIONS

Although the unique input and output characteristics of the CMOS op-amp are noteworthy assets in the design of circuits for operation with a single-supply, the fact that both input and output terminals can be swung down to the negative supply rail permits its use in various circuit categories in which dual supplies have customarily been used. For example:

1. Voltage-followers as used to buffer the output of resistor networks used in digital-to-analog converters;
2. Variable-voltage regulator circuits in which the value of the output voltage must be adjusted downward to the proximity of zero;
3. Absolute-value, ideal, full-wave rectifier circuits;
4. Electrometer circuits and the like.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig. 2 illustrates an application in which a number of the CA3130 characteristics are exploited. Fundamentally, it is a single-supply voltage-follower circuit with sufficient gain to drive a 1-milliampere meter in response to picoampere input currents. With the resistor-divider network (R1, R2) shown, it can measure dc voltages over the range of 10 millivolts to 300 volts. The maximum op-amp input voltage developed across R2 is only about 3 volts when the voltage to be measured is 300 volts. This 3-volt potential is applied to the non-inverting input terminal 3 of the op-amp via the R3, C1 network, which minimizes range-switching transients. It should be understood that in this application, the op-amp is effectively measuring potentials ranging downward from 3 volts to zero, with respect to the negative rail (terminal 4). Measurements indicate that with this range of input voltage, the input resistance of the CA3130 is in the order of 3 teraohms. Since the TO-5 case of the op-amp is internally tied to terminal 4, input terminal 3 is effectively protected from spurious leakage currents. Furthermore, since the voltage developed across the glass terminal-to-case insulator is no greater than 3 volts, the leakage currents are very low.

The output voltage is developed between terminal 6 and the negative rail, across the parallel circuit composed of the voltage-ranging network R8, R9, R10, and the meter circuit. The maximum output voltage is about 3 volts, corresponding to the 300-volt potential being measured, with the Meter-Multiplier switch SW2 in the position shown. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to terminal 2 via current-limiting resistor R5. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

Calibration resistors R12 and R14 individually establish full-scale meter deflection when 1 milliampere is forced to flow through resistors R11, R12 and R13, R14, respectively.

Op-amp (and meter) nulling is accomplished by first setting the range-selector switch SW1 to the lowest voltage position and shorting the input terminal to ground. Nulling potentiometer R6 is then adjusted until the first indication of positive meter movement is noted. The circuit is then ready for voltage measurements.

Thermocouple Temperature Control with Zero-Voltage Load Switching

Fig. 3 shows the circuit diagram of a thermo-couple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connected to one leg of the supply line. Consequently, the thermocouple can be "ground-referenced", provided the appropriate leg of the ac line is maintained at ground. The comparator, A_1 (a CA3130), is powered from a 6.4-volt source of potential provided by the zero-voltage-switch (ZVS) circuit (a CA3079).[4] The ZVS, in turn, is powered off-line through a series-dropping resistor R6. Terminal 4 of the ZVS provides trigger-pulses to the gate of the load-switching triac in response to an appropriate control signal at terminal 9.

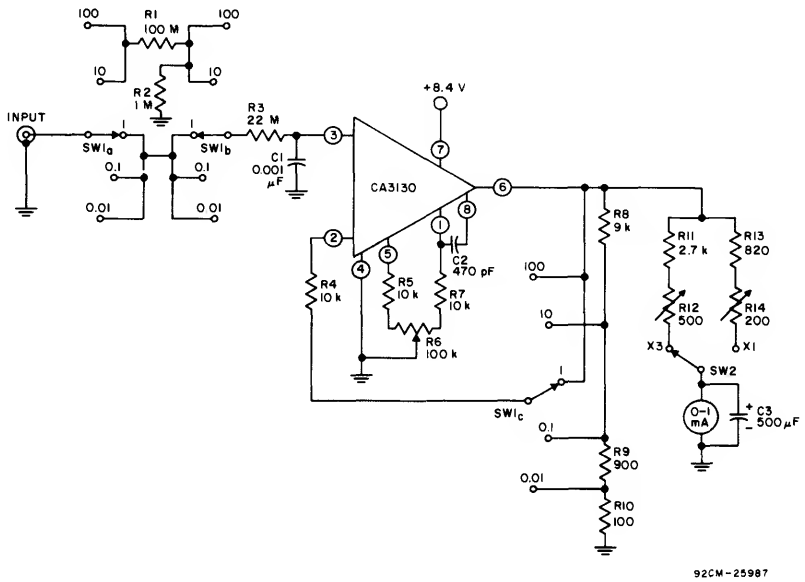


Fig. 2. Schematic diagram of a voltmeter with high input resistance.

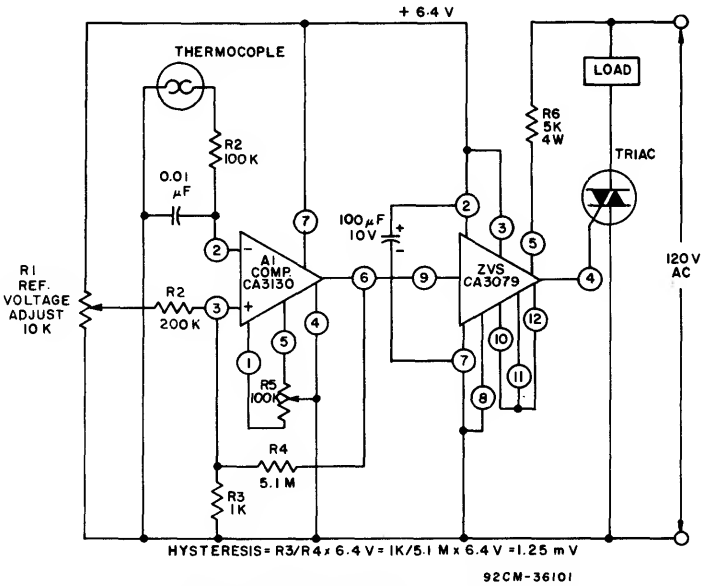


Fig. 3. Thermocouple temperature control with zero-voltage switching.

The CA3130 is an ideal choice for the type of comparator circuit shown in Fig. 3 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R1 drives the voltage-divider network R3, R4 so that reference voltages over the range of 0 to 20 millivolts can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Fig. 3, the circuit is provided with a control-point "hysteresis" of 1.25 millivolts.

Nulling of the comparator is performed by means of the following procedure: Set R1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the non-conductive mode under the conditions above, adjust R5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R1 can be set to the voltage threshold desired for control-circuit operation.

Photodiode Current-to-Voltage Converter

The circuit in Fig. 4 illustrates the use of the CA3130 in an application where sensitivity is required to input currents in the sub-picoampere region. The circuit provides a ground-referenced output voltage which is proportional to the current flowing through a photodiode in the input circuit. Resistor R1 is used to limit the input current to a safe value in the event that the back-biased photo-diode should avalanche and expose the input terminal of the CA3130 to the comparatively high voltage sometimes used in the photodiode supply. Capacitor C1 is connected across the feedback resistor R_f to provide high-frequency roll-off and enhance amplifier stability.

The CA3130 is nulled by means of the following procedure: Place a shorting jumper-connection across resistor R_f. If there is an indication of positive output potential under this condition, adjust R2 until the output is zero. If, on the other hand, the output potential was initially found to be zero with R_f shorted, vary R2 until the first indication of positive output potential is noted, then adjust R2 for zero output. Remove the jumper connected across R_f, and the circuit is ready for operation.

Fig. 4 shows that the output voltage E_{out} is equal to IR_f, where I is the photodiode current and R_f is the value of the feedback resistor. Thus, for example, the output voltage is 1 volt when the photodiode current is 10 nanoamperes and the value of R_f is 100 megohms. The leakage current through capacitor C_1 must be negligible.

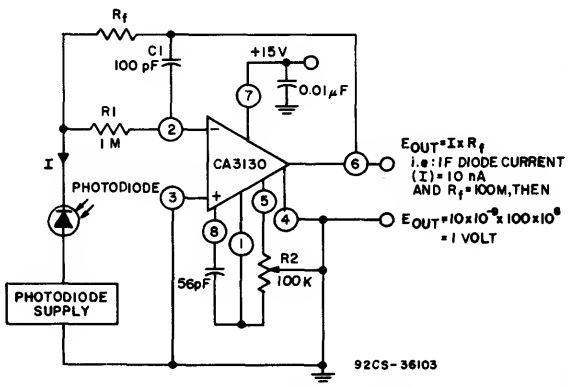


Fig. 4. Photodiode current-to-voltage converter.

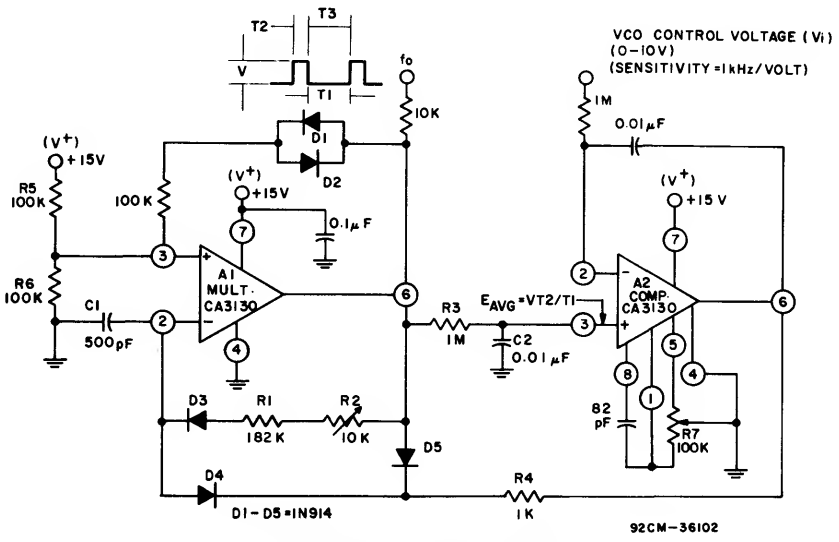


Fig. 5. Voltage-controlled oscillator.

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig. 5. The oscillator operates with a tracking error in the order of 0.05 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V_i$, the VCO control voltage. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator characteristics.

Diodes D_4 and D_5 assure that the control signal supplied via R_4 is inoperative during the pulse-period T_2. Consequently, T_2 is primarily a function of R_1, R_2, and C_1. Diode D_3 effectively isolates R_1 and R_2 during time period T_3. Diodes D_1 and D_2 are used to compensate for changes in V_{AK} of D_3 during temperature excursions, thereby stabilizing the pulse-width T_2. Resistors R_5 and R_6 are a voltage-divider network used to establish the non-inverting terminal (terminal 3) of A_1 at a potential of $V^+/2$.

As noted above:

$$E_{avg} = V\ T_2/T_1$$

since $T_1 = 1/f_o$

$$E_{avg} = V\ T_2\ f_o$$

or

$$T_2 = E_{avg}/V\ f_o$$

Since, under conditions of circuit equilibrium, as described above, $E_{avg} = V_i$, $T_2 = V_i/V\ f_o$ (under conditions of equilibrium). Now if V_i = 10 volts, f = 10 kHz and V = 15 volts, $T_2 = 10/15 \times 10^4$ Hz = 66.6666 microseconds.

The VCO is calibrated by setting V^+ = 15 volts, V_1 = 10 volts, and adjusting R_2 until T_2 = 66.6666 microseconds; i.e., f_o = 10 kHz. The VCO control voltage (V_1) is then reduced to 10 millivolts, and the offset nulling potentiometer R_7 is adjusted until the output frequency (f_o) is 10 Hz. This calibration cycle should be repeated since secondary adjustments will probably be required to assure that the VCO operates with optimized linearity up to 10 kHz.

REFERENCES

1. For complete data and applications information the CA3130-Series circuits see RCA Data File No. 817, "BiMOS Operational Amplifiers", RCA Solid State Division, Somerville, N.J.
2. For a description of the theory and practice of "current-mirrors" see RCA Application Note ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifier," H.A. Wittlinger, RCA Solid State Division, Somerville, N.J.
3. For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see RCA Data File No. 619 on the CA3600E, "CMOS Transistor Array," RCA Solid State Division, Somerville, N.J.
4. For technical information on the CA3079 zero-voltage switch, see RCA Data File No. 490, "Zero-Voltage Switches." Comprehensive applications information is contained in RCA Application Note ICAN-6182. "Features and Applications of RCA IC Zero-Voltage Switches (CA3058, CA3059, and CA3079)," by A.C. N. Sheng, G.J. Granieri, and J. Yellin, RCA Solid State Division, Somerville, N.J.

ICAN-6459

Why Use the CMOS Operational Amplifier — And How to Use It

by H. A. Wittlinger

What Is The CMOS Op Amp?

The circuit diagram of the CA3130-Series CMOS Op Amp[1] is shown in Fig. 1. This circuit marks another milestone in the continuing evolution of the ideal monolithic op amp. The use of PMOS transistors in the input stage and CMOS transistors in the output stage results in unique characteristics and features which can be advantageously exploited in the majority of op-amp applications.

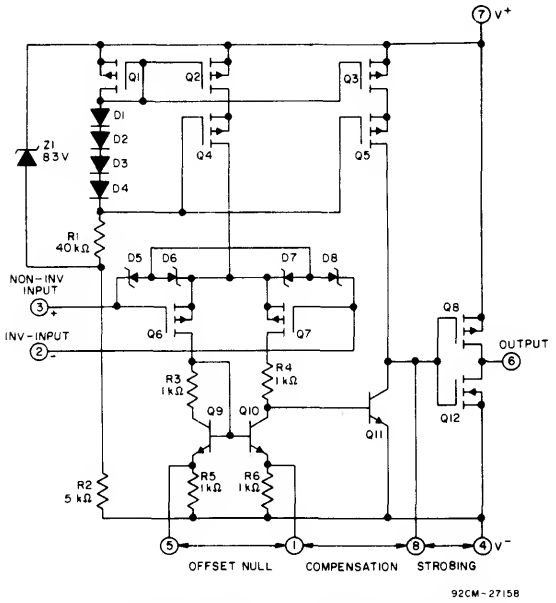


Fig. 1 - Schematic diagram of the CA3130 series CMOS op amps.

The use of PMOS transistors (Q6, Q7) in the input stage provides very high input resistance; Z_I is typically 1.5 teraohms (1.5×10^{12} ohms); the input currents under 15-volt operation are 5 picoamperes (typically) and 2 picoamperes (typically) under 5-volt operation. The common-mode input-voltage range includes the negative supply rail. When the input terminals are swung with small signals in the proximity of the negative supply rail, the input currents are in the range of several hundred femtoamperes; furthermore, the input terminals can even be swung 0.5-volt below the negative supply rail without losing phase sense in the output signal or causing other malfunctions. The upper limit of the common-mode input-voltage range is 12 volts (typically) under 15-volt operation.

The use of CMOS transistors (complementary PMOS and NMOS, Q8 and Q12) in the output stage permits the output terminal to be swung within 10-millivolts of either supply rail when operating into high impedance loads. This characteristic, in concert with the ground-referenced capability of the input circuit, is of importance in implementing many single-supply applications of the op amp; in fact, this combination of characteristics permits the design of many single-supply op-amp circuits previously executed by means of dual supplies. In addition to these unique characteristics, the CMOS op amp offers a number of other electrical characteristics and features which are superior to those offered by similarly priced units. Following are some typical examples:

- Open-Loop Gain 110 dB
- Unity-Gain Compensation:
  Crossover Freq. 4 MHz
  Slew Rate 10 V/μs
- Output Currents:
  Source 22 mA
  Sink 20 mA
- Class A Output-Stage Amplifier (no crossover distortion)
- Strobing terminal permits output-stage amplifier to be strobed off
- Operates with single 5-volt supply (or ±2.5-volt dual supply).

The Benefits of Low Input Current (i.e., High Input Resistance)

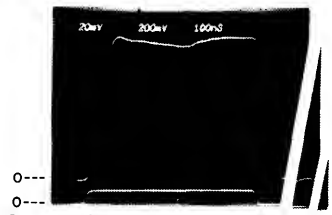
The operation of all op amps requires a small (but finite) current flow at the input terminals. In op amps using bipolar transistors in the input stage this current is known as the input bias current; in op amps using FET's in the input stage this current is known simply as input current because the FET is a voltage-operated device rather than a current-operated device. (The input current in FET's consists of leakage currents.) input currents to an op amp produce an input voltage error which is proportional to the source impedances in which they flow. Obviously, op amps with the lowest input-current requirements offer benefits in reducing input voltage errors — particularly when the signal-source resistance is high. The CA3130, with its PMOS-transistor input stage, typically requires an input current of only 5 picoamperes (or less) while the popular "741" op amp (which uses bipolar transistors) typically requires an input bias current of 80 nanoamperes — a difference ratio of 16,000X.

The input resistance of an op amp also places a load on the signal source. The high input resistance of the CA3130 (1.5×10^{12} ohms, typical) permits it to be operated in conjunction with signal sources having very high resistances.

Sample-and-Hold Circuit

The sample-and-hold (or track-and-hold) function is widely used in linear systems to temporarily store analog information, e.g., in DVM systems, industrial process-control systems, multiplex systems,[2] and A-D converters. The circuit diagram of a sample-and-hold circuit is shown in Fig. 2 where C1 is the sample-holding capacitor. The major design precaution in the use of this method to "hold" charge is that neither the sample-control amplifier nor the sample-readout amplifier should significantly alter the charge stored on C1. The CA3080A Operational Transconductance Amplifier (OTA) is a particularly suitable capacitor charging amplifier because its output resistance is more than 1000 megohms under the "hold" condition, thereby minimizing the loading on the storage capacitor C1. Furthermore, the strobing terminal 5 on the OTA sample-control amplifier simplifies the control of the sample-and-hold process. An effective solution to the read-out requirement involves using the CA3130 CMOS op amp. Since its input-current loading is typically about 3 picoamperes in this application, its loading on the charge-holding capacitor C1 is usually negligible. Both of the amplifiers are operating as voltage-followers (noninverting mode). Nulling of the entire system is accomplished by shorting the input terminals and then adjusting the nulling potentiometer R6 until the output voltage is zero; when the input terminals are unshorted, the circuit is ready for operation. The C1, R3 network phase compensates the OTA; C5 is the compensation capacitor for the CA3130.

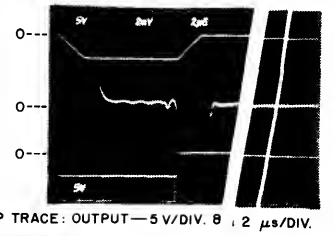
Fig. 3 shows an oscilloscope photo of the sample-and-hold output-signal response to a small-signal step-pulse input. Fig. 4 shows a multitrace oscilloscope photograph of large input and output signals for the circuit of Fig. 2 operating in the linear sample-mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The center trace in Fig. 4 shows the difference between the input and output signals as generated by a Tektronix 7A13 differential amplifier system; system settling time is about 3 microseconds.



TOP TRACE: OUTPUT — 20 mV/DIV. & 1 ,00) ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 1 ,00 ns/DIV.

92CS-27160

Fig. 3 - Oscilloscope photo showing o ut put-signal response of circuit of Fig. 2 to a sr nall-signal step-pulse input.



TOP TRACE: OUTPUT—5 V/DIV. & 2 µs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT — 2 mV/DIV. & 2 µs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 µs/DIV.

92CS-27161

Fig. 4 - Oscilloscope photo s ho wing circuit of Fig. 2 operating in the linear sample mode.

Wideband Amplifier

Wideband amplifiers, (video-signal processors, oscilloscope preamplifiers, instrumentation, pulse-signal amplifiers, and the like) capable of functioning from dc into the high-frequency region, are of almost universal interest to designers. The diagram of a wideband amplifier, with a bandwidth from dc to about 35 MHz and a gain of 10X, is shown in Fig. 5. This amplifier has ground-level input and

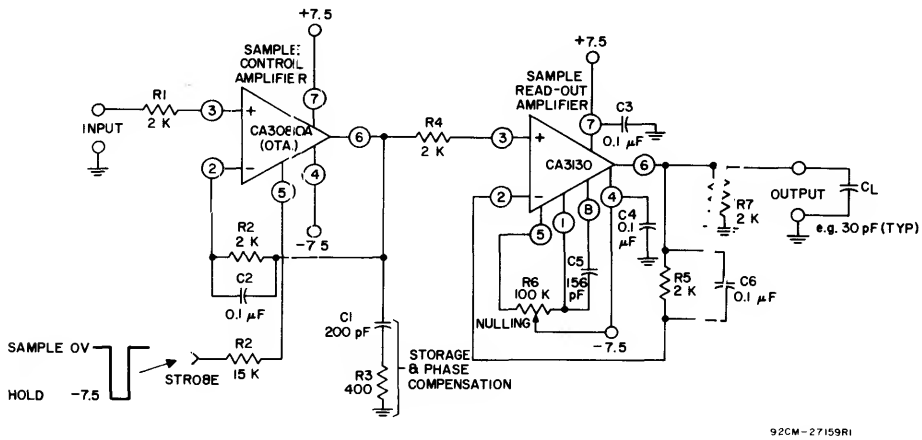


Fig. 2 - Sample-and-hold circuit.

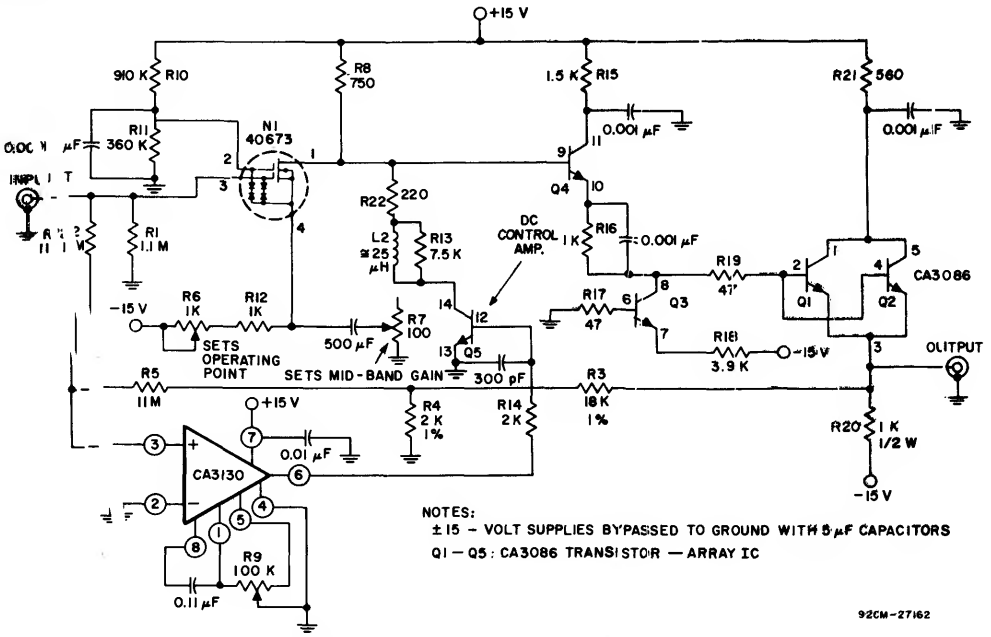


Fig. 5 - Wideband amplifier (10X) (bandwidth approximately 35 MHz).

output terminals. The design is split into two sections; high-frequency gain is provided by N1, a 40673 dual-gate MOS/FET[3] while low-frequency gain (with dc stabilization) is provided by the CA3130 CMOS op amp. Transistors Q1 and Q5 are part of a CA3086 transistor-array IC[4]. The gain of 10X is established by the values of R3 and R4 in the feedback path.

The input resistance of the amplifier is 1 megohm. Consequently, the shunt-loading across R1 resulting from the R2, R5 combination must be minimized. Furthermore, the low input currents required by the CA3130 permit the use of 11-megohm resistors for R2 and R5. The CA3130 operates as a single-supply amplifier that drives the dc control amplifier transistor Q5, which shares load resistor R7 with MOS/FET N1. Transistors Q3 and Q4 are used in a level-shifting stage that drives the parallel-connected pair Q1, Q2 as an emitter-follower. Variable resistor R6 is used to set the operating point of MOS/FET N1 for a nominal drain current of 10 milliamperes. The entire amplifier is nulled by shorting the input terminal to ground and adjusting R9 for zero dc output voltage. The mid-band gain is set by driving the amplifier with a pulse of about 5 nanoseconds rise time (or less) and adjusting resistor R7 for optimum response. This amplifier normally drives a 1-kilohm load and can accommodate input signals up to 100 millivolts (peak-to-peak) without overloading.

Interfacing with Digital Circuits

The output-stage CMOS transistors (Q8 and Q12) shown in Fig. 1 are connected in the classical CMOS inverter configuration. Consequently, the op amp is ideal for use as a direct interface with CMOS digital circuits operating over the supply range of 5 to 15 volts.

Fig. 6 shows the CMOS op amp connected as a direct interface with two gate circuits of either the low power,

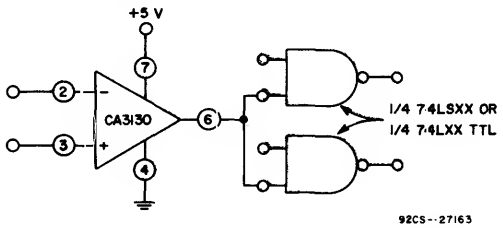


Fig. 6 - CA3130 driving low power Schottky TTL.

Schottky-clamped TTL (74LSXX) type or the low power TTL (74LXX) type; both op amp and digital circuits are operated from a single 5-volt supply. This circuit can also be used with 54LSXX or 54LXX circuits provided the supply voltage on the CA3130 is not permitted to drop below 4.75 volts.

The current-sourcing and current-sinking capabilities of the CMOS output stage in the CA3130 are easily augmented by parallel-connecting additional CMOS digital-inverter IC's across Q8 and Q12 (Fig. 1). Such an arrangement is shown in Fig. 7 where three parallel-connected inverters in the CD4007A are connected across the op-amp output stage; the circuit can interface with the inverters (e.g., CD4049A) as an alternative for the CD4007A. Circuits of the generic type shown in Fig. 7 are used for interfacing with standard 74LXX or 74SXX T^2L; interfacing with 54XX, 54SXX, and DTL is also practical if the supply voltage of the CA3130 is not permitted to drop below 4.75 volts.

Equalized Preamplifier

Operational amplifiers are becoming increasingly popular as equalized preamplifiers for the small signals produced by a magnetic-type phonograph cartridge or tape playback head; op amps can provide a high degree of rejection against noise and hum on the power-supply voltage bias;

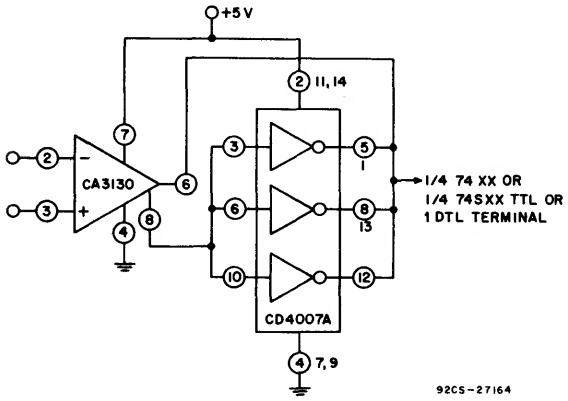


Fig. 7 - CA3130 driving CMOS interface to TTL or DTL.

their differential input circuitry permits easy application of a feedback network to "equalize" (roll-off) the preamplifier in accordance with playback frequency-response requirements of the RIAA or NAB specifications. The CA3130 is useful as an equalized preamplifier because it is capable of operating with an unusually high dynamic range of output voltage ("head-room") for a particular supply voltage; its unique input circuit characteristics also permit the design of a circuit with fast turn-on characteristics in single-supply operation.

Fig. 8 shows a circuit[5] using the CA3130 as the preamp for signals from a magnetic phonograph cartridge; the amplifier

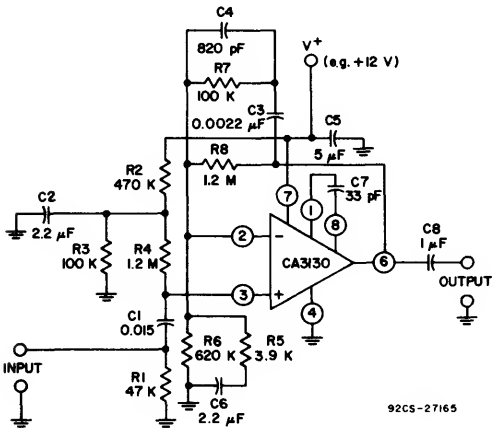


Fig. 8 - Equalized preamplifier for signals from magnetic phonograph cartridge.

is "equalized" in accordance with the RIAA frequency-response specifications for playback. Resistor R1 terminates the magnetic cartridge. The divider-network R2, R3 develops about 2 volts with respect to ground, supplied via R4 as bias voltage to the noninverting terminal 3. Optimum performance is achieved when terminal 6 is maintained at a dc potential of about $V_{CC}/2$, a condition established when terminals 2 and 3 are held at similar potentials. Thus, if V_{CC}=12 V, then $V_{CC}/2$=6 V, and the divider-network R8, R6 establishes a dc bias voltage of about 2 volts with respect to ground at the inverting terminal 2. This design feature permits the amplifier to be turned on quickly because the capacitors connected to its input terminals need only be charged to 2 volts above ground for proper operation. The following expression relates the resistor values required to produce the proper bias voltage for setting the output voltage at terminal 6 to a value of $V_{CC}/2$:

$$\frac{R3}{R2+R3} = \frac{1}{2}\left(\frac{R6}{R6+R8}\right)$$

At low audio frequencies, the reactances of C3 and C4 are comparatively high; therefore, the low frequency gain of the amplifier is established by the ratio of resistances R8 and R5. At mid-band frequencies (e.g., 1-kHz), the reactance of C3 has decreased significantly so that R7 increasingly shunts R8. In this mid-band range, the gain is set at about 30 dB by the ratio of resistances R7 (shunted by R8) and R5. At increasingly higher frequencies, the reactance of C4 decreases and, accordingly, shunts R7; therefore, at the highest frequencies the gain is determined by the ratio of the reactance of C4 and the resistance of R5. Phase compensation for the op amp is provided by C7.

The circuit in Fig. 8 is also generically suitable for use as a preamplifier following a magnetic tapehead. It can be equalized for NAB tape standards by making C4=180 picofarads and R7=56 kilohms.

References

1. For complete data and applications information on the CA3130 Series Op Amps, see RCA Data File No. 817, "BiMOS Operational Amplifiers," RCA Solid State Division, Somerville, N.J.
2. For technical information on the CA3080, see RCA Data File No. 475, "Operational Transconductance Amplifiers (OTA's)." Comprehensive applications information is contained in RCA Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers," by H.A. Wittlinger, RCA Solid State Division, Somerville, N.J.
3. For complete technical information on the 40673, see Data File No. 381, "Silicon Dual Insulated-Gate Field-Effect Transistor," RCA Solid State Division, Somerville, N.J.
4. For complete technical information on the CA3086, see RCA Data File No. 483, "General-Purpose N-P-N Transistor Array," RCA Solid State Division, Somerville, N.J.
5. Circuit designed by L.A. Kaplan, RCA Solid State Division, Somerville, N.J.

ICAN-6472

A Chrominance Demodulator IC with Dynamic Flesh Correction

by L. A. Harwood

A chrominance demodulator integrated circuit, RCA type CA3137, is described which includes a novel dynamic flesh-correction circuit for modulating the reference carrier in the vicinity of flesh colors as a function of the phase information contained in the chrominance signal. The circuit corrects purple and green flesh tones without affecting the primary red, blue, and green colors.

Other functions provided by the new IC are the saturation and hue controls and three low-impedance output stages for the color difference signals. Internal filters reduce the harmonics of the subcarrier to a very low level. Relatively few external components are required to complete the circuit and no tuning adjustments are necessary.

The chrominance demodulator together with the chrominance procesor, RCA type CA3126, provide a complete chrominance system for color TV receivers.

Description of the Chrominance System

The complete chrominance system consisting of the chrominance processor and the developed demodulator is shown in Fig. 1. Fig. 2 is a block diagram of the major functions in the new chrominance demodulator. At first, the flesh-control circuit is assumed disabled to simplify the description.

The chrominance signal, derived from the processor circuit proceeds through a gain-controlled amplifier and through an attenuator to a pair of demodulators. The chrominance amplifier gain control adjusts the level of saturation. The attenuator following the amplifier reduces the chrominance signal to a level which is within the linear range of the demodulators. "I" and "Q" demodulators were chosen to simplify the flesh-correction circuit as explained later.

The regenerated subcarrier also derived from the processor circuit is applied to a hue-control circuit where the hue is manually adjusted by the viewer. The phase-adjusted carrier proceeds through an amplitude limiter and upon filtering through a buffer stage to the "I" demodulator, a 90-degree phase-shifter following the buffer stage provides the proper reference signal for the "Q" demodulator. The demodulated "I" and "Q" signals are filtered to remove the harmonics of the subcarrier and upon amplification are matrixed to produce the R-Y, B-Y, and G-Y color difference signals. DC translators normalize the DC levels of the three outputs. Each of the output stages is designed to provide a low output impedance.

The flesh-control circuit is enabled by means of a switch as shown in Fig. 2. The function of this circuit is to reduce the need for frequent adjustment of the hue control. The flesh-correction circuit introduces an intentional distortion in the chrominance signal in the vicinity of flesh colors (+ "I" signals). This circuit uses the phase detector, shown in Fig. 2, to compare the chrominance and subcarrier signals. In the presence of chrominance signals in the vicinity of flesh colors (+"I"axis), it controls the π/demodulator to pass the amplitude-limited chrominance signal. The latter signal combines with the reference carrier in a filter network to produce a new, phase-modulated, reference carrier so as to reduce the originally existing phase difference between the reference and chrominance signals.

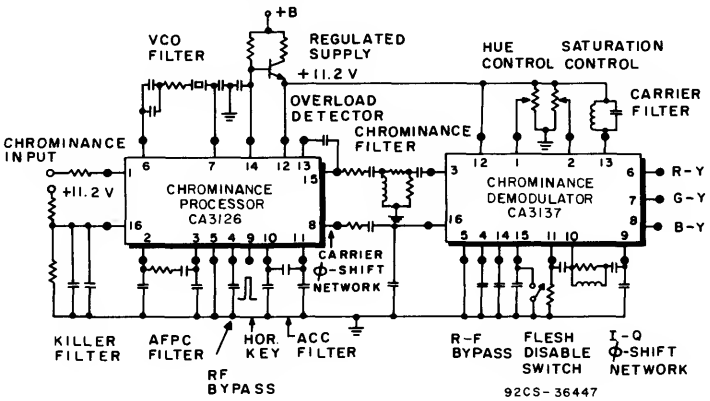


Fig. 1 - Composite chrominance system.

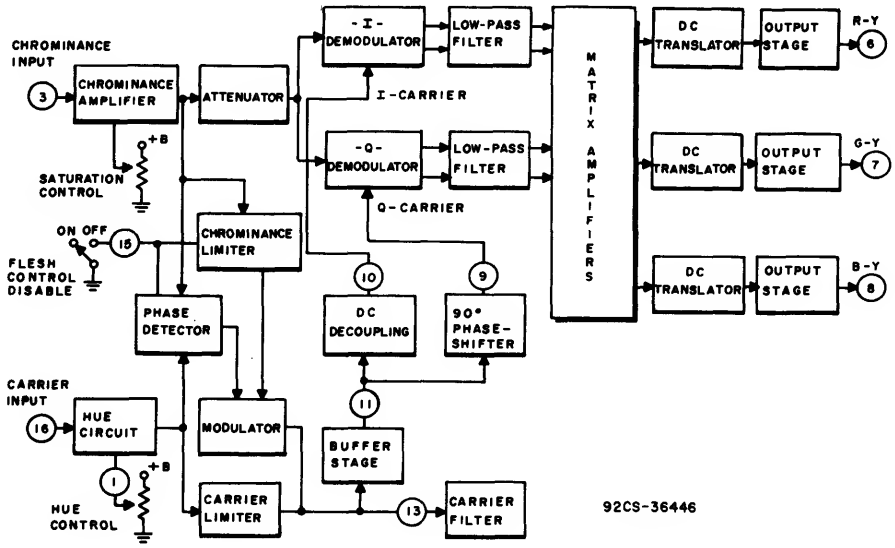


Fig. 2 - Chrominance IC block diagram.

Signal Analysis of the Flesh-Control Circuit

A new approach to the flesh control problem is employed in the demodulator circuit and the principle of operation is described in this section.

As indicated previously, the function of the flesh-control circuit is to reduce the need for frequent adjustment of the hue control by the viewer. Due to inadequate control of the phase relation between the reference carrier and the picture information, hue adjustments are required not only when switching channels but also on different shows on the same channel. Proper setting of the hue control by the viewer, requires a judgment which is based on visual memory of certain colors such as the color of the human flesh, blue sky or green grass.

In the absence of an absolute phase reference, the setting of the hue control is usually performed on scenes with flesh colors and reflects the viewer's preference of those colors. Obviously, this is not a very "scientific" method of assuring faithful reproduction of colors transmitted from the studio. Picture-tube nonlinearity, phosphor tolerances, and other system imperfections compound the adjustment difficulty of the hue control.

A study of the need for color controls on color receivers (2) points out that: simple hue and chrominance controls cannot compensate for all variations from the intended color that may occur in a single picture. However, it is important that a few well-known colors be properly reproduced. This is emphatically true of flesh tones. Controls that compensate for errors in flesh tones will in general be adequate for other colors because the viewer is generally ignorant of the intended colors and tolerates wide differences in their reproduction. But he will not tolerate bad flesh tones that give the impression of skin disease or men from Mars.

This explains the customer's acceptance of flesh-control circuits available in most color receivers.

Although flesh-correction circuits inherently distort the transmitted signal, it is desirable to keep the distortion to a minimum and restrict it to areas where correction is needed. The principle employed in the demodulator is illustrated in Fig. 3. The circle diagram represents the locus of the chrominance signals, and the rotation of the vectors due to flesh correction is indicated by arrow signs. Colors with electrical signals coinciding with the + "I" axis and also the signals having negative "I" components remain unaffected. Also signals in close vicinity of the + "I" axis experience relatively small rotation. Thus, normal flesh colors, solid red, blue, and green colors remain essentially the same. The greatest shift is in colors in the magenta and yellow-green areas and the shift is toward the flesh colors (+ "I" axis). The amplitude of the rotated signals remains constant and the saturation is not affected by this form of flesh control.

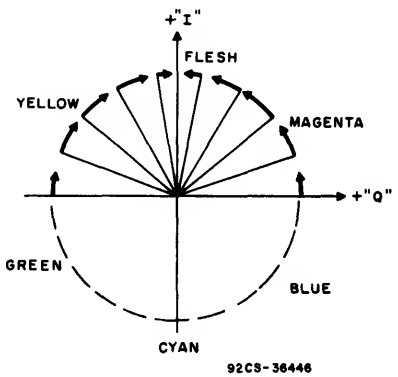


Fig. 3 - Rotation of color vectors due to flesh correction.

The signal processing described above can be accomplished by modulating the reference carrier with the phase-information available in the chrominance signal. For example, addition of an amplitude-limited chrominance signal to the reference carrier produces a phase-modulated carrier as shown in Fig. 4. The reference vector OA and the chrominance vector AB produce a new reference vector OB. The phase angle α, between the uncorrected reference and chrominance signals, is reduced to a smaller angle β satisfying one of the objectives set in Fig. 3. In this process, however, signal AC with a negative "I" component also rotates the reference carrier. To prevent this undesirable effect, the chrominance signal is passed through a modulator stage gated by a signal from the phase-detector. The response of the phase-detector is shown in Fig. 5. This signal controls the conduction of the modulator stage. Maximum conduction occurs when the chrominance phase coincides with the +"I" direction. The conduction diminishes for other signals, and for chrominance signals with negative "I" components the modulator blocks the passage of the chrominance signal. The control range of the modulator stage can be altered by applying a DC offset to this circuit. The offset bias, shown in Fig. 5, reduces the conduction angle of the modulator circuit to less than 180°.

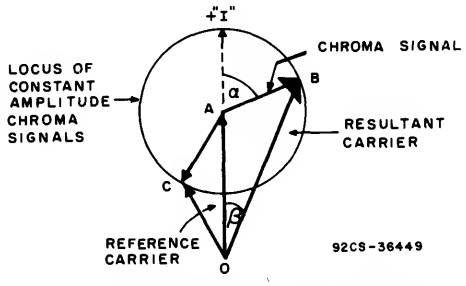


Fig. 4 - Reference carrier phase modulated by the chrominance signal.

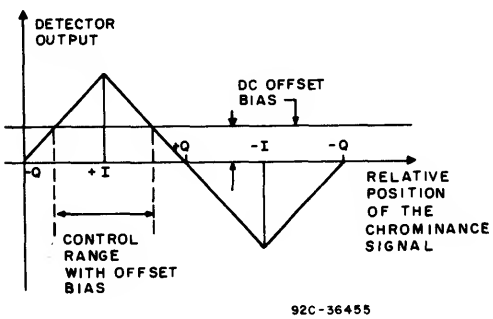


Fig. 5 - Phase detector response.

The action obtained with this control is shown in Fig. 6. It shows the locus of the reference carrier as a function of the phase of the chrominance signal.

An important consideration in the design of a dynamic flesh-control circuit is the system bandwidth. To process the chrominance signal, without introduction of time delays,

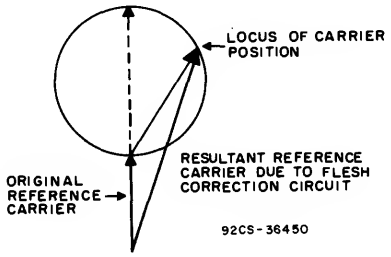


Fig. 6 - Locus of the reference carrier modified by the flesh-correction circuit.

the highest modulation frequency in the chrominance channel must be considered. In the described circuit, there are two sections where filtering is indicated. One of those is the tuned filter at terminal 13, employed to remove harmonics of the phase-modulated reference carrier. This circuit resonates at 3.58 MHz and the bandwidth is set to 2 MHz to pass all the information in the chrominance signal.

The second area where filtering is implied is in the phase detector. Substantial filtering of signal harmonics is required to produce a detector response as shown in Fig. 5. This response was used to simplify the description of the flesh-correction circuit.

Essentially no filtering is employed in the CA3137 phase detector. The waveforms of the signal processed in the flesh-correction circuit are shown in Fig. 7. Signal A

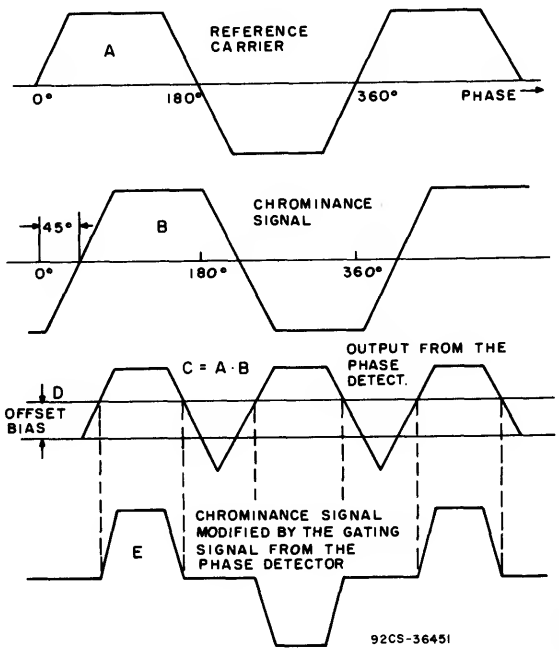


Fig. 7 - Signal waveforms in the flesh-correction circuit.

represents the reference carrier and signal B is the chrominance displaced by 45° from the reference carrier. The trapezoidal waveform of the signal results from amplitude limiting of a sinusoid. Multiplication of signals A and B produces signal C. A dc offset voltage applied to the modulator is indicated by the line D. The modulator is gated only by this fraction of signal C which exceeds the line D. The chrominance signal B in passing through the modulator is modified by the gating signal, and curve E is the resultant waveform. It is phase-shifted toward the reference carrier, thus, the resultant reference carrier is produced by adding to the original carrier a signal already phase-shifted toward this carrier.

The operation of the flesh-correction circuit is not affected by this slightly modified concept; it satisfies the requirements set in Fig. 3.

The rotation of the reference carrier as a function of the chrominance phase, plotted in Fig. 8, determines the operation of the flesh-correction circuit. The control range of this circuit is ±100° with respect to the "I" reference and the maximum correction range is ±20°.

The described signal processing is achieved with relatively simple circuitry. The composite demodulator circuit including the flesh correction is explained in the following section.

MAJOR FUNCTIONS IN THE CA3137 DEMODULATOR IC

Fig. 9 shows the major functions performed in the demodulator; bias and other auxiliary circuits are deleted.

Saturation Control

The gain control in the demodulator is optimized for linearity of its control characteristic and for a minimum of differential phase-distortion; the latter is less than 2° over its operating range.

The chrominance signal, applied to terminal 3, is amplified in the differential stage Q17-Q18 and the output signal is developed across resistors R26, R27, R28, and R29. Transistors Q19 and Q20 connected in common base mode, isolate the output signal from the input terminals of devices Q17 and Q18 thus reducing undesired feedback. This amplifier provides two signal levels. One, developed across resistors R28 and R29, is adjusted for linear operation of the "I" and "Q" demodulators and is applied to the bases of transistors Q26-Q27 and Q33-Q34.

Considerably larger signals are developed across resistors R26 + R28 and R27 + R29 to drive the chrominance limiter Q16-Q11 and the phase detector amplifier Q8-Q9, both stages in the flesh-control circuit.

Diodes D1 and D2 provide a bypass path for the chrominance signal to ground through an external low r-f impedance at terminal 4. The impedance of both diodes is a linear function of the dc current supplied from follower F13 through resistor R30. This current is a linear function of the potential applied to the base of the follower F13 (terminal 2), hence the attenuation of the chrominance signal is a linear function of this applied potential and the control characteristic is linear.

The Hue Control Circuit

The hue control circuit in the CA3137 produces a ± 45° control range which is linear over the major part of the control range. The carrier signal applied to terminal 16 passes through the follower transistor F2 and proceeds through two paths. One path leads through resistor R6 to the base of Q4 and the signal maintains its original phase. In the second path, the signal is phase-shifted +45° by the phase-shift network C1 and R3 + R5. A fraction of the phase-shifted signal, developed across resistor R3, is amplified by the differential amplifier stage Q2-F3 and also appears across the load resistor R6. The phase of this signal is -135° with respect to the reference due to phase inversion in the amplifier stage. The resultant amplitude and phase of both signals developed across R6 depends on the gain of the amplifier which is a function of the control bias applied to terminal 1. Resistor R2 is dimensioned so that with terminal 1 at +B potential transistor Q1 is cut off. At this control position, the relative phase of the output signal is zero degrees (reference phase) since no current passes through the transistor Q2.

With the control bias at approximately ground potential, the gain of amplifier stage Q2-F3 reaches its maximum, which is dimensioned to produce a signal 1.4 times larger than the zero phase signal appearing across resistor R6. The resultant of the two signals, one with a phase of zero degrees and the second with a phase of -135 degrees, is a signal with a phase of -90 degrees.

Since the gain of the amplifier Q2-F3 is a linear function of the potential applied to terminal 1, the phase control is essentially linear over its operating range.

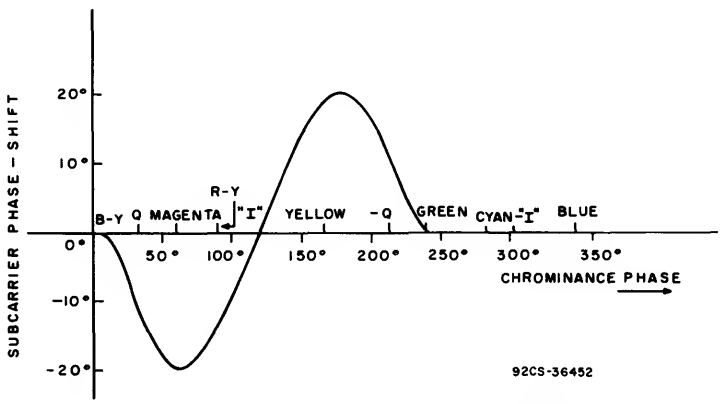


Fig. 8 - Subcarrier phase shift as a function of chrominance phase.

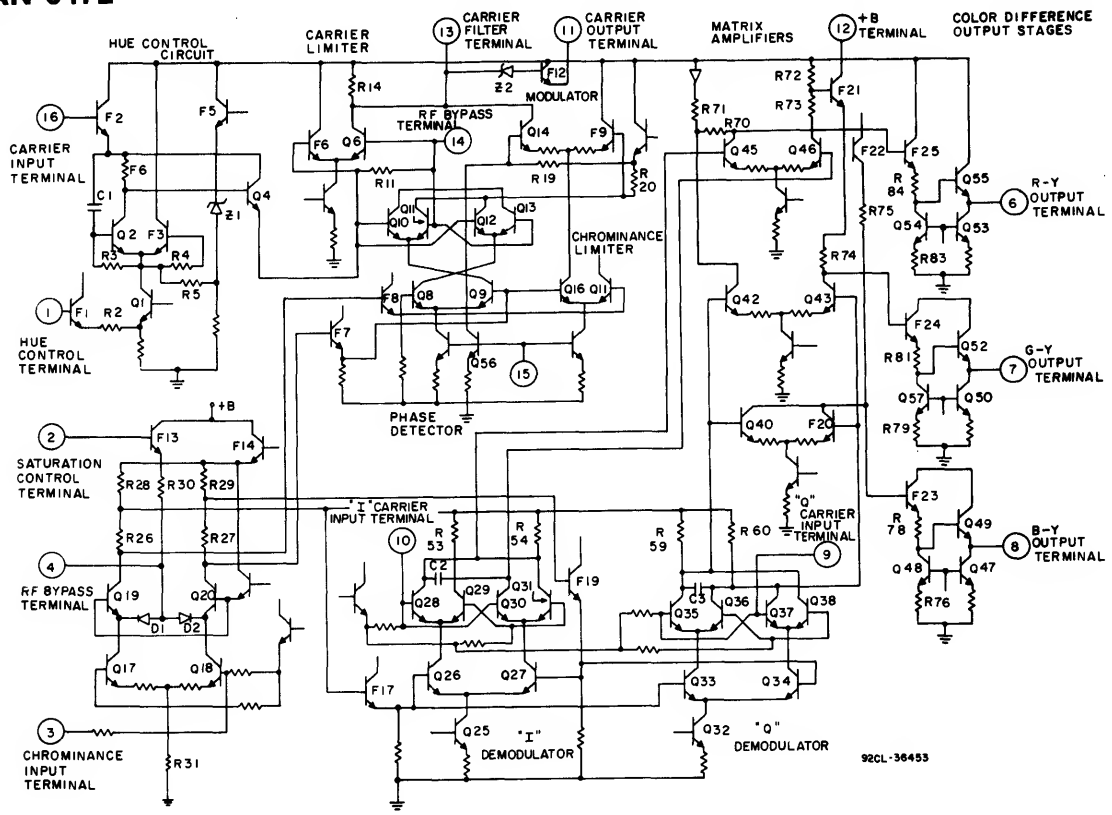


Fig. 9 - RCA CA3137 chrominance demodulator simplified diagram.

The phase-shifted carrier signal proceeds through the transistor follower Q4 and through a limiter stage F6-Q6 and appears at terminal 13. A resonant filter, connected to this terminal removes harmonics of the 3.58-MHz signal and the filtered carrier passes through zener diode Z2 and follower F12 to terminal 11. At this point, the phase of the carrier is that of the + "I" signal and is coupled to terminal 10 to drive the "I" demodulator.

An L-C phase-shift network rotates the carrier from terminal 10 by 90 degrees and this signal is applied to terminal 9 to energize the "Q" demodulator.

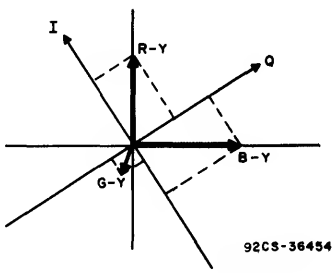


Fig. 10 - Color difference signals.

IQ Demodulators, the Matrix and the Output Circuits

The "I" demodulator formed by devices Q25 through Q31 and the "Q" demodulator formed by Q32 through Q38 detect the chrominance signal derived from the gain-controlled amplifier stage. The demodulated "I" signal is developed across load resistors R53 and R54 and similarly the "Q" signal is developed across resistors R59 and R60. Integrated capacitors C2 and C3 reduce the harmonics of the 3.58-MHz signal.

The demodulated "I" and "Q" signals are combined in matrix amplifiers to produce three-color difference signals according to the vector plot in Fig. 10.

Amplifiers Q45-Q46, Q42-Q43, and Q40-F20 driven by the "I" and "Q" demodulators produce + "I", -"I" + "Q" and -"Q" signal components which are matrixed in appropriately dimensioned matrix resistors.

The R-Y signal is produced by a + "I" signal component developed across resistors R70 + R71 and by a + "Q" signal developed across resistor R71. The G-Y signal is produced by an -"I" signal developed across resistor R72 and by a -"Q" signal across resistor R74. Finally, the B-Y signal is formed by an -"I" signal developed across resistors R72 + R73 and by a + "Q" signal across resistors R75.

Each of the color-difference signals passes through dc level shifters to adjust the quiescent point to the same dc level. The respective dc level shifters are formed by components F25, R84, Q54 and R83 for the R-Y signal; F24, R81, Q57, and R79 for the G-Y signal and F23, R78, Q48, and R76 for the B-Y signal.

The three output stages Q53-Q55, Q50-Q52, and Q47-Q49 are designed to provide a low output impedance at the three output terminals (terminals 6, 7 and 8).

The Flesh-Control Circuit

The operation of the flesh-control circuit is optional and can be activated by the viewer by means of an on-off switch connected to terminal 15. Grounding this terminal disables the flesh circuit. In the "on" position, the chrominance signal developed at collectors of amplifiers Q19-Q20 and amplitude limited in the limiter stage Q16-Q11 proceeds through a modulator stage Q14-F9 to a tuned filter at terminal 13. The amplitude of the chrominance signal passed through Q14 is a function of the instantaneous potential at the bases of devices Q14 and F9. This control potential is produced by the phase detector Q8 through Q13.

The output of this detector is the product of the chrominance signal applied to the devices Q8,Q9 and of the reference signal applied to the devices Q10 through Q13. The reference carrier to this detector is oriented in the + "I" direction to coincide with the reference carrier to the "I" demodulator. A + "I" chrominance signal, applied to the phase detector produces a control voltage to allow maximum conduction through the modulator Q14. Accordingly, the + "I" signal will pass through the limiter Q16-Q11 and the modulator Q14 to the filter at terminal 13. The + "I" reference carrier, present at this point, and the + "I" chrominance signal combine to produce a larger signal. However, the phase of the resultant signal remains unchanged. Thus, on + "I" chrominance signals, no correction is introduced by the flesh-control circuit. This is also true for chrominance signals with -"I" signal components. In the presence of these signals, the phase detector produces an output signal which cuts off modulator Q14.

Chrominance signals having a + "I" component are passed through the modulator Q14. However, the amplitude of these signals is reduced, by the action of the phase detector, in proportion to the phase difference from + "I" orientation. A current source Q56 introduces an intentional offset across resistor R19, to reduce the acceptance angle of the modulator Q14.

The chrominance signal passed through the modulator Q14 combines with the + "I" reference signal and a new reference carrier is generated across the resonant filter at terminal 13. The phase shift of the resultant carrier is in the direction of the chrominance signal reducing the original phase angle between the chrominance and the reference carrier.

Conclusion

The new IC provides the functions of chrominance demodulators, matrixing, r-f filtering, dynamic flesh control, hue and saturation controls. No tuning adjustments are required and only few external components are necessary to complete the circuit. The dynamic flesh control reduces the need for frequent hue adjustments, maintains good flesh colors, and preserves the primary red, blue, and green colors.

Acknowledgment

The author acknowledges the contributions and participation in the development of this circuit of J. Avins, L. A. Cochran, and E. J. Wittmann.

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2. Charles J. Hirsch, "A Study of the Need for Color Controls on Color TV Receivers in a Color TV System Operating Perfectly," IEEE Transactions on Broadcast and TV Receivers, November 1964, Vol. BTR-10, No. 3, pp. 71-96.

ICAN-6668

Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

by H. A. Wittlinger

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. (Transconductance $g_m = \frac{\Delta i_{out}}{\Delta e_{in}}$). The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with RCA COS/MOS devices as post-amplifiers.

Fig. 1 shows the equivalent circuit for the OTA. The output signal is a "current" which is proportional to the transconductance (gm) of the OTA established by the amplifier bias current (I_{ABC}) and the differential input voltage. The OTA can either source or sink current at the output terminals, depending on the polarity of the input signal.

The availability of the amplifier bias current (I_{ABC}) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

Circuit Description

A simplified block diagram of the OTA is shown in Fig. 2. Transistors Q1 and Q2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Fig. 3a shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a "current-mirror", with similar geometries for Q_A and Q_B, the current I' establishes a second current I whose value is essentially equal to that of I'.

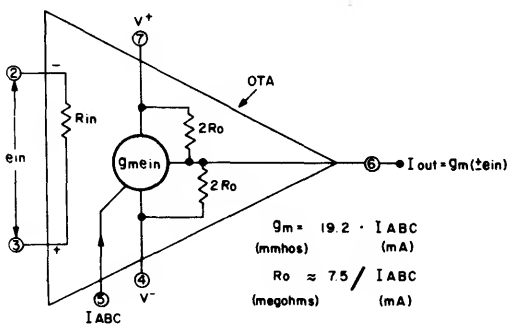


Fig. 1— Basic equivalent circuit of the OTA.

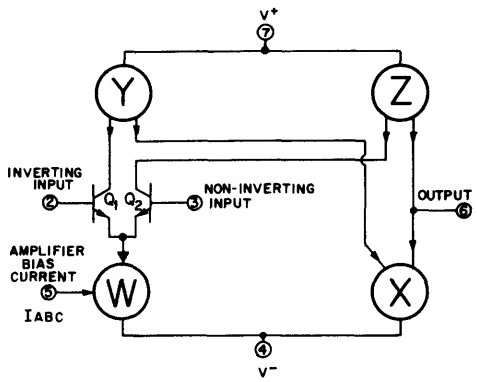


Fig. 2— Simplified diagram of OTA.

This basic current-mirror configuration is sensitive to the transistor beta (β). The addition of another active transistor, shown in Fig. 3b, greatly diminishes the circuit sensitivity to transistor beta (β) and increases the current-source output impedance in direct proportion to the transistor beta (β). Current-mirror W (Fig. 2) uses the configuration shown in Fig. 3a, while mirrors X, Y, and Z are basically the version shown in Fig. 3b. Mirrors Y and Z employ p-n-p transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes "current-mirrors" in more detail.

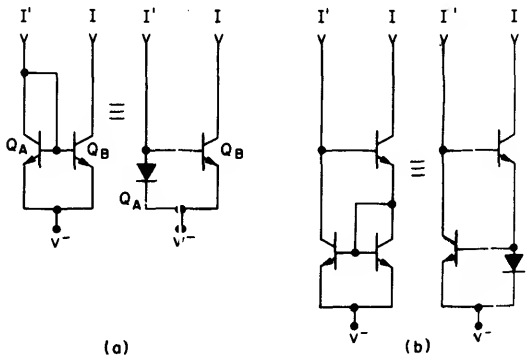


Fig. 3— Basic types of current mirrors; a) diode-connected transistor paired with transistor; b) improved version: employs an extra transistor.

Fig. 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, I_{ABC}, establishes the emitter current of the input differential amplifier Q1 and Q2. Hence, effective control of the differential transconductance (g_m) is achieved.

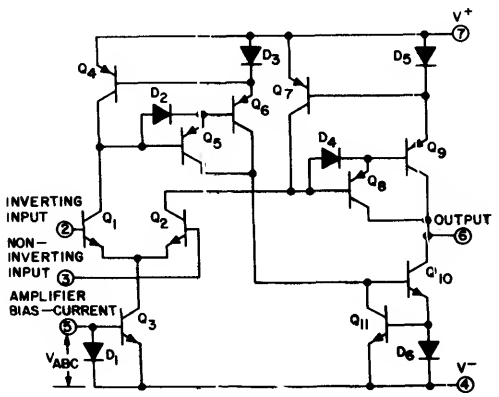


Fig. 4— Schematic diagram of OTA types CA3080 and CA3080A.

The g_m of a differential amplifier is equal to

$$\frac{q\alpha I_C}{2KT}$$

(see Ref. 2 for derivation) where q is the charge on an electron, α is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), I_C is the collector current of the constant-current source (I_{ABC} in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_m = 19.2 \times I_{ABC}$, where gm is in mmho and I_{ABC} is in milliamperes. The temperature coefficient of g_m is approximately -0.33%/°C (at room temperature).

Transistor Q3 and diode D1 (shown in Fig. 4) comprise the current mirror "W" of Fig. 2. Similarly, transistors Q7, Q8 and Q9 and diode D5 of Fig. 4 comprise the generic current mirror "Z" of Fig. 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q10, Q11, and diode D6 of Fig. 2 comprise the current-mirror "X" of Fig. 2. Diodes D2 and D4 are connected across the base-emitter junctions of Q5 and Q8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the

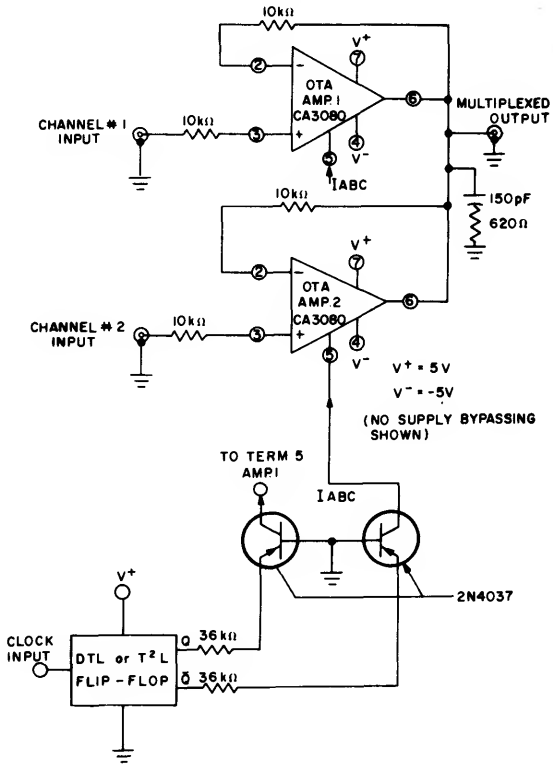


Fig. 5— Schematic diagram of OTAs in a two-channel linear time-shared multiplex circuit.

"Z" and "X" current-mirror of Fig. 2, providing a push-pull Class A output stage that produces full differential g_m. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of g_m and input offset voltage, less variation of input offset voltage with variation of I_{ABC} and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000 MΩ.

APPLICATIONS

Multiplexing

The availability of the bias current terminal, I_{ABC}, allows the device to be gated for multiplex applications. Fig. 5 shows a simple two-channel multiplex system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example positive and negative 5-V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15 V, with the positive-supply at 5 V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through p-n-p transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$. This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8 shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.

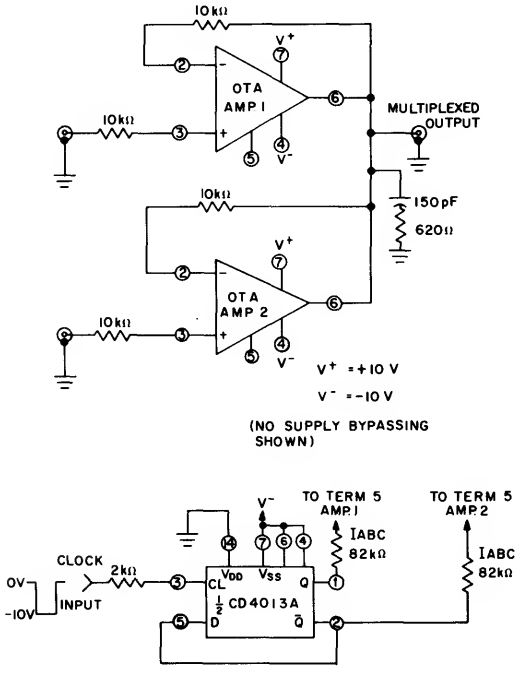
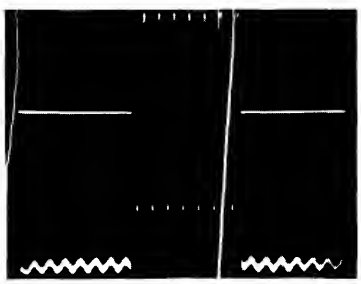


Fig. 6— Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.

TOP TRACE: MULTIPLEXED OUTPUT 1V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2V/DIV & 5 μsec/DIV

Fig. 7— Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.



TOP TRACE: 1V/DIV & 100μsec/DIV — OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

Fig. 8— Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance $(\frac{1}{g_m})$ of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_O \text{ (open-loop)}}{A \text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

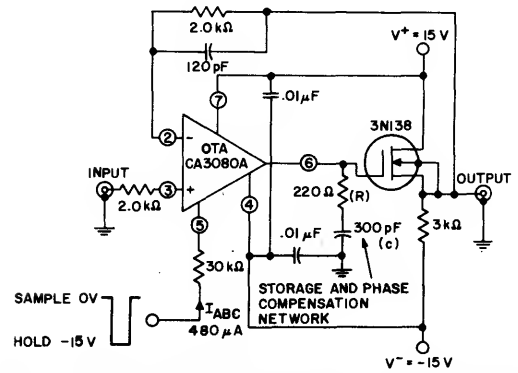
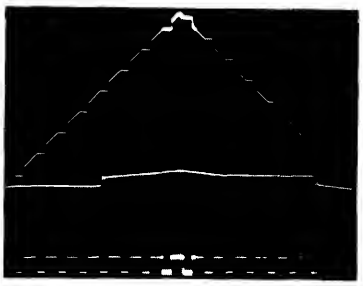


Fig. 9– Schematic diagram of OTA in a sample-and-hold circuit.

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA $(I = C\frac{dv}{dt})$.



TOP TRACE: SAMPLED SIGNAL 1V/DIV & 20μsec/DIV
CENTER TRACE: TOP PORTION OF UPPER SIGNAL 1 V/DIV & 2μsec/DIV
BOTTOM TRACE: SAMPLING SIGNAL 20V/DIV & 20μsec/DIV

Fig. 10– Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.

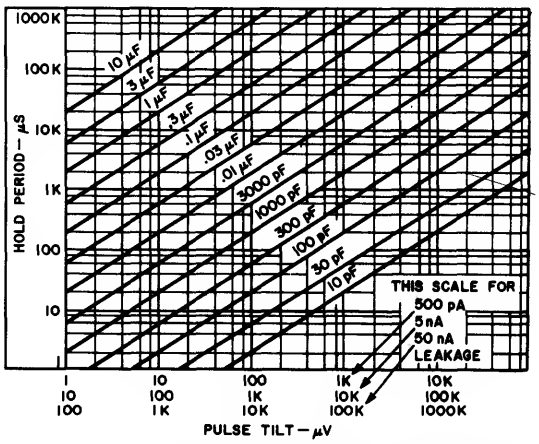
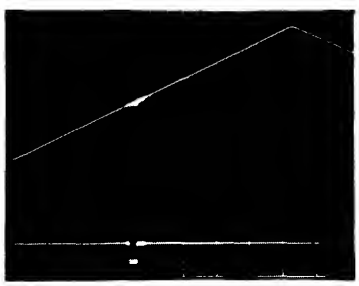


Fig. 11– Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.

Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.

TOP TRACE:SAMPLED SIGNAL 1 V/DIV & 20 msec/DIV
CENTER TRACE:WORSE CASE TILT 20 mV/DIV & 20 msec/DIV

Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.



TOP TRACE:INPUT AND OUTPUT SUPERIMPOSED 1 V/DIV & 2 μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20 V/DIV & 2 μsec/DIV

Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.

TOP TRACE: INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100 mV/DIV & 100 ns/DIV
BOTTOM TRACE: SAMPLING SIGNAL 20 V/DIV & 100 ns/DIV

Fig. 14– Oscilloscope photo showing response of sample-and-hold circuit (Fig. 9).

In Fig. 14, the trace of Fig. 13 has been expanded (100 mV/div and 100 ηsec/div) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1 μs. The resistor in series with the 300 pF phase-compensation capacitor was adjusted to 68 ohms for minimum recovery time.

Fig. 15 shows the basic circuit of Fig. 9 implemented with an RCA 2N4037 p-n-p transistor to minimize capacitive feedthrough. Fig. 16 shows oscilloscope photographs taken with the circuit of Fig. 15 operating in the sampling mode at supply-voltage of ±15 V. The 9.1 kΩ resistor in series with the p-n-p transistor emitter establishes amplifier-bias-current (I_{ABC}) conditions similar to those used in the circuit of Fig. 9.

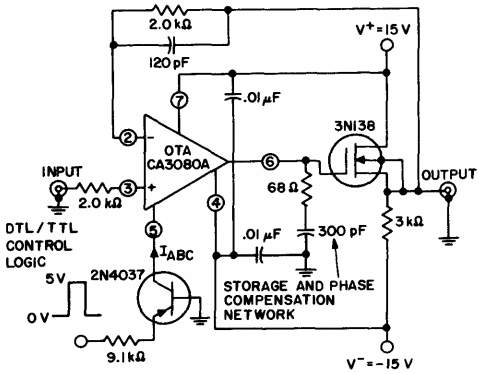
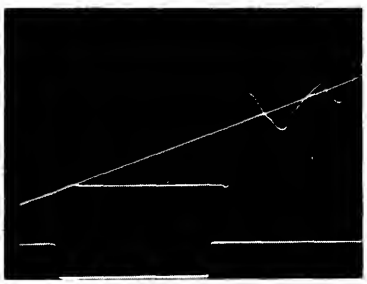


Fig. 15– Schematic diagram of the OTA in a sample-and-hold configuration (DTL/TTL control logic).

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$, corresponding to the first pole in the



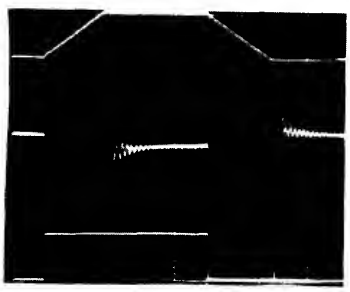
TOP TRACE: INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100 mV/DIV & 100 ns DIV
BOTTOM TRACE: SAMPLING SIGNAL 5 V/DIV & 100 ns/DIV

Fig. 16– Oscilloscope photo for circuit of Fig. 15 operating in sampling mode.

amplifier at an output current level of 500 μA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figs. 9 and 15. The 120 pF capacitor shunting the 2 kΩ resistor improves the amplifier transient response.

Fig. 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Fig. 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dV/dt) = 1.8V/μs.

The center trace in Fig. 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2 mV/div. The output of the amplifier system settles to within 2 mV (the offset voltage specification for the CA3080A) of the input level in 1 μs after slewing.



TOP TRACE: OUTPUT 5V/DIV & 2μsec/DIV
CENTER TRACE: DIFFERENTIAL COMPARSION OF INPUT AND OUTPUT 2mV/DIV— 0 VOLTS THROUGH CENTER— 2μsec/DIV
BOTTOM TRACE: INPUT 5V/DIV & 2μsec/DIV

Fig. 17— Oscilloscope photo showing circuit of Fig. 9 operating in the linear sample-mode.

Fig. 18 is a curve of slew-rate as a function of amplifier-bias-current (I_{ABC}) with various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current (I_{ABC}) when the OTA is supplying its maximum output current.

Gain Control — Amplitude Modulation

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current (I_{ABC}) in the OTA because its g_m is directly proportional to the amplifier-bias-current (I_{ABC}). For a specified value of amplifier-bias-current, the output current (I_O) is equal to the product of g_m and the input signal magnitude. The output voltage swing is the product of output current (I_O) and the load resistance (R_L).

Fig. 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current (I_O) is equal to $-g_m V_x$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, I_{ABC}. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current (I_{ABC}) through resistor Rm. Amplitude modulation of the carrier frequency occurs because variation of the voltage Vm forces a change in the amplifier-bias-current (I_{ABC}) supplied via resistor Rm. When Vm goes positive the bias current increases which causes a corresponding increase in the g_m of the OTA. When the Vm goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the g_m of the OTA.

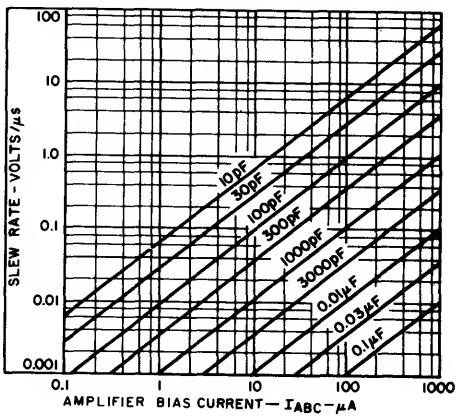


Fig. 18— Slew rate as a function of amplifier-bias-current (I_{ABC}) with phase-compensation capacitance as a parameter.

As discussed earlier, $g_m = 19.2 \times I_{ABC}$, where g_m is in millimhos when I_{ABC} is in milliamperes. In this case, I_{ABC} is approximately equal to:

$$\frac{Vm - (V^-)}{Rm} = I_{ABC}$$

$$(I_O) = -g_m Vx$$

$$g_m Vx = (19.2)(I_{ABC})(Vx)$$

$$I_O = \frac{-19.2\,[Vm - (V^-)]\,Vx}{Rm}$$

$$I_O = \frac{19.2\,(Vx)\,(V^-)}{Rm} - \frac{19.2\,(Vx)\,(Vm)}{Rm}\ \text{(Modulation Equation).}$$

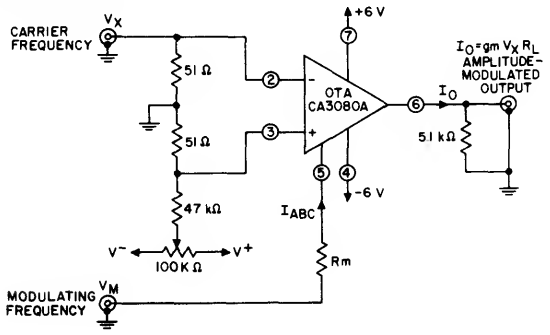


Fig. 19– Amplitude modulator circuit using the OTA.

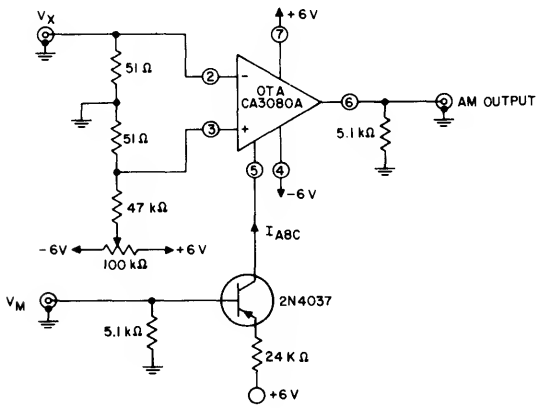


Fig. 20– Amplitude modulator using OTA controlled by p-n-p transistor.

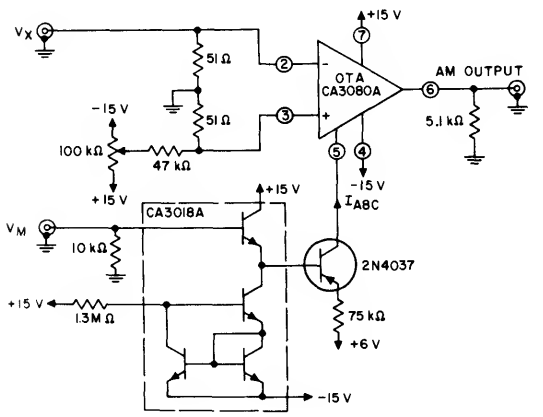


Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of Vm, and the second term represents the modulation, which either adds to or subtracts from the first term. When Vm is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term

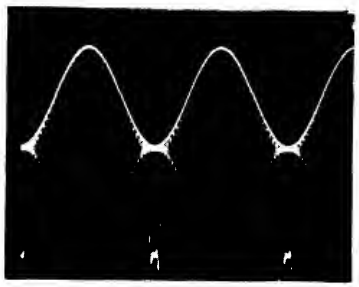
$$(19.2)\,(Vx)\ \frac{V_{ABC}}{Rm}$$

involving the amplifier-bias-current terminal voltage (V_{ABC}) (see Fig. 4 for V_{ABC}) was neglected. This term was assumed to be small because V_{ABC} is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a p-n-p transistor), the effect of V_{ABC} variation is eliminated and transferred to the involvement of the p-n-p transistor base-emitter junction characteristics. Fig. 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation. If an n-p-n transistor is added to the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

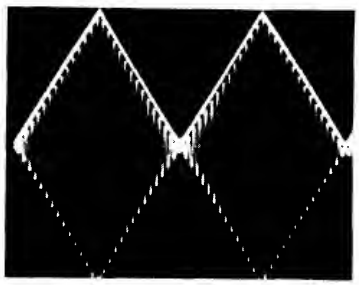
Four-Quadrant Multipliers

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

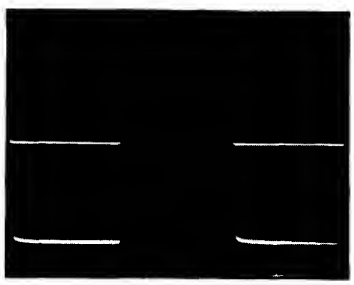
To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m\,(-Vx)$ because the input is applied to the



(a) TOP TRACE: MODULATION FREQUENCY INPUT ≃20 VOLTS P-P & 50μsec/DIV
CENTER TRACE: AMPLITUDE MODULATE OUTPUT 500mV/DIV & 50μsec/DIV
BOTTOM TRACE: EXPANDED OUTPUT TO SHOW DEPTH OF MODULATION 20mV/DIV & 50μsec/DIV



(b) TOP TRACE: MODULATION FREQUENCY INPUT 20 VOLTS & 50μsec/DIV
BOTTOM TRACE: AMPLITUDE MODULATED OUTPUT 500mV/DIV & 50μsec/DIV



(c) TOP TRACE: GATED OUTPUT 1V/DIV AND 50μsec/DIV
BOTTOM TRACE: VOLTAGE EXPANSION OF ABOVE SIGNAL-SHOWING NO RESIDUAL 1mV/DIV AND 50μsec/DIV— AT LEAST 80 db OF ISOLATION fq = 100 kHz

Fig. 22— a) Oscilloscope photo of amplitude modulator circuit of Fig. 15 with R_m = 40 kΩ, V^+ = 10 v and V- = -10 V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.

inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when R = $1/g_m$. The current for this configuration is:

$$I_O = \frac{-19.2\ Vx\ Vm,}{Rm} \text{ and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).

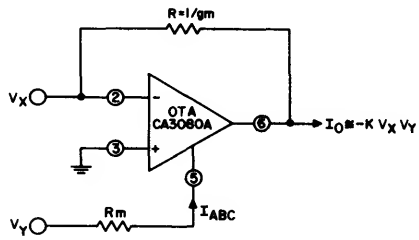


Fig. 23— Basic four quadrant analog multiplier using an OTA.

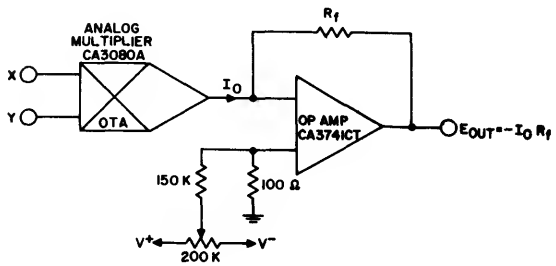


Fig. 24— OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to

compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the g_m of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.

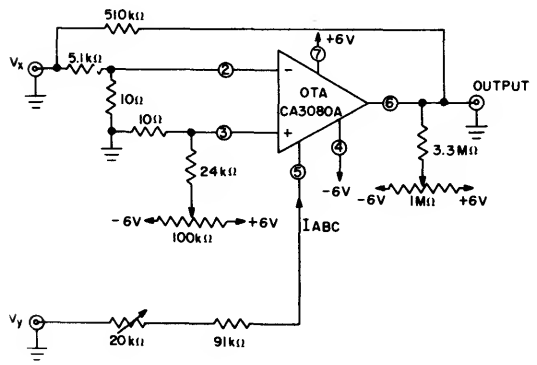


Fig. 25– Schematic diagram of analog multiplier using OTA.

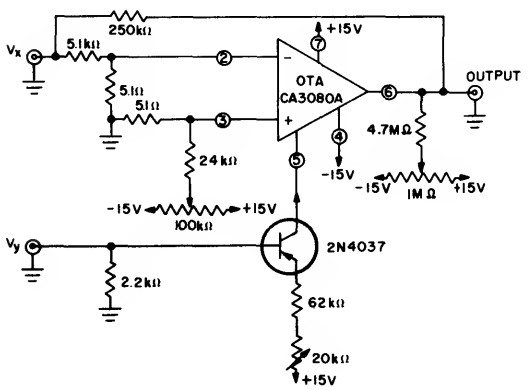


Fig. 26– Schematic diagram of analog multiplier using OTA controlled by a p-n-p transistor.

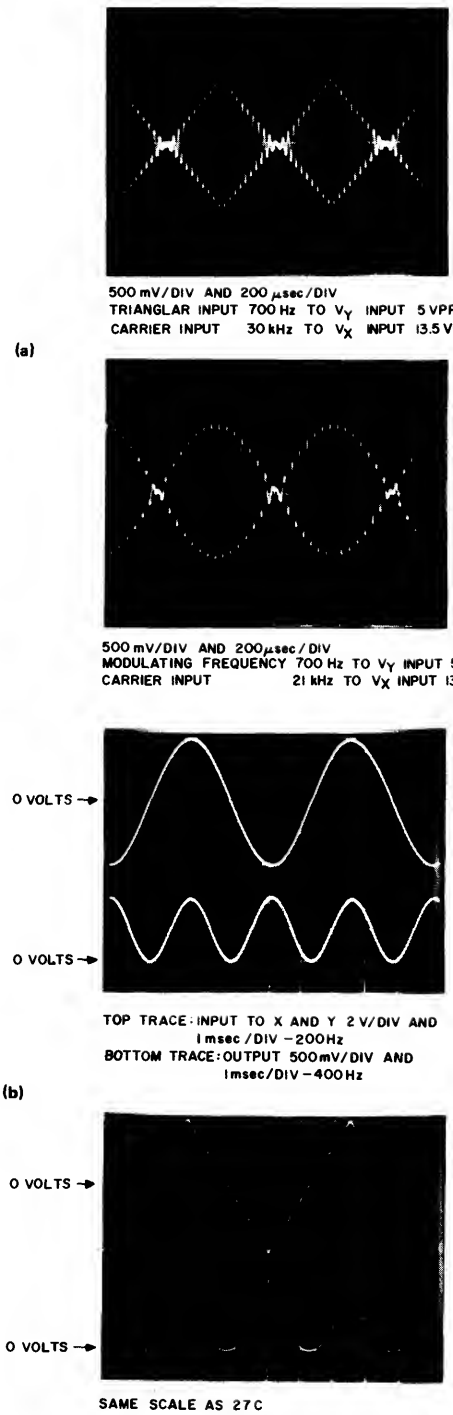


Fig. 27– a) Waveforms observed with OTA analog multiplier used as a suppressed carrier generator; b) waveforms observed with OTA analog multiplier used in signal-squaring circuits.

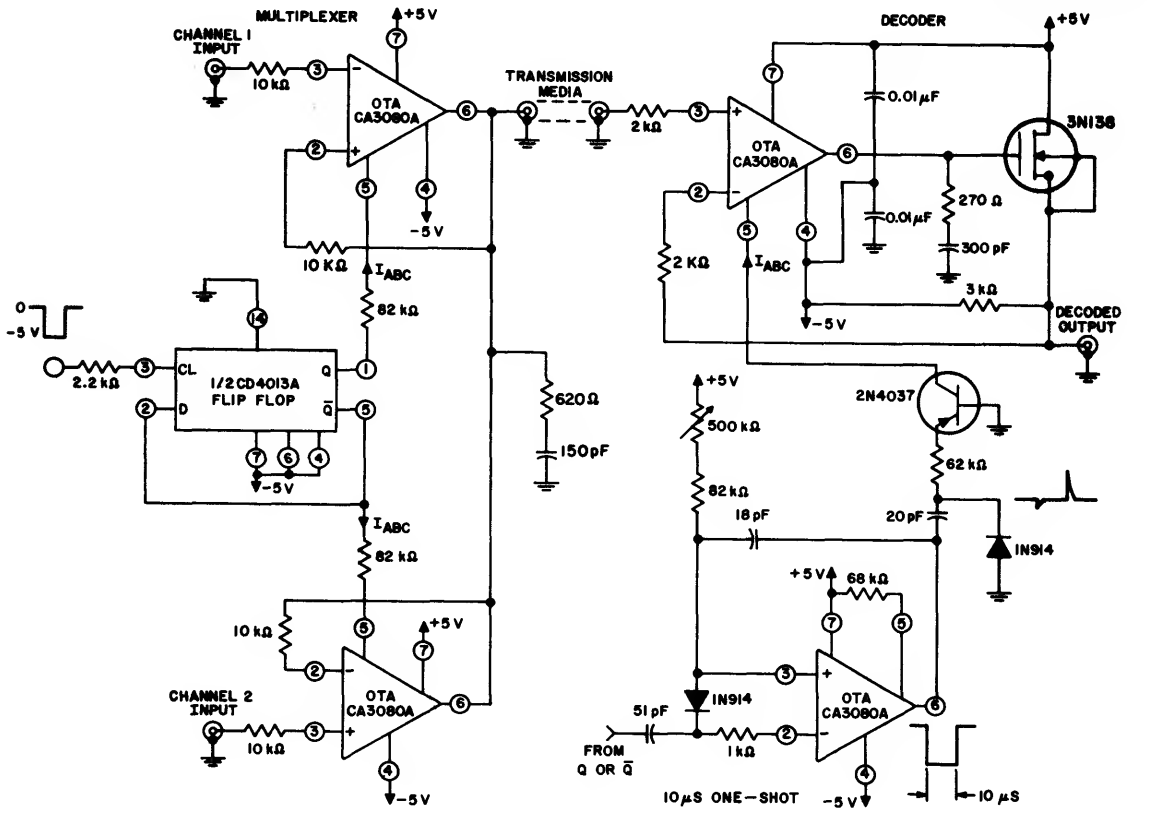


Fig. 28– Two-channel multiplexer and decoder using OTAs.

2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the g_m balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the g_m of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

Figs. 27a and 27b show oscilloscope photographs of the output signals delivered by the circuit of Fig. 26 which is connected as a suppressed-carrier generator. Figs. 27c and 27d contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular-wave inputs.

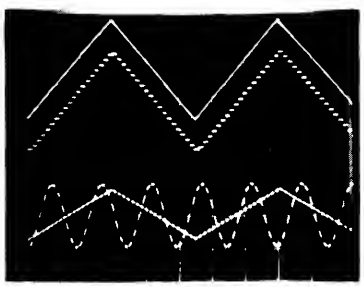
If ±15-V power supplies are used (shown in Fig. 26), both inputs can accept ±10-V input signals. Adjustment of this multiplier circuit is similar to that already described above.

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

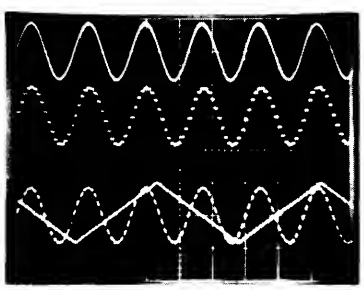
Other forms of four-quadrant multipliers using operational transconductance amplifiers have been published. (See Ref. 2.) the circuit shown in Ref. 2 tends to reduce the effects of the previously discussed g_m temperature dependency.

Linear Multiplexer – Decoder

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Fig. 28. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Fig. 29 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10 μsec delay- "one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-

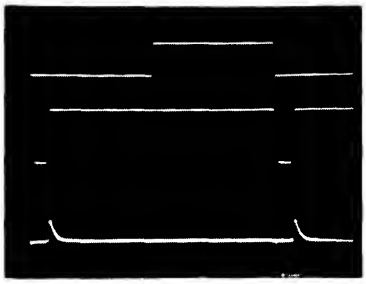


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (2 VOLTS/DIV)

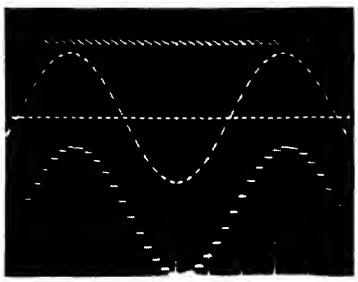


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (1VOLT/DIV)

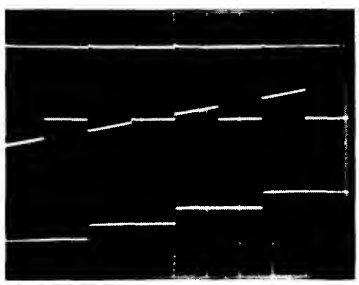
Fig. 29– Waveforms showing operation of linear multiplexer/sample-and-hold decode circuitry (Fig. 28).



20 μsec/DIV
(a) TOP TRACE: FLIP-FLOP OUTPUT (5 VOLTS/DIV)
CENTER TRACE: "ONE-SHOT" OUTPUT (5 VOLTS/DIV)
BOTTOM TRACE: PULSE AT THE COLLECTOR OF THE 2N4037 TRANSISTOR (0.1 VOLTS/DIV)



(b) TOP TRACE: COLLECTOR OF PNP TRANSISTOR (0.5 V/DIV)
CENTER TRACE: MULTIPLEXED OUTPUT WITH ONE CHANNEL INPUT GROUND (0.5V/DIV)
LOWER TRACE: DECODED OUTPUT (0.5 V/DIV)
TIME ALL SCALES: 5 msec/DIV



(c) TIME EXPANSION TO 500 μsec/DIV

Fig. 30– (a) Waveforms showing timing of flip-flop, delay– "one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). (c) 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).

hold circuit for approximately 1 μs. Fig. 30 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10 μsec "one-shot" to decode a signal.

High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOS/FET) shown in Fig. 9. This configuration yields a voltage gain equal to the (g_m) (R_o) product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Fig. 9) are limited by the 3N138 MOS/FET performance and its source-terminal load. In the positive direction, the MOS/FET may be driven into saturation; the source-load resistance and the MOS/FET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CD4007A (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CD4007A has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

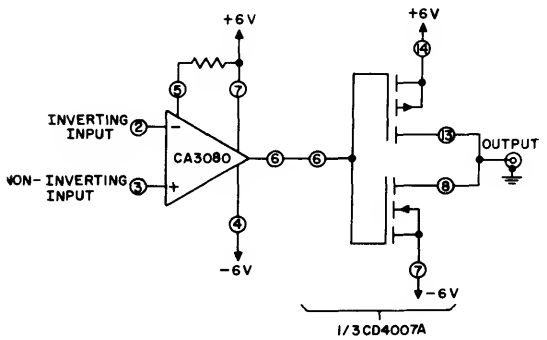


Fig. 31— Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/μsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/μsec (shown in Fig. 32). Even when the three "inverter"/amplifiers in the CD4007A are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/μsec. A slew-rate of about 1 V/μsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

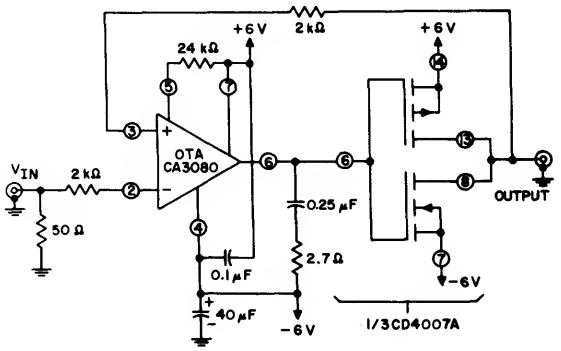


Fig. 32— Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

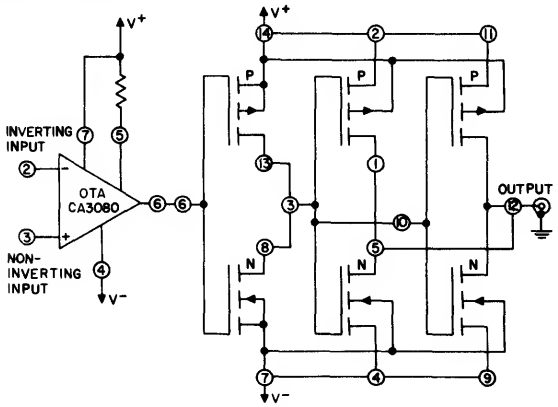


Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.

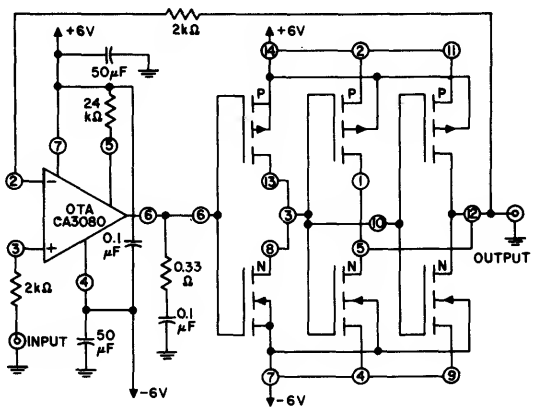
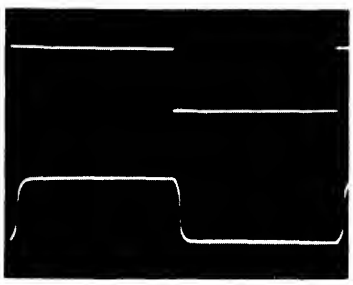


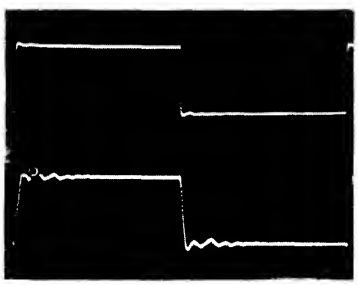
Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).

(a)



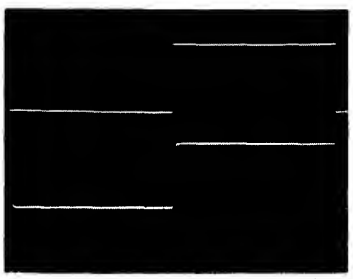
TOP TRACE: INPUT – 5 V/DIV – 100 μsec/DIV
BOTTOM TRACE: OUTPUT SAME SCALE

(b)



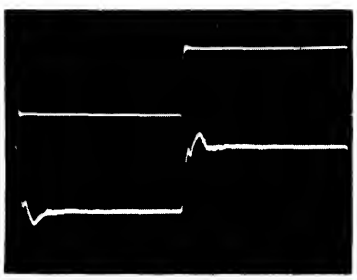
TOP TRACE: INPUT – 50 mV/DIV – 1 μsec/DIV
BOTTOM TRACE: OUTPUT – SAME SCALE

(c)



TOP TRACE: INPUT – 5 V/DIV – 100 μsec/DIV
BOTTOM TRACE: OUTPUT – SAME SCALE

(d)



TOP TRACE: INPUT – 50 mV/DIV – 1 μsec/DIV
BOTTOM TRACE: OUTPUT – SAME SCALE

Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.

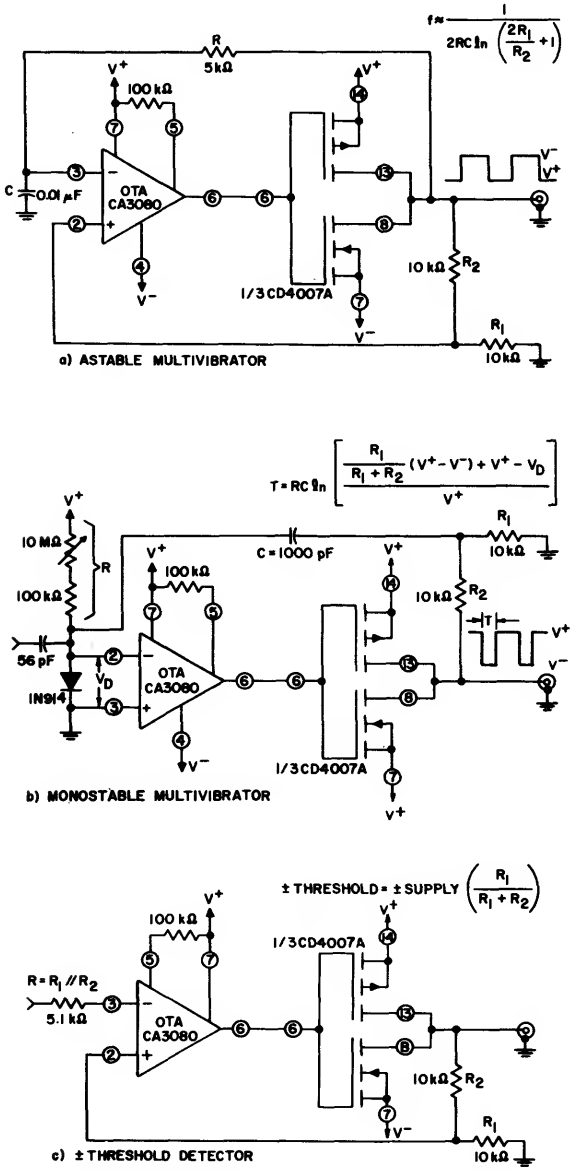


Fig. 36— Multistable circuits using the OTA and COS/MOS Inverter/Amplifiers: a) astable multivibrator; b) monostable multivibrator; c) threshold detector (plus or minus). For greater current output, the remaining amplifiers in the CD4007A may be connected in parallel with the single stage shown.

Fig. 36 shows a variety of circuits that can be assembled using the CA3080 to drive one "inverter"/amplifier in the CD4007A. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs. power consumption tradeoffs may be made by adjustment of the I_{ABC} current to the CA3080. The quiescent power consumption of the circuits shown in Fig. 36 is typically 6 mW, but can be made to operate in the micropower region by suitable circuit modifications.

Micropower Comparator

The schematic diagram of a micropower comparator is shown in Fig. 37. Quiescent power consumption of this circuit is about 10 μW (typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420 μW. Under these conditions, the circuit responds to a differential input signal in about 8 μsec. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 nsec., but the power consumption rises to 21 mW.

The differential amplifier input common-mode range for the circuit of Fig. 37 is -1V to +10.5 V. Voltage of the micropower comparator is typically 130 dB. For example, a 5 μV input signal will toggle the output.

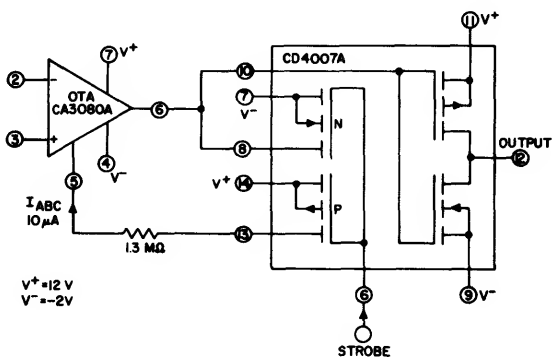


Fig. 37— Schematic diagram of micropower comparator using the CA3080A and COS/MOS CD4007A.

APPENDIX I
CURRENT MIRRORS

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Fig. A shows this basic configuration of the current-mirror. Q2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_b$. If a current I_1 is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q2 such that Q2 "sinks" the applied current I_1.

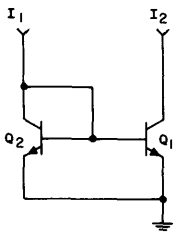


Fig. A— Diode – transistor current source.

If the base of a second transistor (Q1) is connected to the base-to-collector junction of Q2, shown in Fig. A, Q1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current (I_1) and the collector current (I_2) of transistor Q, is due to the fact that the base-current for both transistors is supplied from I_1. Fig. B shows this current division, using a unit of base current (1) to each transistor base. This base

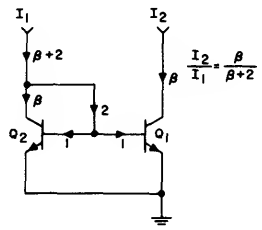


Fig. B— Diode – transistor current source. Analysis of current flow.

current causes a collector current to flow in direct proportion to the β of each transistor. The ratio of the "sinking" current I_2 to the input current I_1 is therefore equal to $\frac{I_2}{I_1} = \beta/(\beta+2)$. Thus, as β increases, the output "sinking" current (I_2) level approaches that of the input current (I_1). The curves in Fig. C show this ratio as a function of the transistor β. When the transistor β is equal to 100, for example, the difference between the two currents is only two percent.

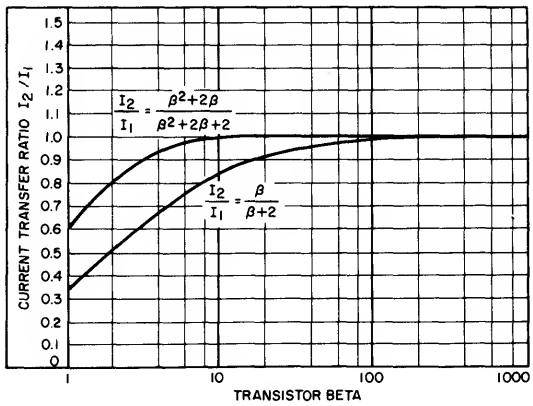


Fig. C— Current transfer ratio I_2/I_1 as a function of transistor beta.

Fig. D shows a curve-tracer photograph of characteristics for the circuit of Figs. A and B. No consideration in this discussion is given to the variation of the transistor (Q1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q1.

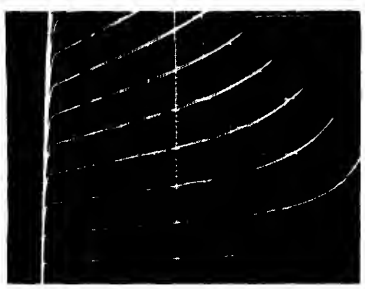


Fig. D— Photo showing results of Figs. A & B.

This diode-connected transistor (Q3 in Fig. E) may be considered as a current-sampling diode that senses the emitter-current of Q1 and adjusts the base current Q1 (via Q2) to maintain a constant-current in I_2. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Fig. F shows the improved output resistance characteristics of the circuit of Fig. E. (Compare Fig. D and F).

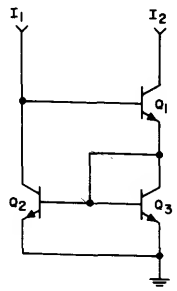


Fig. E— Diode – 2 transistor current source.

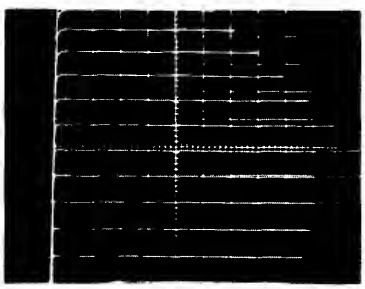


Fig. F— Photo showing results of Fig. E.

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3.

The resulting current-transfer ratio $I_2/I_1 = \frac{\beta^2+2\beta}{\beta^2+2\beta+2}$ Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.

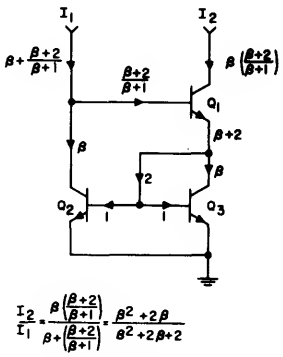


Fig. G— Current flow analysis of Fig. E.

Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

Acknowledgements

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.

2 RCA published data for CA3060 File No. 404

ICAN-6669

FET-Bipolar Monolithic Op Amps Mate Directly to Sensitive Sources

by Robert D. Baird

Monolithic op amps containing both field-effect and bipolar devices provide the high-input impedance needed by a class of circuits that can "touch" or "feel" their environment. The input stages of these circuits often double as sensors. But when external sensors are needed, only the simplest transducers are required. What's more, these mixed-technology chips don't sacrifice other op-amp qualities like slew rate, bandwidth, offsets and drifts to get high-input impedance. And even though they are only a few years old, these op amps now sell at "jelly-bean" prices.

The two types of single-chip FET-bipolar op amps, BiFETs (from TI and National Semiconductor) and BiMOS (from RCA), boast typical input impedances of at least $10^9\ \Omega$ (see table). So, for high input impedance, any op amp in the table will do.

High Impedance Sources Can't Resist

Input impedance can be critical, especially when mating with the high source impedance of many physical events. Usually the higher the input impedance, the better. Here the standouts are the BIFET LM356, National Semiconductor's single amplifier with 10^{12}-Ω typical input impedance, or BiMOS devices like the CA3140, RCA's single amplifier, and the CA3240, RCA's dual amplifier. Both have 1.5×10^{12}-Ω typical input impedances.

But a dual-amplifier chip offers an additional plus when you need a differential-input circuit—two isolated inputs in one package. One circuit that needs two isolated high-impedance inputs is a differential amplifier for biomedical instrumentation (Fig. 1).

A biomedical amplifier needs a high impedance to match the source impedance of bioelectric events. In addition, the test subject must be protected against the hazard or even the discomfort stemming from excessive input current.

In Fig. 1, BIMOS input buffers are used in an otherwise conventional instrumentation amplifier. Because the CA3240's input current is only 50 pA max., you can use

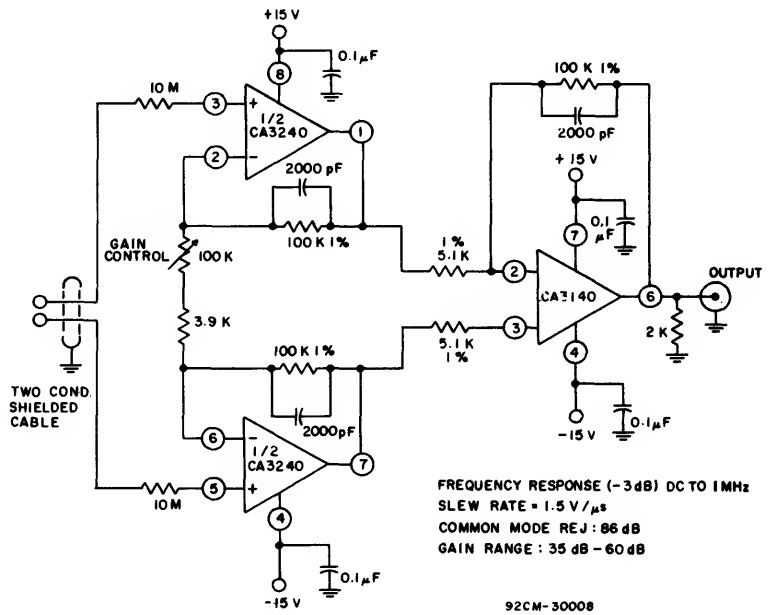


Fig. 1 - The high-input impedance of each op amp in the CA3240 permits 10-MΩ resistors in the probe circuits.

10-MΩ resistors in series with the input probes. Even under a fault condition, these resistors limit current to 2 μA. In addition, because the input current is so low, the effective input-offset voltage is low—even when the contact resistance of the electrodes is noticeably unequal.

To minimize hum and other noise pickup, the circuit must have a high common-mode-rejection ratio. So, match the following critical resistor pairs by using 1% resistors: R_2 and R_3, R_4 and R_6, R_5 and R_7.

With the resistors matched, compute the differential gain from

$$V_{out} = (V_{in1} - V_{in2})\,(1 + 2\,R_3/R_1)\,(R_5/R_4).$$

With an oscilloscope, the biomedical amplifier in Fig. 1 produces electrocardiograms. The electrodes have been placed with V_{in1} at the left side of a human chest, V_{in2} at the center, and Common at the left ankle.

A typical display for such an instrument is shown in Fig. 2. This waveform reflects a total sensitivity, including the scope, of 1 mV/div for which the differential gain of the instrumentation amplifier is set, via R_1, at approximately 40 dB.

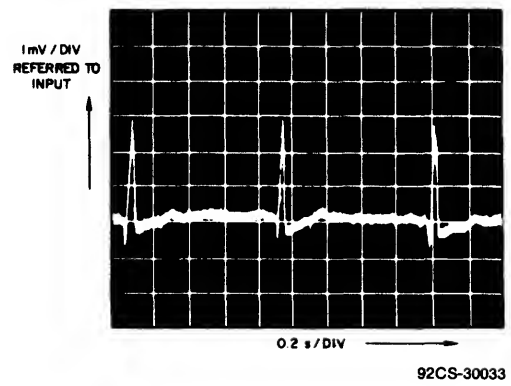


Fig. 2 - The electrocardiogram's low "grass" and hum levels result from matching resistors in the circuit of Fig. 1 for a high common-mode rejection ratio.

Even Water Passes Enough Current

Another circuit that uses the high-input impedance of BiMOS op amps, a dual liquid-level detector, is shown in Fig. 3. Most liquids, including tap water, have enough ions in solution to conduct a slight current. Measuring this current, though, does demand high-input impedance.

The ion current passes through either of two metallized-grid sensors, which can be etched on PC boards or deposited on glass wafers. When liquid covers either sensor, current produced by an applied 0.5 V flows between the immersed grid's two poles and shifts the output voltage of one of the CA3240's op amps. The voltage shift equals the product of the grid current and the feedback resistance.

Because the op amp's input current is low, even the minuscule current passing through the sensor can be processed in a conventional current-to-voltage converter. With a 12-MΩ feedback resistor, just 1 μA of sensor current changes the converter's output as much as 10 to 12 V.

This 10 to 12-V swing is the input to the second stage. Here, the converter outputs combine so that the indicator LED is off when the liquid covers the lower but not the upper sensor. When the liquid covers neither or both of the sensors, the LED goes on.

With appropriate relays or triacs, the third and final stage can control pumps that raise or lower the liquid. To reduce the response time of the PC-type sensors, prevent liquid from soaking into the board by coating the spaces between the grids with wax. Because the input impedance is so high, even the little water that a PC board absorbs will have an effect.

Let Your Fingers Do the Conducting

As useful as it is otherwise, a very high-input impedance circuit may enjoy its greatest popularity as a replacement for the most often used electrical component—the simple switch. Besides user appeal stemming from its almost magical operation, a non-mechanical switch would solve the reliability problem inherent with moving parts once and for all.

In the switch circuit of Fig. 4, the high-input impedance of the CA3240 is again used to sense small currents. But this time the current passes through the user's skin when he contacts two points on a touch plate. As with the biomedical amp in Fig. 1, user safety is all important. And again high

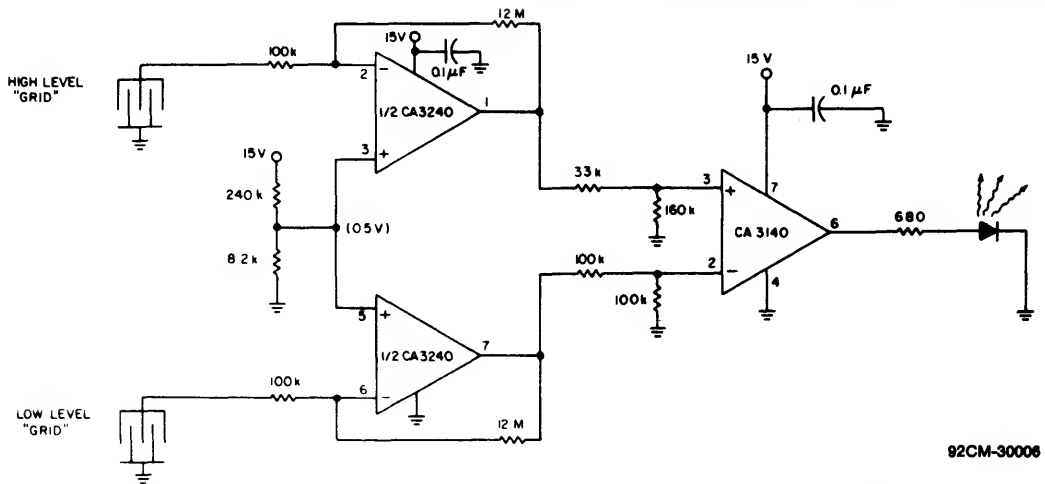


Fig. 3 - In a liquid-level sensing system, high feedback resistances yield the required high gain.

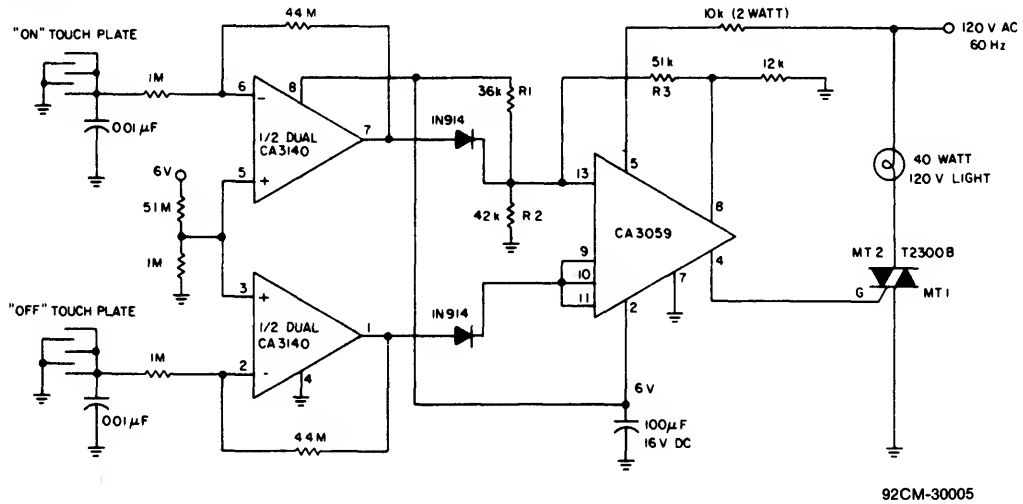


Fig. 4 - The op amp's high-input impedance allows 1-MΩ input resistors to be used in this non-mechanical switch. These resistors in turn limit the shock hazard as well as the current that passes through the skin of the user.

Input Impedances of Mixed-Technology Monolithic Operational Amplifiers

Op Amp	Manufacturing Process	Manufacturer	Op Amps /Pkg.	Input Impedance (Typical Ω)
CA3140	BiMOS	RCA	1	1.5×10^{12}
CA3240	BiMOS	RCA	2	1.5×10^{12}
TL081	BiFET	TI	1	10^{9}
TL082	BiFET	TI	2	10^{9}
TL083	BiFET	TI	2	10^{9}
TL084	BiFET	TI	4	10^{9}
LM356	BiFET	National Semiconductor	1	10^{12}
LM13741	BiFET	National Semiconductor	4	5×10^{11}

resistance ensures low current and shock protection. Fortunately, the high-input impedance of a CA3140 mates easily with the megohm resistance needed.

The input stages for the On and Off touch plates are inverting amps. The resistors determine the output swing. With the resistance values in Fig. 4, a completed circuit at the input swings the output to the positive rail. Each positive transition actuates the CA3059 zero-voltage switch, used here as a latching circuit and zero-crossing triac driver.

A positive pulse on pin 7 of the CA3240 causes the triac to conduct. The triac is then held in conduction by the CA3059 and its associated positive feedback circuit consisting of R_1, R_2 and R_3. A pulse at pin 1 of the CA3240 turns off the triac. Note that the power supply, internal to the CA3059, also supplies the CA3240.

Application of the CA3134 and CA3144 TV Luminance Processors

by T.H. Campbell

This Note describes application information for both the CA3143 and CA3144 luminance processors.[1] These two types are functionally identical, the differences being in input polarity and the gain of the video amplifier. Both IC's provide terminals for the dc control of peaking, contrast, and brightness. Additionally, black-level clamping is provided along with inputs for horizontal and vertical blanking and an inhibit pulse for the black-level clamp. Fig. 1 shows a simplified functional block diagram of the system with external components.

Peaking

The CA3143 and CA3144 were designed to be used with a tapped-delay-line transversal-filter peaking circuit, but can be used with a standard delay line, as shown in Fig. 3, when peaking need not be "ideal", dc peaking-control features will be retained. Although, obviously (as shown by Figs. 2 and 4), the performance is superior when the tapped delay line is used, the following text may stimulate interest in the lower-cost approach.

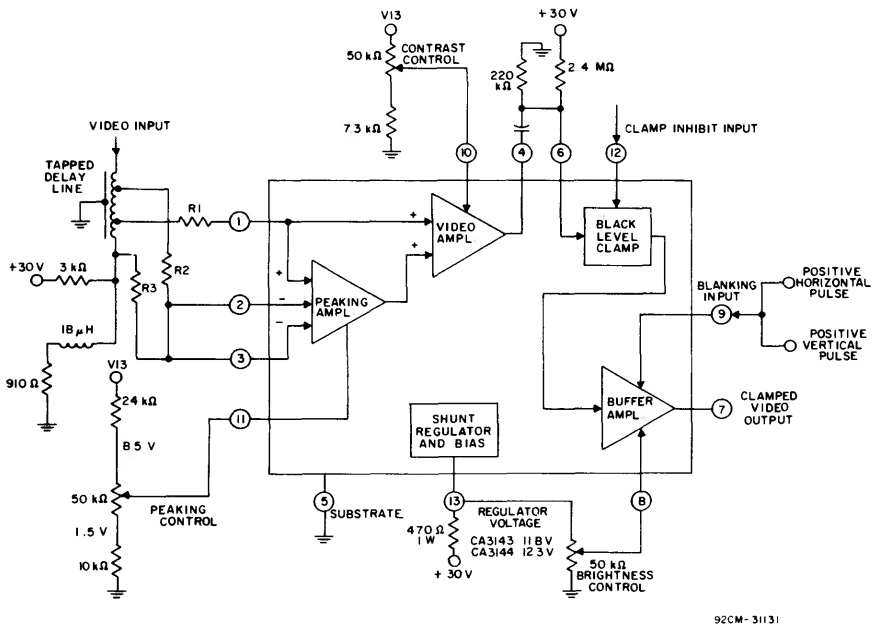


Fig. 1 - Functional block diagram of the CA3143. The CA3144 is identical except for terminals 8 and 9, which are the reverse of that shown.

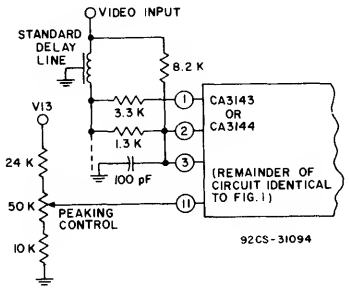


Fig. 3 - Peaking using RC network.

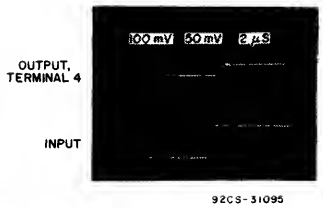


Fig. 2 - Maximum peaking using transversal filter of Fig. 1.

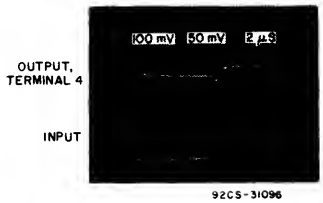


Fig. 4 - Maximum peaking using circuit of Fig. 3.

The theory of transveral filters[2] is not discussed in detail here, but, basically, can be described as tailoring of the system transient response so that desirable amounts of preshoot are obtained. The maximum peaking transient-response characteristics for the transversal filter are shown in the photograph of Fig. 2; the transversal-filter arrangement is shown in Fig. 1.

An approximation to the transversal characteristic using a minimum of low-cost components is possible. Fig. 3 shows one implementation using resistors and one capacitor; the photograph of Fig. 4 shows the maximum-peaking transient response of this circuit. Other combinations can be tailored to individual requirements.

Luminance-Chrominance Tracking

Modern color-TV receiver controls are arranged so that the contrast potentiometer controls not only the amplitude of the luminance output, but also the color saturation. Both the CA3143 and CA3144 may be used in conjunction with either the CA3137E chroma demodulator or the CA3151 one-chip chroma system to accomplish this task. Fig. 5 shows the typical contrast control characteristic for both the CA3143 and the CA3144. The saturation controls on the two chroma circuits mentioned above also have the characteristic shown in Fig. 5. The two controls may, therefore, be ganged together in the manner of Fig. 6.

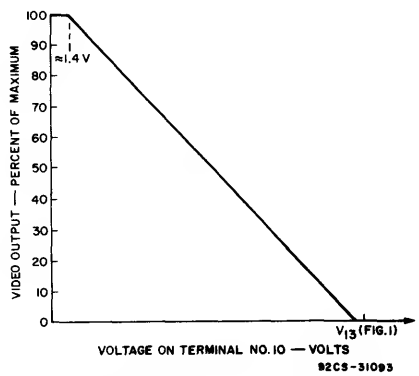


Fig. 5 - Contrast-control characteristic of CA3143 and CA3144.

The shunt regulator on terminal 13 of the luminance circuit can be used to provide a zener reference voltage for the chroma IC so that supply variations will not be a factor. A contrast-preset potentiometer provides for luminance set-up. The color control is a front-panel adjustment which can be set for customer perference, but it is also acted upon by the contrast control on the base of the p-n-p transistor.

References

1. RCA Solid State Data Sheets for TV Luminance Processors, CA3143 and CA3144.
2. J.P. Bingham, M.N. Norman, R.L. Shanley, B. Yorkanis, "A New Low-Level Luminance Processing System", IEEE Trans. on Consumer Electronics, Vol. CE-22 No. 2, pp. 135-142, May 1976.

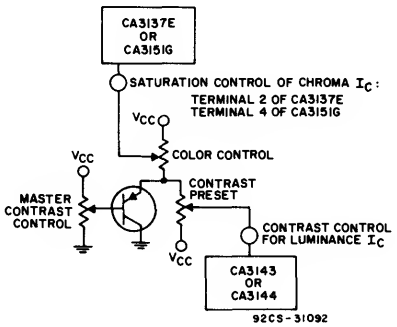


Fig. 6 - Tracking contrast and saturation controls using CA3143 and CA3144.

ICAN-6728

Application of the CA3134 Sound IF and Output Subsystem in Television Receivers

by George M. Harayda

In the CA3134, the sound if and audio output subsystems for color or black-and-white television receivers are combined in a single monolithic integrated circuit.[1] As shown in the block diagram, Fig. 1, the CA3134 includes a multistage if amplifier-limiter, an fm detector, an electronic attenuator, and an audio power amplifier. The power amplifier is designed to drive, primarily, an 8-, 16-, or 32-ohm speaker, although, if the designer chooses, it may be used to drive 4- or 10-ohm or other sized loads. The amplifier has a typical power output of 5 watts with a 16-ohm load and a V+ of 30 volts. The consolidation of the functions mentioned into an integrated circuit minimizes the number of components and reduces the area of the printed circuit board necessary for this portion of a television receiver. This consolidation also permits a reduction in manufacturers' component inventories and simplifies field servicing.

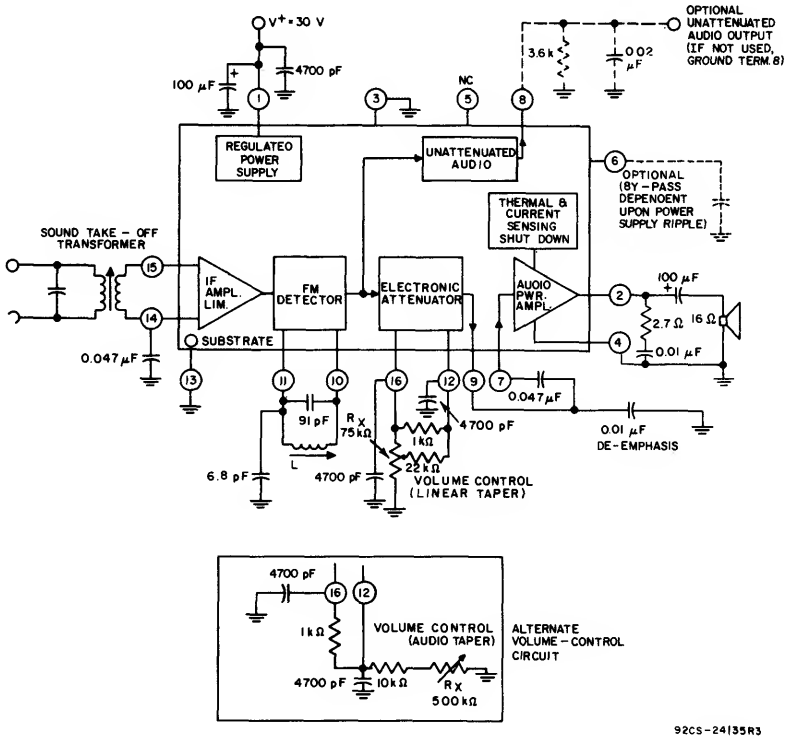


Fig. 1 - Block diagram of CA3134 in typical circuit application.

The incorporation of additional features in the CA3134 results in an improvement in performance when the circuit is compared to a system in which a type such as the CA3065 is used with a discrete or integrated circuit power amplifier. These additional features include a volume control with an improved taper, a provision for the optional use of an unattenuated audio output (fixed level unaffected by volume control position) (terminal 8), an additional power-supply-ripple bypass point (terminal 6), and a power amplifier with both current limiting and thermal-sensing shutdown protection.

Circuit Description

The CA3134 is designed primarily for use with either a single- or double- tuned sound take-off transformer (balanced input) to couple the sound if frequency (4.5 MHz) output from the video detector stage to the CA3134. This transformer serves both for impedance matching and as a bandwidth-limiting network to help reject unwanted frequencies such as intermodulation frequency products. Other undesired signals include residual am video information and sync information. Fig. 4 shows the overall circuit diagram for the CA3134.

Sound IF Amplifier-Limiter

The sound if stage amplifies the input signal until clipping eliminates am video and sync signals. In a typical TV system, the signal level available to the sound if amplifier-limiter is 35 mV rms. At this signal level, the input impedance components at terminals 14 and 15 of the CA3134 consist of a resistance, R_P, of approximately 25 kilohms in parallel with a capacitance, C_P, of approximately 3 pF. The sound if amplifier provides enough gain to bring the input signal level to an amplitude suitable for fm detection, but not so high as to cause PC layout or coupling problems, Fig. 2.

As shown in Fig. 4, the if amplifier consists of four stages of differential amplifiers, Q15-Q16, Q19-Q20, Q23-Q24, and Q27-Q28, using resistors R13, R16, R19, and R24 as constant-current sinks; each stage is followed by emitter followers, Q17, Q21, and Q25. Because the differential amplifier functions as a limiter, am signals are eliminated and the signal into Q30 consists of constant-amplitude, frequency-modulated square waves. These square waves are shaped into approximate sine waves by Q30 and its associated RC networks to assure proper operation of the fm detector. The signal output form R31 into the base of Q41 and to terminal 10 is a constant-amplitude fm sine wave.

FM Detector

The fm sine wave at terminal 10 consitutes the input signal to the differential peak detector stage. The extracted signal contains the audio information. The detector section is formed by the differential amplifier configuration comprising transistors Q31, Q32, Q35, Q36, Q40, and Q41. Transistors Q31 and Q41 are emitter followers that operate at approximately 0.3 mA and provide high impedance at each input of the detector (terminals 10 and 11). Transistors Q32 and Q40, which operate at approximately 10 microamperes, along with the 15-picofarad capacitors C3 and C4 and the external frequency-sensitive network on terminals 10 and 11, perform peak or envelope detection. As shown in Fig. 1, this frequency-sensitive network consists of a parallel LC network in series with a 6.8-pF capacitor. The signal voltage (from Q30) is applied across the entire network connected to terminal 10. The portion of the signal from Q30 that is across the external 6.8-pF capacitor is applied to terminal 11, and the resulting difference in these signals provides the basic S curve used in the recovery of the audio signal from the fm signal.

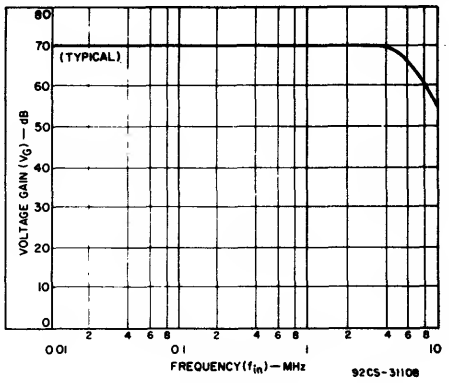


Fig. 2 - Voltage gain of if amplifier as a function of frequency.

An advantage of the differential peak detector is that it requires the alignment of only one single-tuned coil. This coil (L in Fig. 1) can be aligned by any one of the following methods (with an input terminated in 50 ohms, f_o = 4.5 MHz, f_m = 400 Hz, $\Delta f = \pm 25$ kHz, and a voltage at terminal 15 (V_{15}) $\simeq$ 100 mV rms):

1. Tune L for maximum recovered audio. To minimize thermal effects on alignment, the volume control should be adjusted so that the maximum recovered audio level at the load is limited to a low power level (approximately 0.1 watt or less).
2. Tune L for maximum recovered audio and fine tune for minimum distortion.
3. With no rf input signal, note the dc voltage at terminal 9. Then apply a 4.5-MHz cw signal and adjust the detector coil L until the dc voltage at terminal 9 is the same as the value noted.

After aligning the differential peak detector coil, align the input transformer by reducing the fm input signal level until the recovered audio level drops approximately 3 dB. Then tune the input transformer for a maximum recovered audio level while the input level of the if amplifier-limiter is below its limiting point. Fig. 3 shows the recovered audio, am rejection, and signal-to-noise ratio for the CA3134 as a function of rf input level.

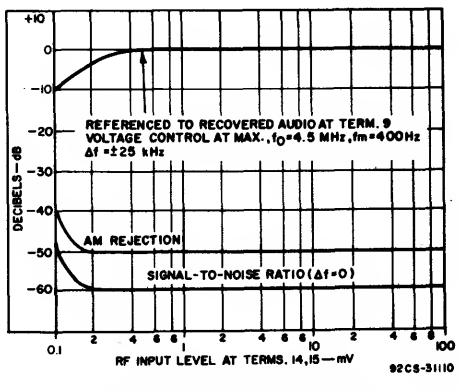


Fig. 3 - Recovered audio and signal-to-noise ratio as functions of rf input level.

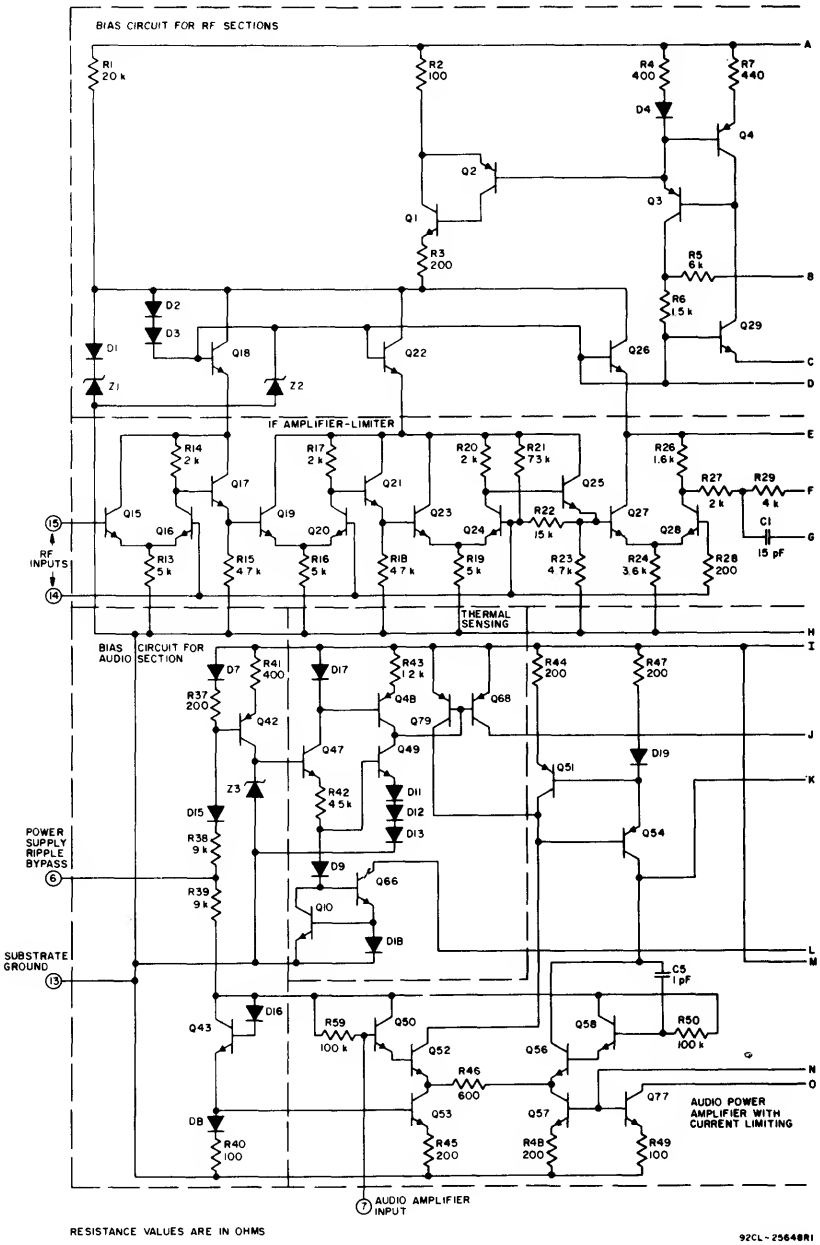


Fig. 4 – Schematic diagram of CA3134.

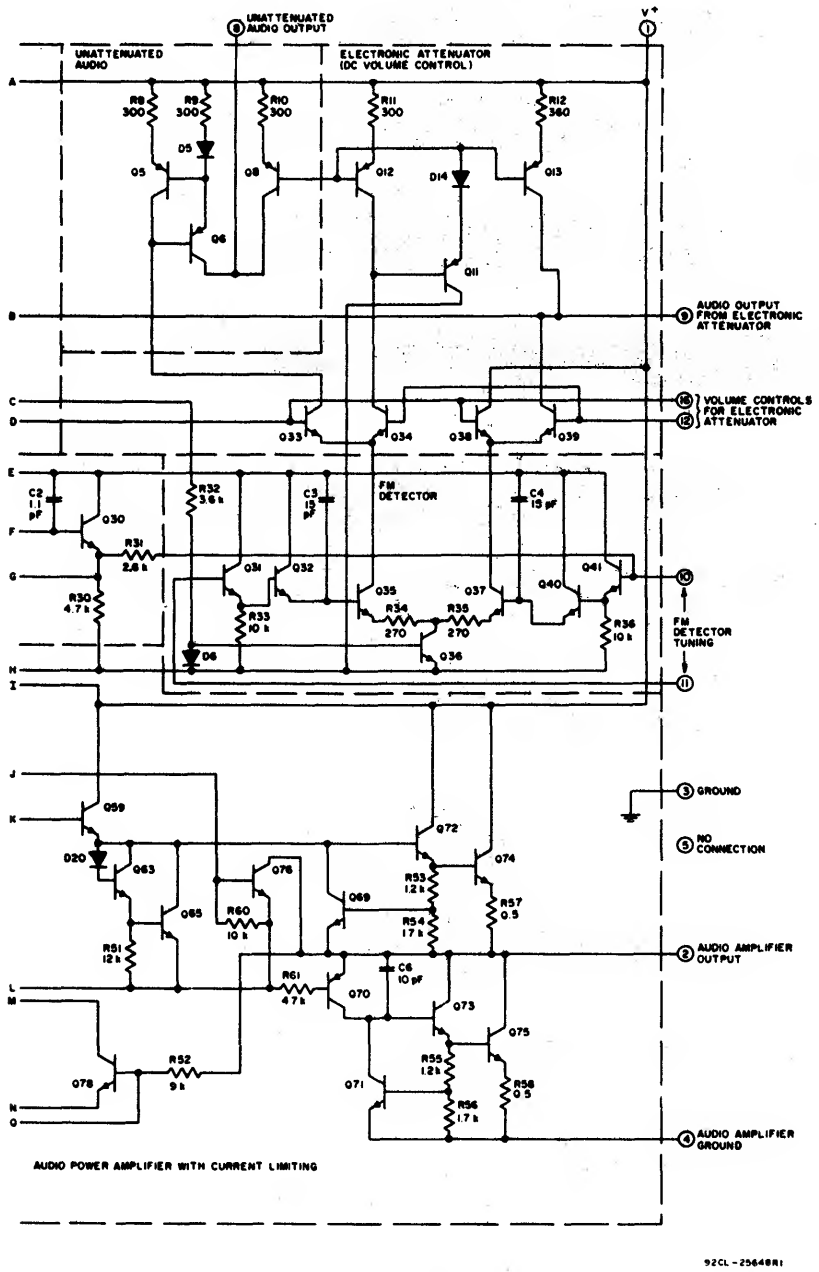


Fig. 4 – Schematic diagram of CA3134 (cont'd).

Volume Control and Electronic Attenuator

Control of the audio signal detected by the differential peak detector is accomplished by differential amplifiers Q33-Q34 and Q38-Q39. The volume is controlled when the bias levels of the differential amplifiers are changed by a current flowing through an external fixed resistor between terminals 12 and 16. The amount of current flowing through this external resistor (which determines the level of recovered audio) is controlled by the position of the variable resistance (volume control) relative to ground. The voltage reference at terminal 16 is established by internal zener diode Z2, approximately 6 volts. The maximum level of recovered audio, therefore, occurs when no currents other than the base currents for Q34 and Q39 are being drawn from the zener diode through the external resistor. When the volume control is adjusted for the minimum level of recovered audio, the current drawn from terminal 16 should be limited to less than 1 milliampere.

This method of controlling the recovered audio has a very predictable volume-control taper, which can be modified to suit the designer's preference by changing the external component values. In addition, it allows for either a one- or two-wire volume control. The one-wire volume control (Fig. 4, alternate volume-control circuit) requires only one wire from the printed circuit board to the external volume control, but requires that the value of the variable resistor be large (approximately 500 kilohms) and that the resistor have an audio taper to assure an acceptable change of audio output level with a linear change (rotation) of the volume-control. The two-wire volume control allows the use of a volume control having a lower value of resistance and a linear taper.

The output impedance of the electronic attenuator (terminal 9) is typically 7.5 kilohms (R5 + R6). A tone control may be inserted between the output of the electronic attenuator and the input of the audio power amplifier (terminal 7).

Unattenuated Audio Output

The operation of Q38 and Q39 is duplicated by Q33 and Q34 as the volume control is varied. The currents from Q33 and Q34 are combined by the current-mirror configuration produced by D5, Q5, Q6, and Q8, Q12. When an external resistor is placed between terminal 8 and ground, the current from this current-mirror configuration produces a recovered audio voltage at a fixed level independent of volume-control position. This output may be used to mute the sound in the event the broadcasting station loses its sound carrier or broadcast signal or to allow for the direct recording of the audio portion of a program.

Audio Power Amplifier

The audio power amplifier is a quasi-complementary class AB type with a typical voltage gain of 35dB. Internal feedback eliminates the need for external feedback components, especially costly electrolytic capacitors. The input impedance (at terminal 7) is typically 100 kilohms (R59). Fig. 5 shows the frequency response of the audio power amplifier and Fig. 6 its efficiency. Both current limiting and thermal shutdown protection are provided. Current limiting is accomplished by limiting the drive to the output transistors from the driver transistors Q72 and Q73. The limiting drive is determined by the feedback from R53, R54, and Q69 to Q72, and R55, R56, and Q71 to Q73. When the peak output current exceeds approximately 0.8 ampere, the voltage developed across the emitters of Q72 and Q73 will cause Q69 and Q71, respectively, to conduct, thereby limiting the drive to the output transistors Q74, Q75.

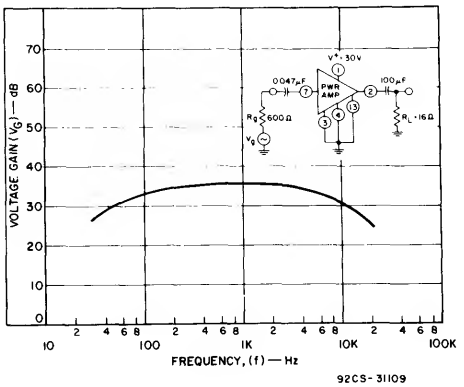


Fig. 5 - Voltage gain of audio power amplifier as a function of frequency.

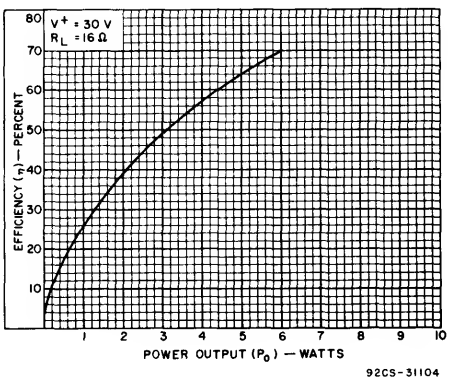


Fig. 6 - Efficiency of audio power amplifier as a function of output power.

When the chip temperature exceeds 150° C, the thermal-sensing portion of the CA3134 begins to shut down the power amplifier by removing the bias from the power amplifier driver stages. The temperature at which the thermal shutdown circuitry is activated is determined by the relative areas of D9, Q66, and D18 and those of Q49, D11, D12, and D13. When Q49 conducts, transistors Q79, Q68, and Q76 are in turn biased into conduction and remove bias from the amplifier driver stages. Because the drive is not removed symmetrically, the signal is distorted and gives an indication that the unit is in a fault condition.

Application

For the required power output from the CA3134 (Fig. 7), the speaker impedance must be such that its current drain will be both within the capability of the power supply and less than the current-limiting level of the CA3134. To decouple the CA3134 from the power supply and provide a means for preventing excessive drive to the speaker, a series resistor should be placed between the power supply and terminal 1. The value of this resistor depends upon the required power output level for the worst-case power supply voltage condition. This resistor also reduces the amount of power dissipated in the CA3134.

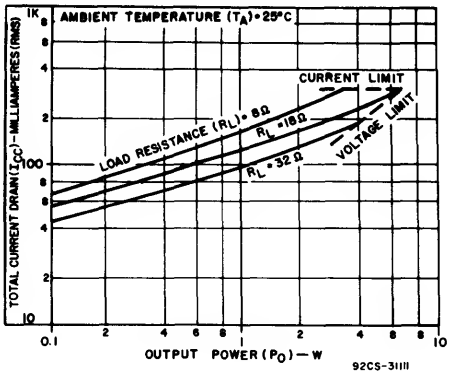


Fig. 7 - Total supply current as a function of output power.

The maximum power dissipation (Figs. 8, 9, 10, and 11) together with the anticipated maximum ambient temperature (Fig. 12) determines the required junction-to-ambient thermal resistance necessary to assure that the maximum chip temperature is lower than the rated junction temperature of 150°C. The overall thermal resistance can be lowered by careful PC board layout. As much of the copper area as possible should be exposed, and coil shields (input transformer and detector tuned circuit) should be used to help radiate heat.

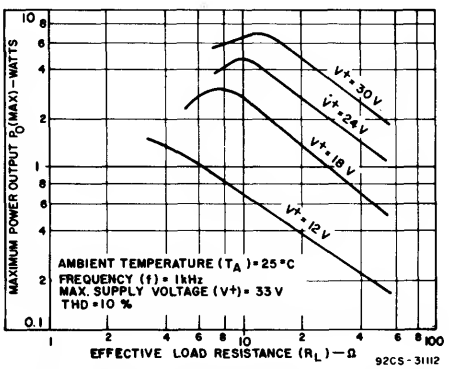


Fig. 8 - Maximum output power as a function of effective load resistance.

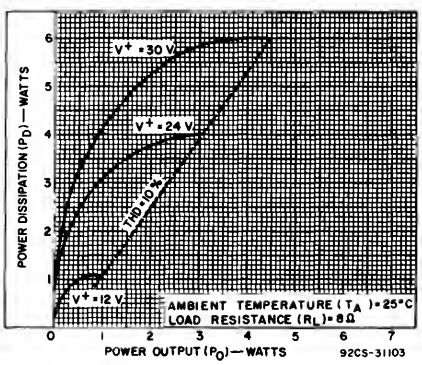


Fig. 9 - Power dissipation as a function of output power at RL = 8 ohms.

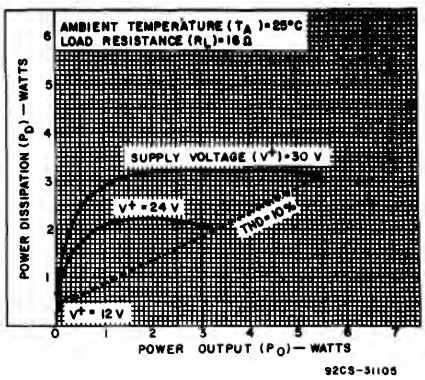


Fig. 10 - Power dissipation as a function of output power at RL = 16 ohms.

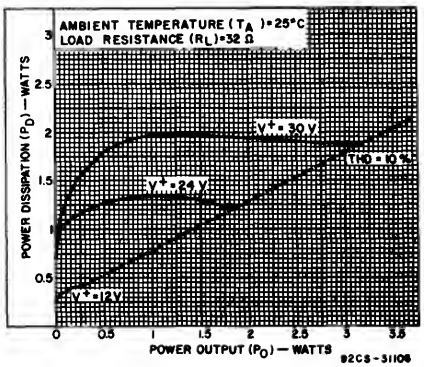


Fig. 11 - Power dissipation as a function of output power at RL = 32 ohms.

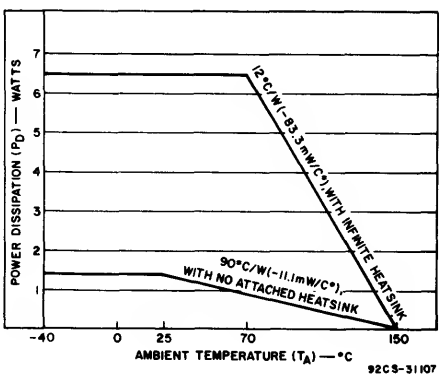


Fig. 12 - Maximum power dissipation as a function of ambient temperature.

Acknowledgment

The author is indebted to both Jack Craft for many helpful discussions and Wayne Austin for his suggestions in the preparation of this Note. The contributions of H. Chinery in the electrical characterization of the CA3134 and Ralph Thompson in the mechanical characterization of the package are acknowledged.

References

1. RCA Solid State Data Sheet for CA3134 types, "TV Sound IF and Audio Output Systems," File No. 1097.

Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

by T. J. Robe

The advent in recent years of very high-gain operational amplifiers operating in the 1/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

Considerations in Low-Noise Performance

Fig. 1 shows the schematic diagram of a noise model useful in a review of the considerations pertinent to optimizing low-noise performance in amplifier operation.

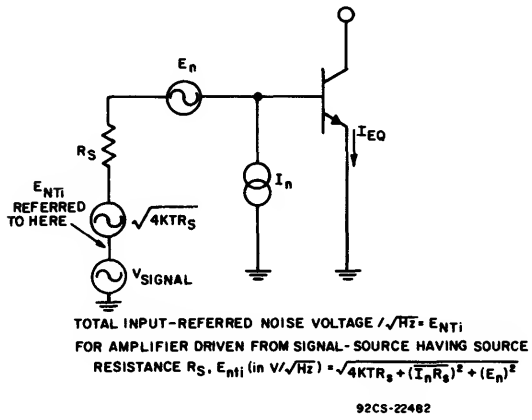


Fig. 1 - Sources of noise in the transistor-amplifier stage.

This model illustrates that consideration must be given to three major sources of noise:

1. Noise contributed by the "thermal-noise" voltage developed across the signal-source resistance, R_S. The magnitude of this voltage in $V/\sqrt{Hz}$ is approximately equal to $\sqrt{4KTR_S}$ for a 1-cycle bandwidth, where k is Boltzmann's constant (1.38×10^{-23} joule/°K), T is the temperature in degrees Kelvin, and R_S is the source resistance in ohms.
2. The noise voltage, E_n, resulting from the combined effects of shot noise due to emitter current flow and thermal noise due to transistor base resistance. These effects add in rms fashion to give a total E_n equal to $(E_{shot}^2 + 4KTrb'b)^{1/2}$. The shot-noise component, E_{shot}, is inversely proportional to the square root of I_{EQ}, and has a value

$$E_{shot} = \frac{14.2 \times 10^{-12}}{\sqrt{I_{EQ}}} \quad (V/Hz.)$$

3. The noise current, I_n, resulting from the combined "shot noise" generated by the flow of base current and the 1/f noise generated in the transistor. The magnitude of I_n is approximately proportional to $\sqrt{I_{IB}}$, where I_{IB} is the base current.

When each input terminal in a differential amplifier is driven from a source resistance (R_S), the total noise voltage (referred to the input, see Fig. 1) per unit bandwidth is given by:

$$E_{nti} \text{ (in } V/\sqrt{Hz}) = \sqrt{2KTR_S + 2(\overline{I_nR_S})^2 + (E_n)^2}$$

When amplifiers are driven from low source impedances, E_n is the predominant factor in noise contributions, whereas the effect of I_n predominates when input signals are supplied from high source impedances.

The traditional methods used to select very-low-noise devices for operational amplifiers involve the measurement of either spot or wideband (≈ 10 kHz) noise figures in the 1/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). The metering circuits cannot respond fast enough to measure the effects of burst-noise. Fig. 2a shows a photograph of typical burst-noise as a function of time for an operational amplifier having poor burst-noise characteristics. This photo illustrates burst noise which is characterized by random abrupt output voltage-level changes that persist for periods from approximately 1/2 millisecond to several seconds. Additionally, the random rate at which the bursts occur ranges from approximately several hundred per second to less than one per minute. Furthermore, these

rates are not necessarily repetitive and predictable. Consequently, the nature of burst-noise prevents its measurement by means of the standard averaging techniques. Instead, a technique to detect individual bursts must be used and a DUT must be under observation for a period in the order of 10 seconds to one minute. Fig. 2b shows a photo of the output of a virtually burst-noise-free operational amplifier, the RCA CA6741T.

Test Configuration

Some of the major questions relevant to the type of test required are:

1. What characteristics of the burst-noise should be detected?
2. What test-circuit configuration is most suitable to detect these characteristics?

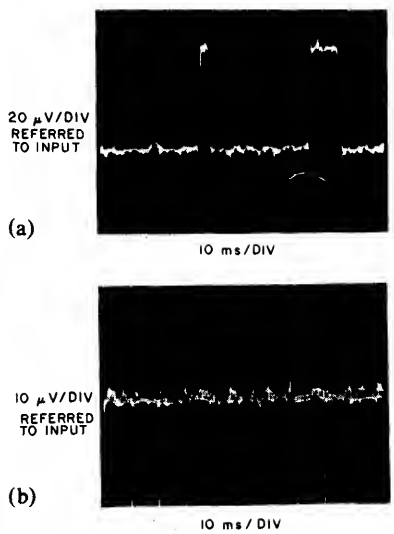


Fig. 2 - (a) Photo of output waveforms for amplifier with poor burst-noise characteristics; (b) photo of output waveform for the RCA-CA6741T.

3. What are the "Pass-Fail" criteria?

There are three major characteristics of the noise burst which have an impact on the suitability of a device from the standpoint of applications: burst amplitude, duration, and rate of occurrence. Of these, burst-amplitude and rate of occurrence are of primary interest to potential users of a particular device. Long duration bursts (of sufficient amplitude) seriously degrade the performance of dc amplifiers; however, suitable devices could be selected by the rejection of any unit which produced even one burst during some prescribed test period. Therefore, an absolute measurement of burst duration is not a prime necessity.

The rate of occurrence, on the other hand, as measured by the burst-count in a given test period could conceivably be considered as a variable of prime importance in the selection process. For instance, a burst-rate of 100 per second is clearly objectionable in almost any low-level low-frequency application, whereas the occurrence of only one low-amplitude burst in a one-minute period might be quite acceptable. Consequently, it is desirable to include flexibility in the testing system so that "Pass-Fail" criteria can be established on the basis of burst-noise count in some prescribed period of time. The test equipment described herein detects total noise (1/f noise plus burst noise) bursts with amplitudes above a preset threshold level during a given test period and allows acceptance or rejection on the basis of the number of noise voltage excursions beyond the threshold level, in the selected test period.

Another factor to be considered is the bandwidth of the test system. Excessive bandwidth allows the normal "white" noise of the terminating resistors and the DUT to obscure burst-noise occurrences and does not realistically simulate the low-frequency applications in which burst-noise is particularly objectionable. On the other hand, a test circuit having excessively narrow bandwidth prevents detection of the shorter-duration bursts ($\approx$ 1/2 ms) even if their amplitude is relatively high. A suitable compromise is chosen in which the system rise time permits a burst of "minimum" duration to reach essentially its full amplitude. Because the rise time and bandwidth of an amplifier are related by the equation:

$$BW \approx \frac{0.4}{t_r}$$

the minimum bandwidth to detect a 0.5 ms burst is approximately:

$$BW_{min} = \frac{0.4}{(0.5)(10^{-3})} = 0.8 \text{ kHz.}$$

Consequently, a 1 kHz bandwidth has been selected as a reasonable one for a burst-noise test system and, therefore, prescribes the need for a low-pass filter in the system.

The test requirements outlined above can be implemented with the following circuit elements shown in the block diagram of Fig. 3a. Fig. 3b shows the complete system schematic:

1. A fixed high-gain amplifier incorporating the DUT as the first stage to amplify the microvolt-level burst to an easily detectable level (this should be a burst noise-free unit);
2. A low-pass filter to limit the test bandwidth to approximately 1 kHz,
3. A comparator to produce a fast-rise high-level single-polarity output pulse whenever an input burst-noise pulse (of either polarity) exceeds a preset (but adjustable) threshold level;
4. A counter to tally the number of pulses emanating from the comparator during the test period: a single decade counter is adequate.

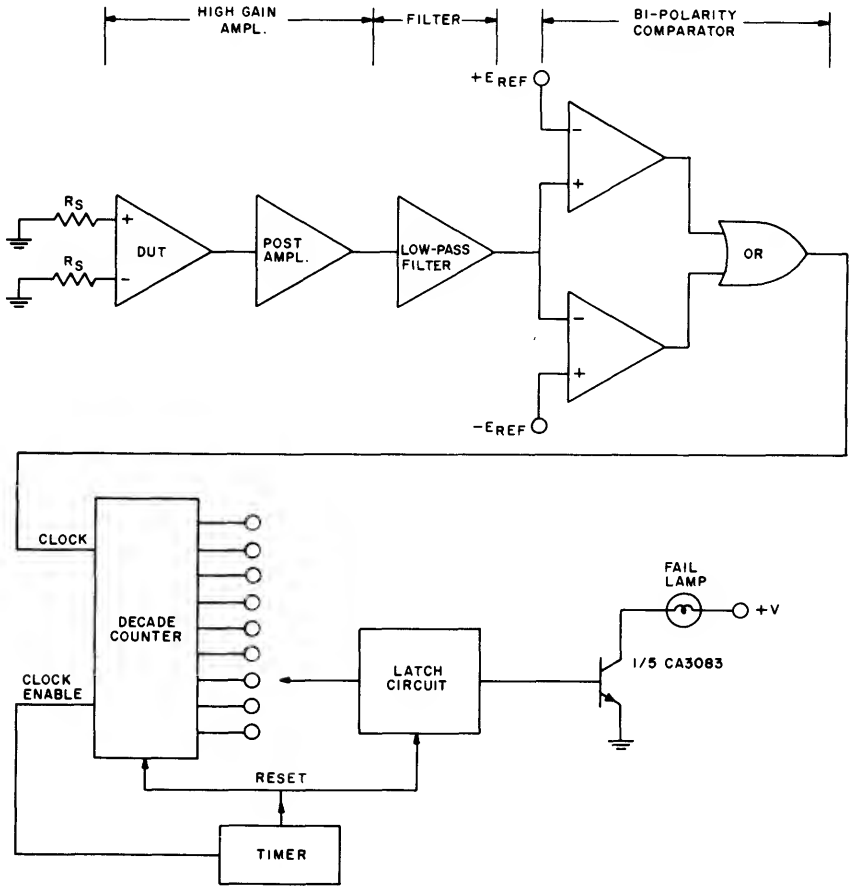


Fig. 3a - Block diagram of burst-noise test set-up.

5. A latch circuit which trips to the "latched" state when the count exceeds a preselected number (e.g. 1 to n). The latch circuit, if tripped, energizes an indicator lamp.
6. A timer to control the period over which the counter is enabled. It should incorporate the capability to reset both the counter and the latch circuit at the beginning of each test period.
7. Power supplies for the DUT and other auxiliary circuits.

Test Conditions

Some of the conditions which affect the burst-noise performance of the DUT include bias-level, source resistance (Rs), and ambient temperature (T_A).

The quiescent operating conditions in operational amplifiers are normally set by the magnitude of the positive and negative supplies. Many of the newer Op-Amp types, however, have bias-terminals into which fixed currents can be injected to set their performance characteristics. The RCA-CA3060, CA3080, and CA3080A Operational Transconductance Amplifiers (OTA's) and; the RCA-CA3078 and CA3078A Micropower Op-Amps are examples of such devices. For best low-frequency and burst-noise performance, these amplifiers should be operated at the lowest bias currents consistent with the gain-bandwidth requirements of the particular application.

In the test for burst noise, the source resistance (Rs) seen by the input terminals of the DUT, is a key test parameter. Burst noise causes effects which are equivalent to a spurious current-source at the device input and, therefore, burst-noise current generates an equivalent input noise-voltage in proportion to the magnitude of the source resistance through which it flows. Accordingly, to increase the sensitivity of the test system, it is desirable to use the highest source resistance consistent with the input offset-current of the DUT. For example, an Op-Amp which has 0.1 μA input offset current could realistically be tested with source-resistance in the order of 100KΩ (10 mV input offset), whereas a 1 MΩ source-resistance (100 mV input offset) could cause excessive offset in the output. For 741 type Op-Amps a 100kΩ resistance is recommended.

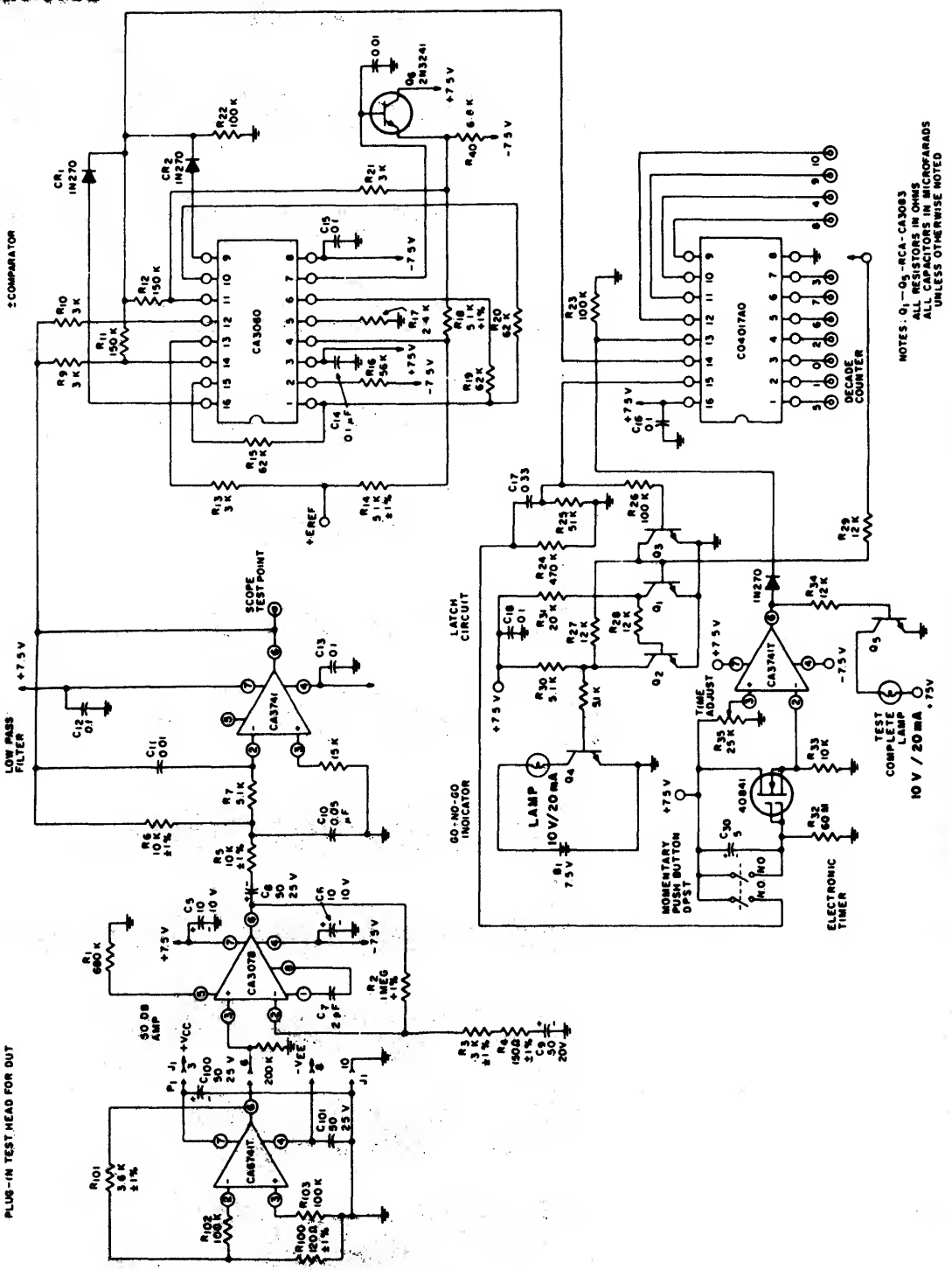


Fig. 3b - Complete schematic diagram for burst noise test-set.

Burst-noise generation in amplifiers is usually more pronounced at lower temperatures (particularly below 0°C). Consequently, consideration must be given to the temperature of the DUT in relation to the temperature range under which the device is expected to perform in a particular operation.

A test parameter of importance is the time duration of observation. Because the frequency of burst-noise occurrence is frequently less than once every few seconds, the minimum test period should be in the range of from 15 to 30 seconds.

Pass-Fail Criteria

A test system built to accommodate the test philosophy outlined above has the ability to reject or pass a DUT on the basis of two variables: burst-amplitude and the frequency of burst occurrence. The burst-amplitude which will trip the counter can be no lower than the background 1/f noise peaks of burst-free units, otherwise normal background noise will fail the DUT.

The background noise peaks depend on the source termination Rs, the wide band 1/f noise figure of the DUT, and the test system bandwidth. A good estimate of the normal background noise-peak levels can be computed from the definition of noise factor and an empirically determined noise-crest factor of approximately 6:1. The crest-factor is the ratio of the maximum peak-noise voltage to the RMS noise voltage. The noise factor is defined as the ratio of the total noise power at the amplifier output to the output-noise power due to the source resistors alone. In terms of the RMS noise voltages at the input terminals of the amplifier this is equivalent to:

$$\text{Noise Factor (F)} = \frac{E^2\text{input noise total}}{E^2\text{noise source resist}} = \frac{(E_{NTi})^2}{(E_{NRS})^2} \quad (1)$$

E_{NTi} is the total input noise-voltage, i.e., the sum of noise generated in the source termination resistance and noise generated by the DUT.

E_{NRs} is that part of E_{NTi} due to Rs alone.

$$\text{Therefore,} \quad E_{NTi} = (\sqrt{F})\,(E_{NRs}). \quad (2)$$

E_{NRs} can be computed by using the well known expression for "white-noise" generated across the terminals of a resistor (R):

$$E_{NR}(RMS) = \sqrt{4kTBR} \quad (3)$$

where k = Boltzmans Constant = 1.372×10^{-23} j/°K

T = Absolute Temperature in °K
B = Noise Bandwidth in Hz
R = Value of the resistor in ohms.

Thus, at a room temperature of 290°K

$$E_{NR}(RMS) = 1.28 \times 10^{-10} \sqrt{BR}$$

For example, a 100 kΩ resistor preceding a system with a bandwidth of 1 kHz will generate a noise-voltage of

$$(1.28 \times 10^{-10}) \quad (\sqrt{10^3 \cdot 10^5}) \quad = 1.28\ \mu V_{RMS}$$

Both inputs of an Op-Amp are usually terminated in Rs, hence it is necessary to combine the effects of both resistors to determine the effective E_{NRs} at the input of the DUT. Because the noise voltages from these two resistors are uncorrelated their voltages must be added vectorally rather than algebraically.

$$E_{NRs}\,(\text{effective}) = \sqrt{(E_{NR_{s1}})^2 + (E_{NR_{s2}})^2} \quad (4)$$

because $E_{NR_{s1}} = E_{NR_{s2}}$, when $R_{s1} = R_{s2}$

$$E_{NRs}\,(\text{effective} = (\sqrt{2})\ (E_{NRs})$$

and for 1 kHz bandwidth at 290°K

$$E_{NRs}\,(\text{effective}) = (\sqrt{2})\,(1.28\ \mu V) = 1.81\ \mu V_{RMS}.$$

If in this example, the DUT has a wideband 1/f noise figure of 4 dB (2.5:1 power ratio) the total RMS background noise-voltage at the input will be

$$E_{NTi} = (\sqrt{F})\ (E_{NRs})\ \text{(from eq.(2))}$$
$$= (\sqrt{2.5})\ (1.81) = 2.9\ \mu V_{RMS}$$

If a crest factor of 6:1 is assumed, the peaks of the background noise will be approximately (6) (2.9) = 17 μV peak. This voltage is the lower limit of the burst-amplitude rejection level. A reasonable threshold for burst detection and rejection might be 50-100% greater than this minimum value.

An alternate method used to set the burst-threshold limit involves a direct measurement (at the output of the high gain amplifier-filter combination) using a storage oscilloscope or a "true RMS" voltmeter. By this method the noise peak or RMS noise voltage of burst-free units is determined. This measurement provides a good practical check on the accuracy of the computation outlined above. Selection of the acceptable number of burst counts in the test period is arbitrary, but dependent on the type of application intended for the DUT. To be acceptable in some critical applications, the DUT may not generate even a single burst-pulse in a relatively long period of time.

Burst-Noise Test System Circuits

1. High gain Amplifier – Filter

Fig. 4 shows the schematic diagram of the high-gain amplifier-filter which provides a fixed gain of 80 dB with a 12 dB octave roll-off above 1 kHz. The gain-function is somewhat arbitrarily distributed between the DUT and

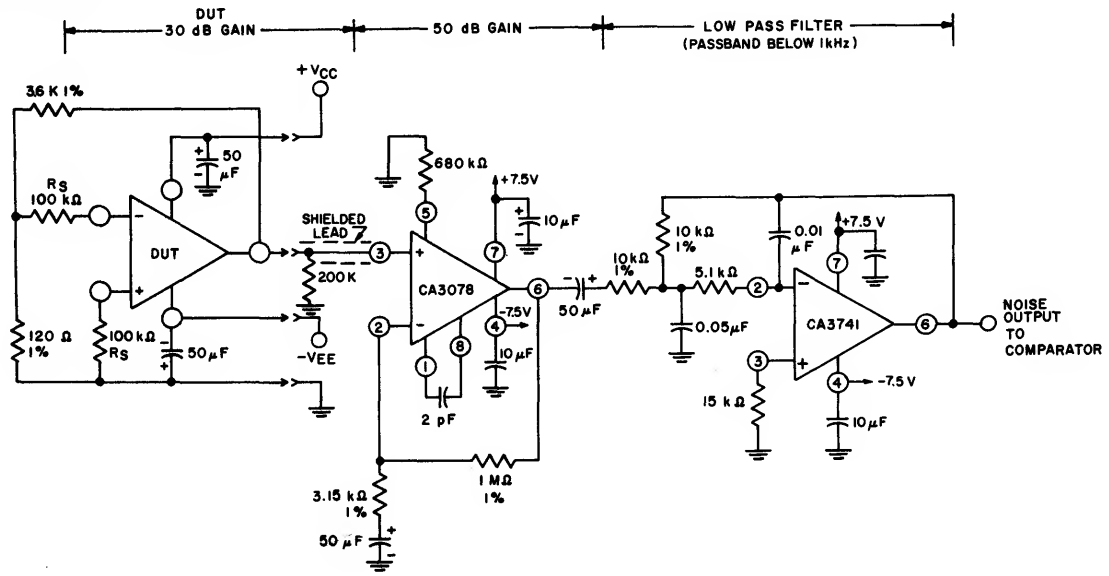


Fig. 4 – Schematic diagram of high-gain amplifier/filter.

post-amplifier: 30 dB and 50 dB respectively. This distribution is based on the need for sufficient gain in the DUT portion to eliminate significant noise-signal contributions from the second stage while simultaneously allowing adequate loop-gain in each stage to provide accurate gain-setting with precise external resistors. The first stage is shown as a plug-in module so that any type of DUT configuration having 30 dB gain can be tested.

The capacitive coupling employed provides a low frequency cutoff of about 1 Hz and eliminates the need for dc-offset zero-adjustments. The dc offset-voltage at the filter output is less than 5 mV which corresponds to less than 0.5 µV error when referred to the noise input (an 80 dB gain is assumed.) Several seconds must be allowed, however, for the DC operating point to stabilize after the power is applied to the DUT.

2. Bi-Polarity Comparator

Fig. 5 shows the schematic diagram for the threshold-detecting comparator. Because bursts of either polarity must be detected and converted to positive output pulses, two comparators are required: one having a positive-threshold reference and the other having a negative-threshold reference of equal magnitude. The RCA CA3060 triple OTA is convenient to use because a single package provides circuits for both comparators plus a reference inverter for the negative threshold reference. The positive feedback provided by the R_f and R_i connections produces a hysteresis effect with reference to the input switching threshold, (i.e., the comparator does not return to its quiescent state until the input noise signal drops well below the initial threshold trip-level). This feature is necessary to prevent multiple triggering by the background noise signals superimposed on top of the burst-noise pulse. By this means, multiple counting of a single burst-noise pulse is avoided.

The magnitude of the threshold reference voltage E_R determines the burst-level which trips the comparator. If a voltage gain of 80 dB is provided by the amplifiers, a 200 mV reference voltage will enable the circuit to be triggered when a burst-noise pulse (whose amplitude is equivalent to the level of 20 µV referred to the DUT input) is present.

3. Counter-Latch-Timer Control Circuits

The remaining circuits of the go-no-go burst-noise tester are shown in Fig. 6. The decade-counter is incorporated in single COS/MOS IC (RCA CD4017AE) which has clock, reset, and enable inputs, and an output terminal for each of ten count-positions (0 to 9). A carry-out signal is available if the use of more than a single decade is desired. The clock input-signal must be positive-going and have a magnitude of

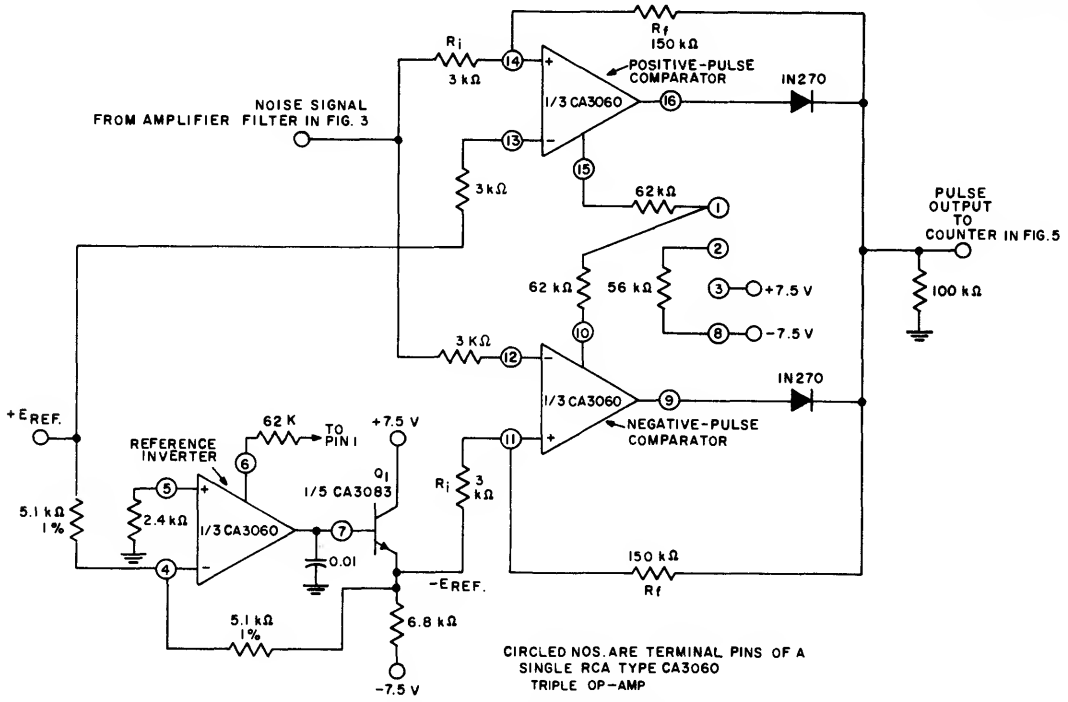


Fig. 5 - Schematic diagram of threshold-detecting comparator.

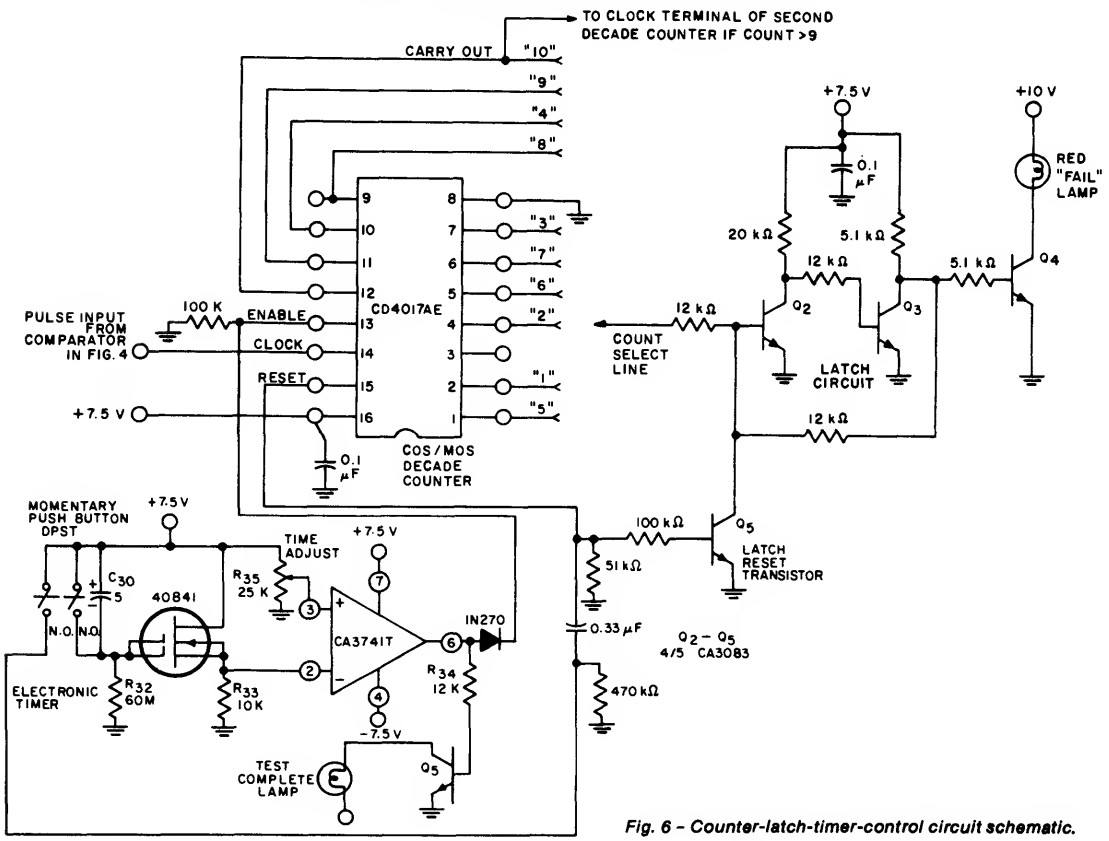


Fig. 6 - Counter-latch-timer-control circuit schematic.

at least 70% of the supply-voltage and rise-time equal to or less than 15 μs. The comparator shown in Fig. 5 provides an output signal which meets these requirements.

Selection of the reject count is made by a pin-jack connection of the latch-circuit input-lead to the appropriate output terminal of the counter. Whenever the selected count-position voltage goes "high" the latch-circuit is switched to the latched-state, and the fail-indicator lamp "on". The latch and lamp will remain "on" until the reset button of the electronic timer is switched to the "Timer On" position. This action provides a momentary reset signal ($\approx$ 20 ms) to both the latch and counter circuits and places a continuous enable voltage on the counter for the duration of the test period.

Spurious Noise Sources and Their Suppression

The very low voltage levels and the high source impedances normally used for burst testing render the system highly susceptable to external spurious noise sources. This problem is particularly serious if a test unit is going to be rejected for as little as one or two input burst-noise pulses exceeding 20-30 μV. The major sources of spurious noise encountered in the development of this test system were:

1. 60-Hz hum pickup,
2. power supply transients,
3. electromagnetic pick up of switching transients.

60-Hz hum is introduced by capacitive or inductive coupling or as power-supply ripple. Power-supply ripple is not normally a problem when testing operational amplifiers with regulated supplies, because the Op Amps generally have good power-supply rejection. This source of noise must be considered, however, when testing devices that do not have good inherent power-supply rejection. Capacitive or inductive coupling of hum can occur when 60-Hz line cord leads are within a few inches of the input terminals of the DUT. Precautions, such as proper lead dress and twisting of the 60-Hz leads, eliminate this problem.

Power-supply transients, as distinguished from power-supply ripple, can be of sufficient amplitude to introduce detectable noise pulses at the operational amplifier input. Such transients are produced when other equipment on the same ac line is switched on or off. A typical power-supply rejection ratio for an operational amplifier is 50 μV/V (i.e. a 1 volt transient on the power-supply is equivalent to a 50 μV noise pulse at the DUT input). This example demonstrates that the test system cannot tolerate power-supply transients greater than approximately 100 mV even when testing units with good power-supply rejection. Unless the power-supply is known to be free of such transients, a battery-operated system is recommended. Even when this system is battery-operated, "On-Off" switching of nearby equipment introduces detectable transients into the system. These problems are eliminated by placing the test circuitry in a completely shielded enclosure with a hinged top for easy access to the test unit. The external noise problem is best solved by use of a shielded enclosure and by use of a battery-operated power-supply contained within the enclosure. Fig. 7 shows a photo of the circuit board layouts of the test unit.

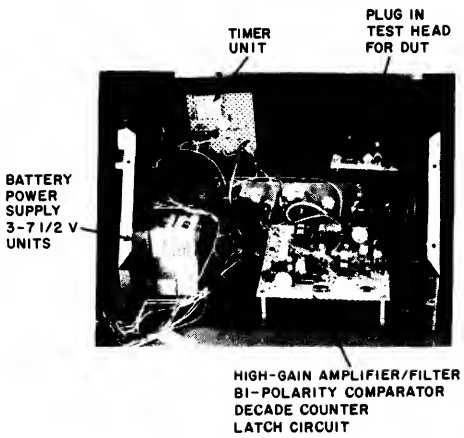


Fig. 7 - Photo of circuit-board layout.

A High Stability Sync-AGC and Horizontal-Vertical Countdown System for 525-Line Color Television Receiver Applications Using the RCA CA3154 and CA3157 Integrated Circuits

by W.M. Austin

The CA3154 Sync-AGC-Horizontal Oscillator and CA3157 Horizontal-Vertical Countdown integrated circuits are a functionally matched IC System for 525-line color TV applications. The CA3154 incorporates a horizontal-frequency oscillator which may be used with an adjustable LC circuit to preset the frequency or with a ceramic resonator with series-tuned characteristics. The CA3157 is functionally matched to the CA3154 and capitalizes on the low-cost high-stability circuit advantages of the horizontal oscillator through a divide-by-16 input counter that provides the 2-times horizontal frequency needed for the divide-by-525-line vertical countdown circuit. Both circuits are supplied in dual-in-line plastic packages (E suffix). Each chip is fabricated by means of modern IC process technology, which includes I^2L logic for the CA3157 switching circuit.

Fig. 1 shows a typical application of the system, a TV receiver circuit driving a vertical-deflection output circuit. Appendix I contains waveforms describing conditions at various IC terminals. Inputs to the system include the video input signal, the horizontal flyback-gating pulse, a + 12-volt power supply, and a + 130-volt power supply. The video input signal is nominally 3 to 4 volts peak-to-peak with sync-tip level referenced to the agc-system internal-bias reference of the CA3154. The horizontal pulse is nominally + 60 volts, as derived from the flyback transformer, and is used to gate the keyed agc circuits and to provide the sawtooth signal to the horizontal afc circuit. The + 12-volt power supply should be ± 5% regulated and well filtered to prevent cross-feed and false triggering problems. For good linearity, and to obtain tracking with brightness variation, the height-control circuit should be operated from a line-voltage source, which in this case is + 130 volts.

The signal outputs of the circuit shown in Fig. 1 are the vertical drive, horizontal predrive, vertical blanking, if agc, and rf or tuner agc. In addition to the video or pix-if outputs, both forward and reverse tuner agc are available. Feedback current sensing is used in the vertical-drive circuit to correct the drive waveform for linear yoke current.

CA3154 Functional Circuits

A block diagram of the CA3154 circuit functions is shown in Fig. 2. The video signal is derived from the video output of the pix-if detector or first video amplifier. The 4-volt dc agc level at the negative sync tip is designed to match the requirements of the synchronous-detector pix-if integrated circuit, CA3136.

The video signal is filtered for high-frequency roll-off at the input to terminal no. 1 to minimize video interference in the sync and agc circuits. A buffer amplifier drives the keyed agc and sync-separator functons. The sync separator strips the sync timing signal from the video signal and provides the composite sync output at terminal no. 3. The RC and diode circuit at terminal no. 2 maintains a uniform dc component in the sync separator drive signal supplied to the sync amplifier.

The agc gate is keyed by the horizontal pulse at terminal no. 16, but is also gated or strobed by the sync signal from the sync separator to provide noise immunity and to prevent the detected video from being sampled by the agc comparator when the system is out of sync. The gain-clamp feature of the CA3154 if agc amplifier is used to set the zero carrier gain of the pix-if by fixing the dc level at terminal no. 14 which, in turn, fixes the level at terminal no. 13. Under strong signal conditions, the agc delay is set by an adjustment at terminal no. 13, Then, as the signal increases, the tuner gain is reduced through the forward or reverse agc outputs from terminal nos. 11 and 12.

CA3154 Sync-Separator Circuit

The detailed schematic diagrams of the CA3154 are shown in Figs. 3(a), 3(b), and 3(c). The video input signal at terminal no. 1, Fig. 3(a), is applied to the base of the Q6 with an agc set-up level of 4 volts at the sync tip. The video signal is amplified 2 times with the aid of the current-mirror circuit of Q1 and Q2, the gain being determined by the resistor ratios of R4 and R1. The signal present at the emitter of Q3 is nominally 6 volts peak-to-peak, with positive-going sync tips of 1.5 volts. The sync separator function is performed by Q33. The emitter of Q33, connected to terminal no. 2, experiences a complex load. The charge and discharge time constants at terminal no. 2 are chosen so that Q33 is held in cut-off during the negative (picture) portion of the video signal, and charging current is present at the emitter of Q33 only during the positive sync-pulse portion of the video signal. The charging current in Q33 would normally be sufficient to saturate the collector of Q33 with the 15 kilohm resistive load, R38. However, saturation is prevented because the negative swing at the collector of Q33 is limited to 7.3 volts by a catcher circuit, Q38. The base of Q38 is nominally biased at 8 volts by the resistor bias string consisting of R42, R43, and R44. The emitter of Q38 is forward biased when the collector of Q33 drops below 7.3 volts. The gain of the sync separator is very low for the duration of the sync tips because the Q33 collector load is the emitter of Q38 instead of R38. Fig. 4 illustrates how the Q33 emitter-time-constant sync separator takes a slice of the sync timing signal between the pedestal and the sync tip and provides a clean pulse free of overshoots and low-frequency level changes.

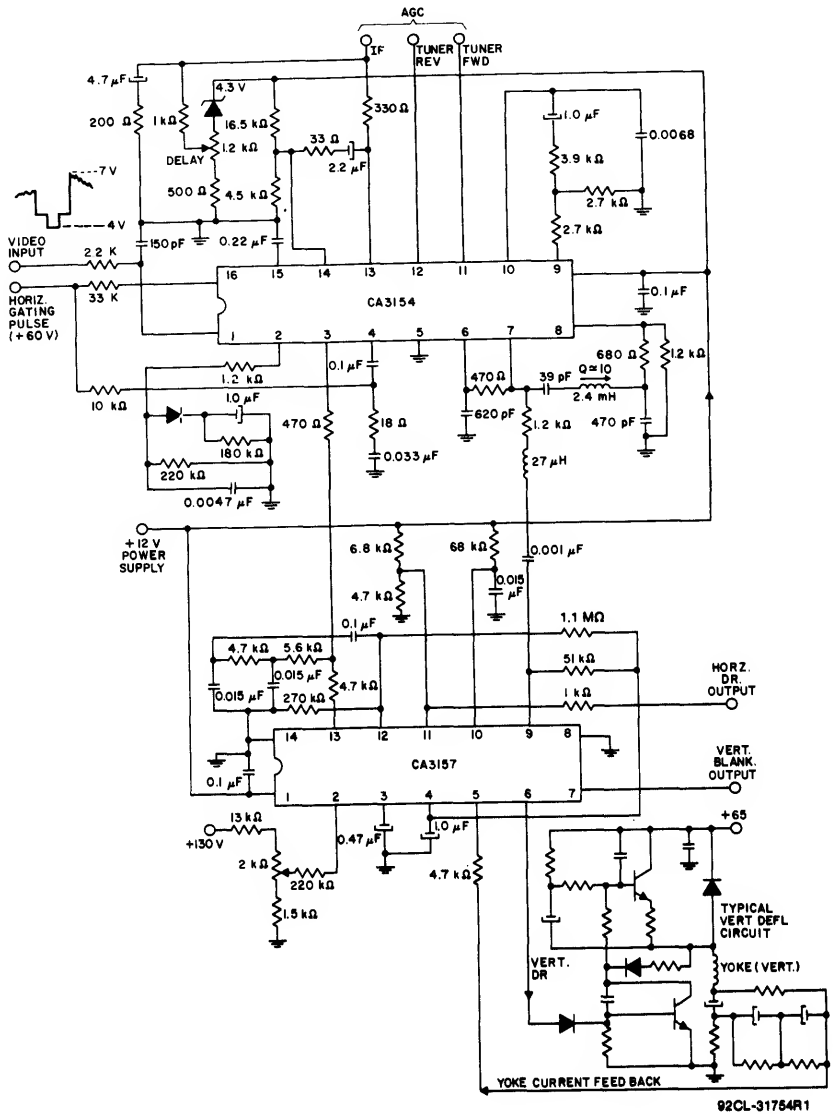


Fig. 1 - Typical CA3154/CA3157 horizontal and vertical countdown system.

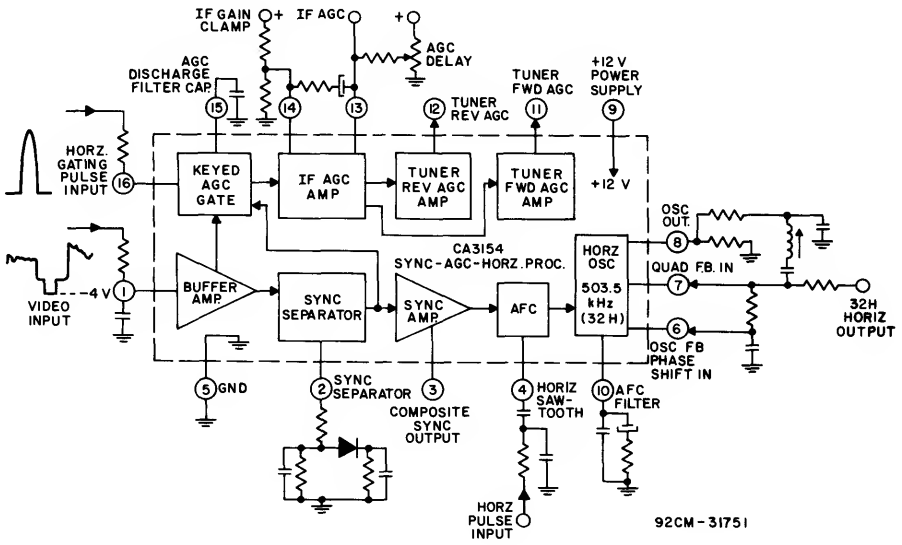


Fig. 2 - Functional block diagram of the CA3154 Sync-AGC-Horizontal Processor IC.

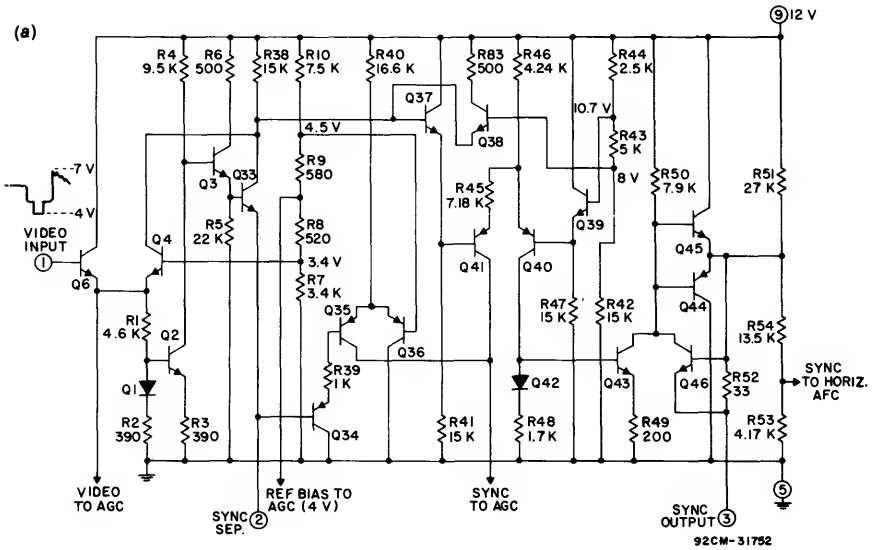


Fig. 3 - Circuit details of the CA3154: (a) sync separator, (b) agc circuit, (c) afc-oscillator circuit.

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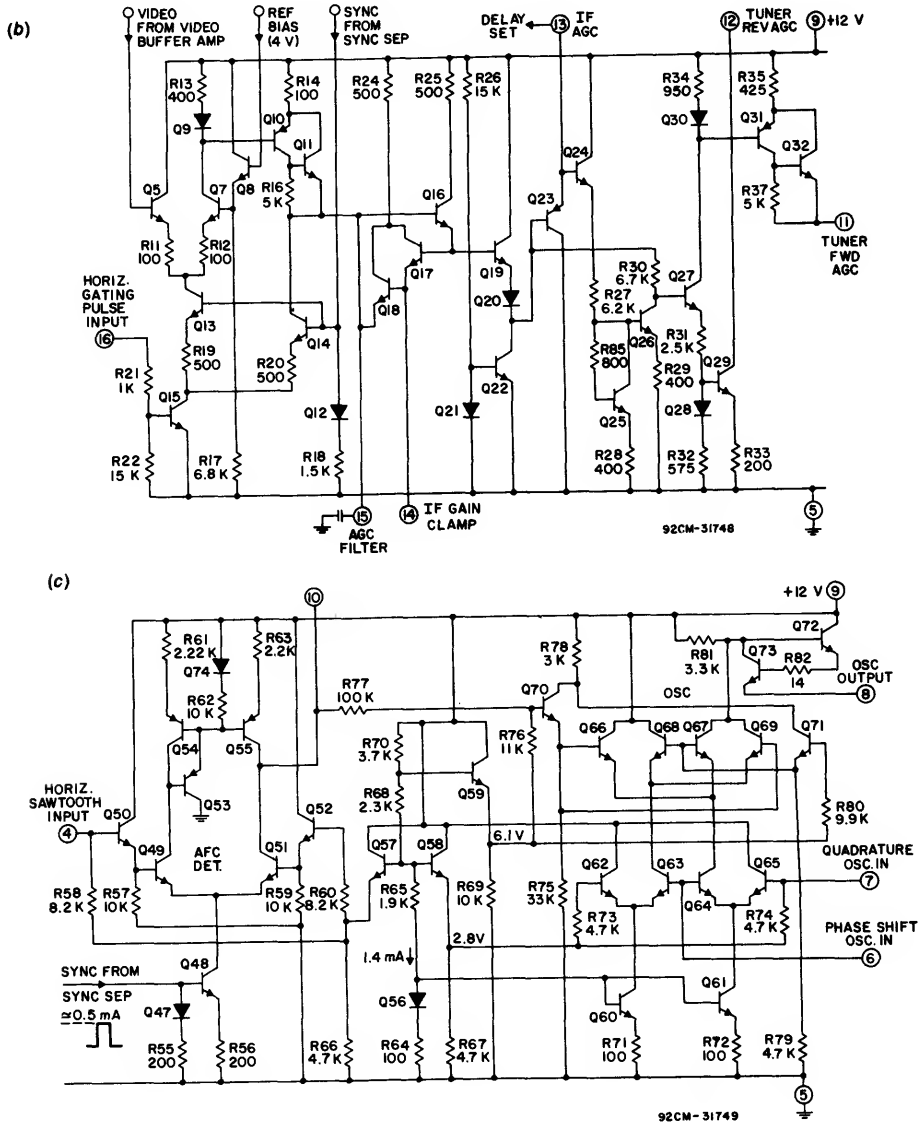

Fig. 3 - Circuit details of the CA3154: (a) sync separator, (b) agc circuit, (c) afc-oscillator circuit.

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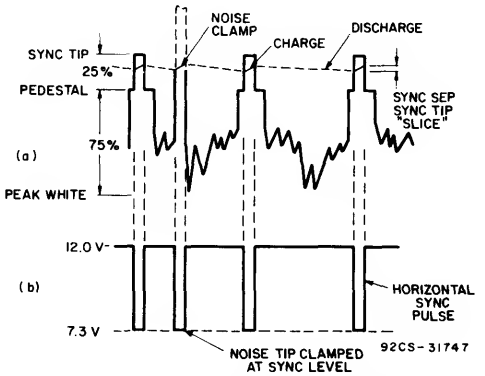

Fig. 4 - Emitter time constant and collector output signal at Q33 of the sync separator.

In the event that a noise pulse of momentary duration and less than 3.4 volts occurs at terminal no. 1, a catcher circuit, Q4, will protect the sync separator from excessive excursions at the Q33 sync-separator collector. The base of Q4 is biased to 3.4 volts by the bias-divider string consisting of R7, R8, R9, and R10. Should a noise pulse at terminal no. 1 cause a peak negative signal of less than 3.4 volts, Q4 will conduct and directly lower the voltage at the collector of Q33 to the 7.3-volt minimum allowed by the Q38 catcher. Q4 also conducts in the agc over-range condition, and turns on the sync strobe gate, which provides agc lock-out protection. For the wide-pulse conditions of vertical sync interval or impulse noise, the diode network at terminal no. 2 conducts and charges the longer time constant of 180 kilohms and 1 microfarad. When the longer charging pulse terminates, the diode remains reverse biased while the short time constant quickly recovers to prevent loss of horizontal sync pulses and equalizing pulses. The discharge period of the long time constant is matched to the needs of the vertical sync interval while, for best stability, the 220 kilohm, 0.0047 microfarad time constant is matched to the fast recovery needs of the horizontal sync.

When there is no signal, terminal no. 1 may go to 7 volts. To prevent total discharge of the terminal no. 2 RC time constant, and to minimize recharging transient delay time, Q34 and Q35 conduct when the base of Q34 drops below 3.8 volts. Under this condition, Q35 causes the agc gates Q13 and Q14 to turn on. The Q40, Q41 differential splits the sync phase so that the agc strobe gate and the sync amplifier are driven at the desired, opposite polarities. The base of Q40 is held at 10 volts by the reference bias from the emitter of Q39. Sync tips from the Q37 emitter drop to 6.6 volts and cause Q41 to conduct. Q41 then turns on agc gates Q13 and Q14, Fig. 3(b). Under the condition of negative sync-tip drive to the base of Q41, both Q40 and Q43 are turned off, giving rise to a positive sync pulse from Q45. The horizontal afc circuit is driven by Q45 through the R53, R54 divider. When sync is absent from the Q41 base, Q40 conducts and holds Q43 in saturation. In this condition, Q44 is pulled low and maintains terminal no. 3 at or near ground reference. Transistor Q46 limits excess current at terminal no. 3 by lowering the base drive to Q45 when the current is nominally -20 milliamperes at terminal no. 3.

CA3154 AGC Circuit

The video signal at terminal no. 1 is direct-coupled to the pix-if detector. The no-signal voltage at terminal no. 1 is typically 7 volts. Under increasing signal conditions, the negative-going sync tip is clamped by the agc reference circuit of the CA3154 at 4 volts. The agc differential-comparator circuit of Fig. 3(b) comprises Q5 and Q7, with Q6 and Q8 providing emitter-follower drive to each side of the agc comparator. The switching level of terminal no. 1 is referenced to the base of Q8, which is biased at 4 volts by the R7, R8, R9, R10 divider. Terminal no. 16, Fig. 3(b), is the horizontal-keying or flyback-pulse gate input terminal through which Q15 is turned on. When the horizontal oscillator is synchronized, the sync pulse gates Q13 and Q14 at the same time that the horizontal key pulse is applied to Q15.

Under these coincident-pulse conditions the sync tip at the base of Q6 is compared to the base reference voltage of Q8. When the sync tip reaches or drops below 4 volts, Q7 conducts and amplifies the sync tip. Current from the sync-amplifier transistor Q41 is fed to the mirror reference Q12 and R18. As a condition of coincidence, mirror output currents from Q13 and Q14 can flow only when Q15 is saturated by the keying pulse applied to terminal no. 16. While Q14 tends to discharge the agc filter capacitor at terminal no. 15, current through Q7 is mirrored in a 4-to-1 ratio by Q9 and the composite Q10 and Q11 circuit so that the filter capacitor at terminal no. 15 is charged. Stable conditions in the agc loop call for charge and discharge currents to provide a steady-state voltage at terminal no. 15. In this state, the currents in R14, R20, and R19 are equal. Therefore, the current in Q7 and R13 is 1/4 while the current in Q5 is 3/4 of that in R14. The ratio of the current in Q5 to that in Q7 is 3 to 1, which results in a differential voltage of approximately 80 millivolts at the bases of these transistors.

Because the base reference voltage at Q5, Q7, and Q8 is not accessible, the above information is noted to make the user aware of the voltage change effect at terminal no. 1 relative to the level of agc voltage at terminal no. 15. A calculation for base differential voltage with emitter degeneration may be made from the following equation:[2]

$$V_{b1} - V_{b2} = -\frac{KT}{q}\ln\left(\frac{I_o}{\alpha I_{C1}} - 1\right) + \left(2\frac{I_{C1}}{\alpha} - I_o\right)R_e$$

where the current Io is the total differential emitter current in Q5 and Q7, and is determined by the current in R45 and R46 when the emitter of Q41 is at 7.3 volts (which is approximately equal to the voltage at the emitter of Q38). The collector current of Q41 is nominally 0.41 milliamperes to Q12 and R18 while the mirrored current in the collectors of Q13 and Q14 is nominally 1 milliampere. The current Ic is 0.75 milliampere at the 3-to-1 condition of agc equilibrium. The current gain α is approximately 1 and KT/q is approximately 27 millivolts. The $V_{CE(sat)}$ of Q15 is approximately 0.1 volt. The emitter resistor value, Re, is 100 ohms, the value of emitter resistors R11 and R12. The base differential voltage for the 3-to-1 case is, then, in this instance:

$$V_{b1}(Q5) - V_{b2}(Q7) = 80\ mV$$

Fig. 5 further references changes at terminal no. 15 to the agc level by relating changes of the if and rf bias to the voltage level on that terminal. Note that in forward-type agc systems, an increased signal into the tuner results in an increased agc voltage. The increased agc voltage decreases the gain of the amplifier by reducing its collector-to-emitter voltage through an increased base-to-emitter potential. In reverse-type agc systems, an increased signal into the tuner results in decreased agc voltage. The decreased voltage reduces the transconductance of the amplifier, thus reducing its gain.

The forward-if agc maximum-gain clamp voltage, set by the divider on terminal no. 14, determines the if gain reduction indicated as point A in Fig. 5. The agc-delay turn-over setting, made by adjusting the potentiometer at terminal no. 13, initiates the tuner gain reduction illustrated as point B in Fig. 5. Because terminal no. 13 is driven by a p-n-p transistor, it is possible to restrict the maximum voltage at that point by a clamp; this maximum agc-delay turn-over voltage is approximately 5.5 volts. The delay turn-over voltage determines the point of transfer of the agc control from the if to the rf amplifiers to assure gain reduction in the tuner so that drive to the if is maximized without the risk of overload at the input.

As shown in Fig. 3(b), the voltage derived from the keyed-agc gate, as measured at terminal no. 15, is applied to the base of Q16, which is a drive point for the agc if and rf amplifiers. Under weak signal conditions, Q14 tends to discharge the agc filter capacitor located at terminal no. 15. The minimum voltage at terminal no. 15 is clamped by the divider bias at terminal no. 14; the bias holds the voltage at terminal no. 15 to one emitter-base voltage drop (one V_{be}) of Q18 below the voltage at terminal no. 14. The voltage between terminals 13 and 15 drops one V_{be} each through the base-emitter junctions of Q16, Q19, and Q20, but increases one V_{be} through the Q23 p-n-p base-emitter junction for a total shift of $-2V_{be}$ or approximately -1.4 volts. Therefore, the divider level at terminal no. 14, less 2.1 volts, is the initial gain reduction indicated as point A in Fig. 5. As the agc voltage increases at terminal no. 15, Q18 becomes reverse biased, and the voltage at terminal no. 14 tracks with the voltage change at terminal no. 13 because both terminals experience a net voltage drop of $2V_{be}$ referenced to terminal no. 15.

In the if gain-reduction range from point A to point B, Q23 drives the Q24 emitter-follower. The current from the Q24 emitter is mirrored in the R27, Q25, Q26, R30 circuit. When the voltage at terminal no. 13 reaches the value set by the delay potentiometer, Q23 approaches the reverse bias state, which limits further increase in the current drive to the R27, Q25 side of the mirror. Since the mirror sink current for Q26 through R30 to the base of Q23 is returned through Q20 and Q19, increased voltage at the base of Q23 will cause the collector voltage of Q26 to increase. This increase, in turn, initiates the drive voltage to the base of Q27 required for the vhf and uhf tuner gain reduction. Forward tuner agc is derived from the collector of Q27 and passes through Q31 and Q32 to terminal no. 11. Reverse tuner-agc bias is available at terminal no. 12 from Q29 and the emitter of Q27. The current capabilities at terminals 11 and 12 are 1 and 2 milliamperes, respectively.

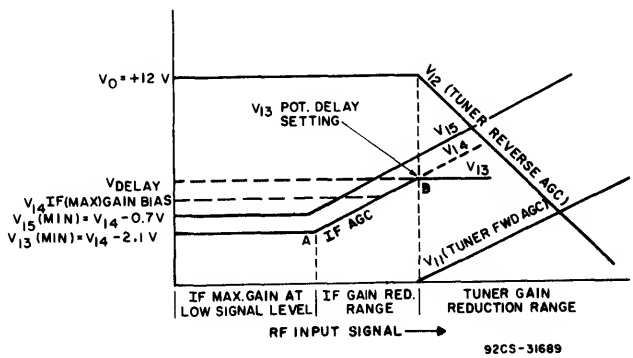

Fig. 5 - Typical operation of the agc circuits of the CA3154.

CA3154 Horizontal-AFC and Oscillator Circuit

Fig. 3(c) shows the combined horizontal-afc and oscillator circuit. The circuit, comprising Q48 through Q55, is the automatic frequency control (afc) detector. The afc detector inputs are horizontal sawtooth inputs at terminal no. 4 and the internally coupled, positive, sync-pulse input to the base of Q48. The afc output is internally coupled from the collector of Q51 to the base of Q70. At terminal no. 10 a double-time-constant circuit is used to filter horizontal pulses and noise interference and also to provide antihunt correction. Error current from the afc detector is converted to the voltage at R76 and applied to Q70 for comparison with the dc reference to Q71. The frequency of the horizontal oscillator is determined by the doubly balanced differential-phase corrections of Q66, Q67, Q68 and Q69.

The afc detector is gated into conduction only when the sync pulse is present in the Q47 and Q48 current mirror. The positive key pulse is shaped by an integrating network into a sawtooth voltage before it is applied to terminal no. 4 Fig. 6 shows the relative coincidence of the sync pulse and sawtooth signals applied to the afc circuit. When the horizontal oscillator is phase locked, detector comparison is made only during the retrace interval. Detector output current is mirrored through Q54, Q53, and Q55 and flows in equal positive and negative duty cycles from Q51 and Q55 when the sync and sawtooth are at zero phase error. When there is a frequency shift in the horizontal oscillator, a phase error occurs which results in a net unbalanced in the duty cycle of the current at the afc detector output. A correction signal is generated in the process of the current-to-voltage conversion in R76, and the oscillator frequency is corrected to reduce the phase error. If the phase error resulting from oscillator frequency drift is excessive, detector gating will occur outside of the range of the positive slope of the sawtooth with a resultant loss of horizontal lock. A 2.8-volt dc reference bias for the horizontal sawtooth is derived from the R64, R65, R68, R70 divider and is coupled to the base of Q52 through Q57 and R60. The same divider string also provides reference bias to the horizontal oscillator and the phase-correction circuit.

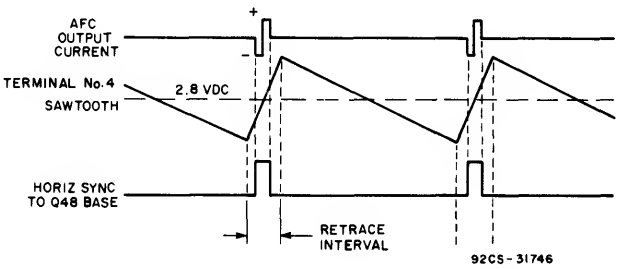

Fig. 6 - AFC signals and time-coincidence conditions.

Fig. 7 is a simplified schematic diagram of the horizontal-oscillator portion of the CA3154. The figure also shows the relative signal phases at various points in the circuit. If the input phase reference at terminal no. 7 is designated as Φ1 and the lagging phase at terminal no. 6 as Φ2, the phase at the collector of Q64 is noninverted Φ1 added to inverted Φ2 or Φ1 — Φ2. The signal phase at the collector of Q63 is —Φ2. The doubly balanced differential summing amplifier comprising Q66, Q67, Q68, and Q69 adds the Φ2 and Φ1 —Φ2 phase components in correct proportions to produce a zero phase shift in the oscillator at the reference horizontal frequency. With a summing-amplifier control factor of $0<k<1$ assigned, the output of the oscillator at terminal no. 8 is proportioned by the value of this control factor and the gain, A, of the differential amplifiers Q62, Q63, Q64 and Q65 in cascode with the summing-amplifier collector load, R81. The oscillator gain, given in terms of phase shift for the oscillator phase control circuit, is:

$$e_o/e_{in} \simeq A[k(-\Phi 2) + (1-k)(\Phi 1 - \Phi 2)]$$

The factor $[k(-\Phi 2)+(1-k)(\Phi 1-\Phi 2)]$ for values of $\Phi 1 = 1 + j0$ and $\Phi 2 = +0.5 - j0.5$ becomes:

$0 + j1.0$ when $k = 0.5$

$-0.5 + j0.5$ when $k = 1.0$

and $+0.5 + j0.5$ when $k = 0$

The conditions that determine k are established by the relative level of the afc-detector correction voltage. This voltage is approximately centered under a balanced condition of +90° shift; a phase shift of 90° lag is used in the external feedback circuit.

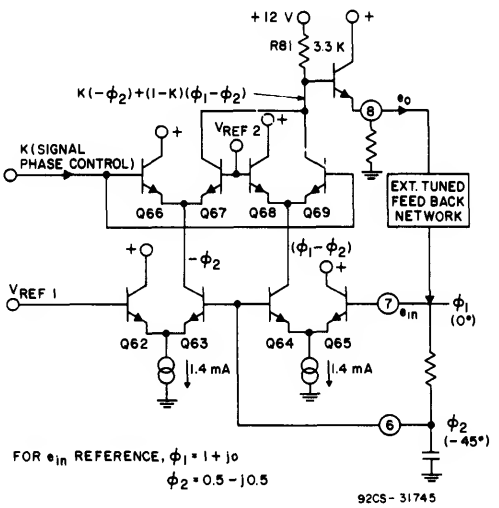

Fig. 7 - Simplified circuit of the horizontal-oscillator portion of the CA3154.

The product of the external loop attenuation and the internal gain provides the transfer function of the oscillator loop under all conditions. At the given free-running frequency for zero phase around the loop, an adequate margin of gain is needed to assure oscillation under all

conditions of operation. The gain of the internal loop is determined by the differential amplifiers Q62, Q63 and Q64, Q65. The typical differential-amplifier emitter-bias current of 1.4 milliamperes is set by the current through Q56 and R64. This current biases Q60 and Q61 to the same level by means of the current-mirror circuit design. The amplifier gain is approximately the product of the transconductance, gm, and the load resistance, R_L. For the differential amplifer,

$$gm = \alpha \frac{I_o}{4KT/q} \text{ ; therefore,}$$

with the 3.3-kilohm load resistor involved in this case, amplifier gain is approximately 40. Alpha is assumed to be 1.0; I_o, 1.4 milliamperes; and KT/q, 28 millivolts. Fig. 8 is a plot of the oscillator phase as a function of terminal no. 10 control, with current injection, for the component values shown, at a horizontal frequency of 503.5 kHz. Fig. 9 characterizes the frequency capability of the loop when driven from terminal no. 6 and 7.

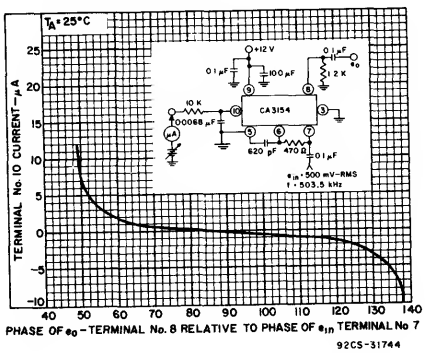

Fig. 8 - Output phase of the CA3154 oscillator (terminal no. 8) referenced to terminal no. 7 for a frequency of 32 kHz.

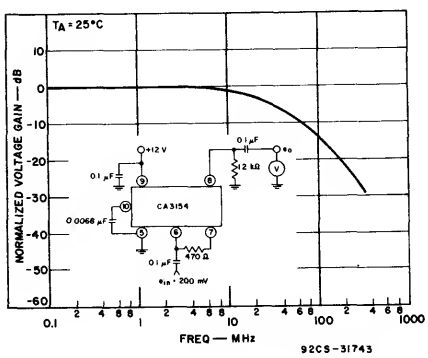

Fig. 9 - Frequency response of the CA3154 with high-level drive.

The oscillator of the CA3154, with the components as shown in Fig. 1, has a frequency shift of ±45° at 503.5 kHz. The frequency shift is a function of the external circuit tuning and the Q of the adjustable coil. Where the 2.4 millihenry coil has a Q of 10, the frequency may be varied within ±50 kHz. The pull-in range is typically ±25 kHz.

While the typical circuit of Fig. 1 shows the operation of the CA3154 at 503.5 kHz, the purpose of its use with the CA3157 is to achieve high stability at low cost. The CA3157 horizontal-vertical countdown circuit requires the 503.5 kHz frequency for its counter circuits so that it can provide proper horizontal and vertical frequencies of 15.734 kHz and 59.94 Hz, respectively. However, the frequency of operation of the CA3154 is not restricted to 32 times the horizontal frequency, and the CA3154 may be used over any desired range within the gain capability of the amplifier. While the design of the afc circuit suggests the primary use of the CA3154 as a line oscillator, its application may be considered in CATV, subscription TV processors, monitors, and sync-reinsertion circuits.

CA3157 H-V Countdown Circuits

The full logic-circuit diagram for the CA3157 is shown in Fig. 10; a functional block diagram is shown in Fig. 11. The following description is limited to the block diagram and the function of the CA3157 in the 525-line color-TV receiver application. An understanding of the functional block diagram requires a fundamental knowledge of the M/NTSC or M/PAL television standards. Reference to the FCC standards or CCIR documents for specific sync signal timing information is recommended for an understanding of the significance of the 525 count. Appendix II contains timing signals for the M-NTSC system.

The advantages[3] of a countdown system and, in particular, those of the CA3157 are: vertical hold-control elimination, improved performance during noise interference conditions with freedom from jitter under poor signal conditions, good interlace with precise digital clocking.

The CA3157 operates from a + 12-volt power supply; a ratio-regulator circuit provides +5.2 volts for the on-chip circuitry. A + 130-volt power supply is used as an optional means of providing a linear current control at terminal no. 2 for the height adjustment. The signal inputs to the circuit are the integrated vertical sync (IV), terminal no. 12; composite sync, terminal no. 13; and the 32-times horizontal frequency, terminal no. 9. Output signals include the horizontal predrive at terminal no. 11 to the horizontal-deflection flyback system, vertical drive at terminal no. 6 to the vertical-deflection circuit, and a vertical blanking pulse at terminal no. 7 used for luminance blanking during the vertical retrace interval. A yoke-current feedback terminal, no. 5, and a mode-select switch for the forced asynchronous (nonstandard signal) option, terminal no. 8, are also provided. The 2-times horizontal frequency (2H) derived from the divide-by-16 counter is internally coupled to the 525-count binary counter. The CA3157 requires a 32-times horizontal frequency to clock the counter circuits properly. While there is flexibility of choice of a multiple of the horizontal frequency for the CA3154, it has been specifically designed to meet the 32-times or 503.5-kHz frequency requirement of the CA3157.

The 503.5-kHz signal frequency from the CA3154 to terminal no. 9 of the CA3157 is divided by 16 in a four-stage ripple counter. The signal is then passed through a divide-by-2 counter, which drives a buffer amplifier, and transmitted to terminal no. 11 where it represents the proper horizontal predrive signal for the horizontal-deflection circuit. The horizontal flyback-transformer output is used to derive a sawtooth signal for the CA3154 afc circuit; this circuit compares the sawtooth signal to the horizontal sync and provides the correction signal required to phase-lock the 503.5-kHz oscillator.

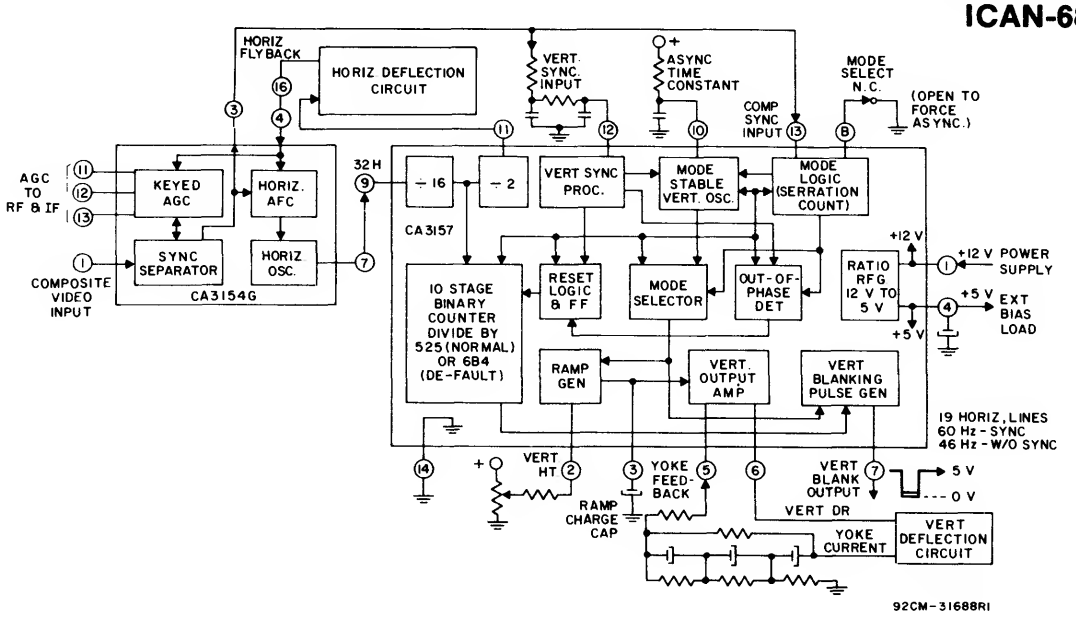

Fig. 10 - Functional block diagram of the CA3157 Horizontal-Vertical Countdown IC.

The 2-times horizontal frequency clocks the 525 binary counter, which has outputs to the mode selector, mode logic, vertical blanking-pulse generator, monostable (asynchronous) vertical oscillator, out-of-phase detector, and the reset flip-flop for the 525 counter. The ramp generator will operate from either the binary counter pulse or the monostable oscillator, depending on the mode logic and mode selector; the mode selector automatically switches to synchronous for standard and to asynchronous for nonstandard signal conditions. The blanking-pulse generator processes the output of the 10-stage binary counter and produces as output a pulse of 38-count (19-line) width. The IVS input at terminal no. 12 is processed in a comparator and logic switching circuit to provide a jitter-free, reconsituted, vertical sync signal with excellent noise immunity. The reconstituted vertical sync (RV) is directed to the out-of-phase detector, which compares the 525-line counter pulse to the RV pulse. If coincidence detection fails seven consecutive times, the out-of-phase detector will signal the reset flip-flop to reset the 525 counter.

The monostable multivibrator operates when triggered by the RV pulse or a 684 default count from the 10-stage binary counter, and provides vertical drive when the mode-recognition circuit switches to asynchronous operation. Mode recognition is based on 9 serration counts in 6 lines following the 525 count. If seven consecutive fields fail to yield a 9 serration count in the 6-line window, the mode circuit will switch to asynchronous operation. Only one field of 9 serration counts is required to restore synchronous operation.

The need for an automatic switching circuit to control operation in the sychronous or asynchronous mode is the result of nonstandard practices in the industry. Generators that produce standard NTSC sync are still expensive, from the consumer-cost viewpoint, and, since it is evident that the array of consumer instruments intended to interface to the TV receiver, video games, service signal generators, video-tape and disc systems, and home cameras, will continue to exist and probably multiply, the control of asynchronous signals, including those from CATV sources, must be planned for. Because a signal may be nonstandard and still produce the equivalent of a 9-digit serration signal to be counted at the composite sync input to terminal no. 13, forced asynchronous operation may be the only acceptable choice in adapting user equipment to the CA3157 system. To meet this potential problem, access to control of the mode-recognition circuit has been provided at terminal no. 8. Automatic selection of mode occurs when terminal no. 8, which is normally grounded, is open circuited; the CA3157 is then forced to operate in the asynchronous mode. In this mode, the monostable circuit functions as a normal oscillator with an RC time constant available at terminal no. 10 and as a comparator circuit forming the vertical drive pulse.

CA3157 Logic Circuits

The following descriptions of the functional sections of the CA3157 are based on positive logic with clock control on the 0 to 1 transition. The binary states referenced in Appendix III are those that enable the controlling gates and inverters. Enable, reset, and preset terminals are controlled by the 1 logic state.

The irregulator grouping of linear circuits with logic circuits shown in Fig. 11 results from the use of the I^2L (integrated injection logic) fabrication process, which permits both linear and digital functions to exist on the same chip. Where conventional I^2L logic is used, only the logic symbols are shown; otherwise, the schematic detail is shown for the linear circuit. The logic circuits of Fig. 11 are the equivalent, not necessarily an exact representation, of the CA3157 circuits, although all logic functions are correct as shown. Some deviations from the true circuit form result from fanout and layout limitations.

To aid the user in understanding the CA3157, a brief explanation of I^2L switching logic is illustrated in Fig. 12. A current injector is a part of the switching input in the standard logic block. Many gates will ordinarily have a common injector terminal in which the p-n-p terminals are

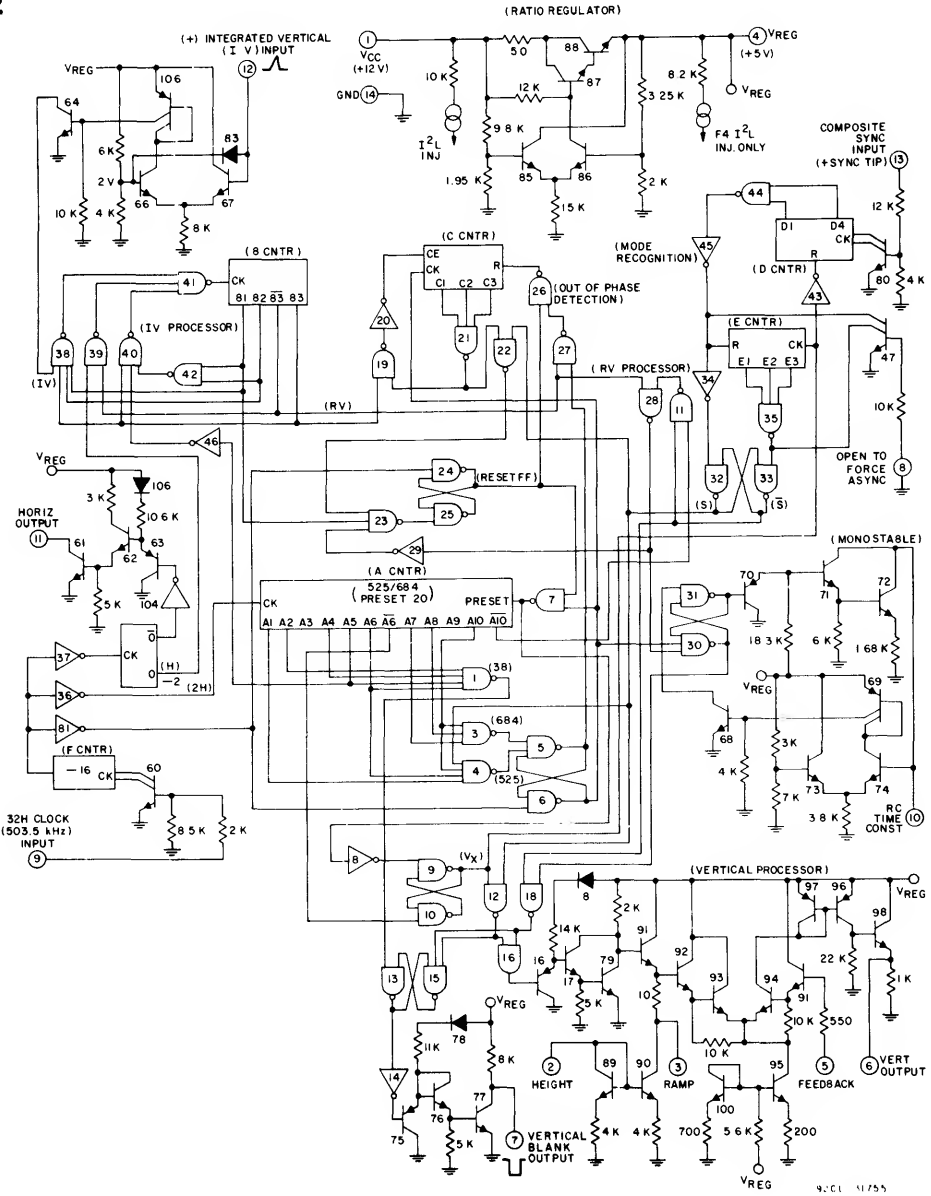

Fig. 11 - Linear/logic circuit diagram for the CA3157.

in parallel. For simplicity, only the injection bias source is shown in the power-supply circuit (Fig. 11), where it is derived from points near terminal nos. 1 and 4. The injector shown in Fig. 12(a) at terminal IB is supplied with steady-state current bias; therefore, the inverter output is at state 0 (low) when the input is 1 (or open) and 1 (high) when the input is 0 (or shorted). Fig. 12(a) shows the n-p-n transistor with a fanout of 3 collector leads. The equivalent logic symbol is an inverter with 3 outputs. A fanout of 1 to 5 leads is common and can be readily adapted to the inverter to form the NAND gate logic shown in Fig. 11. Fig. 12(b) shows 3 inverters with single collectors driving an inverter with 3 outputs. This configuration is equivalent to a NAND gate with 3 inputs and 3 outputs.

The collector of the I^2L n-p-n transistor is the n + diffusion, but to the compatible linear n-p-n process it is an emitter over the p-base diffusion. Similarly, the emitter of the I^2L device is equivalent to the collector of the linear device. The p-n-p current-injector transistor has a lateral construction in which the n base is the collector and the p collector the base of the I^2L n-p-n transistor.

The linear IC process readily adapts to incorporate I^2L integration on the same chip. The use of the same diffusion steps in both linear and I^2L circuit fabrication also permits the integration of high-density logic functions with simple linear-to-I^2L logic interface circuits. The direct compatibility of I^2L and linear processes is shown in Fig. 13. The added

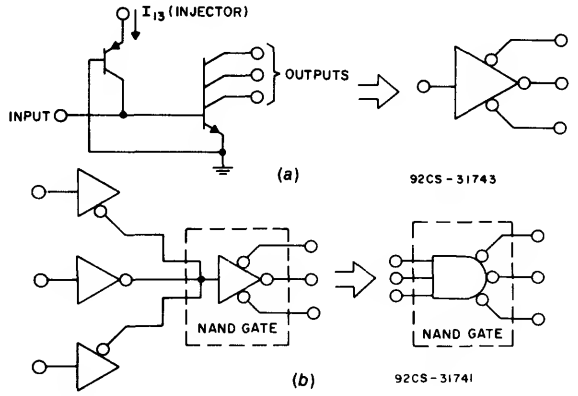

Fig. 12 - I^2L switching logic: (a) n-p-n transistor with a fanout of 3 collector leads. The equivalent logic symbol is an inverter with 3 outputs. A fanout of 1 to 5 leads is common and can be readily adapted to the inverter to form the NAND gate logic shown in Fig. 11. (b) 3 inverters with single collectors driving an inverter with 3 outputs. This configuration is equivalent to a NAND gate with 3 inputs and 3 outputs.

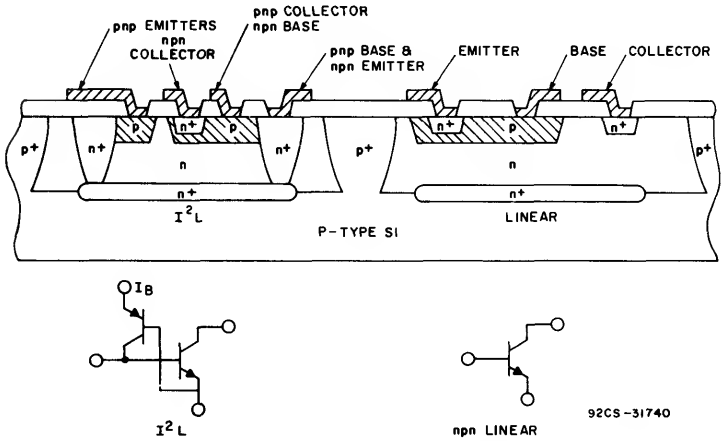

Fig. 13 - I^2L/Linear integration process.

deep n + diffusion step improves the characteristics of the I^2L device by lowering the bulk resistance in the terminal connection, and is often used in the standard linear process for the same reason.

CA3157 Divide-by-16 and Divide-by-2 Counters:

The 503.5-kHz horizontal-oscillator clock input to terminal no. 9 is buffered by switching transistor Q60. Note that in Fig. 1, the input is forward biased with a 51-kilohm resistor to the 5-volt power supply. The forward bias and the 0.001 microfarad coupling capacitor assures switching from low to high levels of oscillator drive by clamping the signal to the base-emitter switching threshold of Q60 in Fig. 11.

The switching signal is applied to the F-counter, which divides the 32-times horizontal signal by 16 and delivers a 2H signal to the A-counter clock input through inverter no. 34. The 2H pulse, buffered, from inverter no. 81 is also used to reset 2 flip-flop circuits used as pulse strecters (gates 24, 25 and 5, 6). The 2H pulse fanout from inverter no. 37 drives a divide-by-2 counter that delivers horizontal frequency clocking to the integrated vertical (IV) processor. The horizontal-rate output signal, H, at 15.734 kHz, is processed through inverter no. 104 and switching transistors Q63, Q62, and Q61. The open-collector square-wave output pulse at terminal no. 11 is the horizontal output to the predriver stage for the horizontal-deflection circuit.

CA3157 A-Counter and Timing Logic Circuits:

The A-counter is a 10-stage binary counter with a preset state of 20. Its primary function is to generate switching-state logic for the divide-by-525 (or 684) gate. It also drives the divide-by-38 vertical pulse-width gate, and directly or

indirectly clocks or controls all other major timing functions on the chip. The preset state of 20 is a preferred binary number that minimizes the number of 1-state inputs to the decoder gates.

The divide-by-525 count is accomplished when inputs from A1, A6 and A10 to gate no. 4 simultaneously go to state 1, and when the synchronous output state input from gate no. 32 to the mode recognition circuit is 1. The appropriate decoding binary number for gate no. 4 is 525 + 20 or 545, as a result of the preset initial condition of 20 instead of zero. When all input lines to gate no. 4 are in the 1 state, the output to gate no. 5 goes to the 0 state. Gate no. 3 output is normally high, and remains high unless the default-count state of 704 (684 + 20) is permitted. Gates no. 5 and 6 form a flip-flop circuit that stretches the short pulse from gate no. 4 into a 16-microsecond pulse. The reset pulse is extended to 16 microseconds to provide other gates a sustained switching state that will assure that their respective drive or decoding function is completed. To accomplish the pulse stretching requirement, the flip-flop composed of gate nos. 5 and 6 is switched by gate no. 4 to the high state at the gate no. 5 output. When the state of the 2H pulse from inverter 81 returns to the 0 state, the output of gate no. 6 will return the flip-flop (gate nos. 5 and 6) to the preset condition.

Both output polarities of gate nos. 5 and 6 are used to drive the other logic circuits. The output of gate no. 5 provides a pulse to gate no. 27 in the out-of-phase detector circuit; this pulse enables a reset of the C-counter. The 0-state output of gate no. 6 drives gate no. 7 which, in turn, resets the A-counter and drives inverter no. 8. The output pulse from gate no. 6 also clocks the C-counter and enables the monostable-oscillator circuit. However, neither the C-counter nor the monostable oscillator act as a result of the pulse from gate no. 6 unless other conditions are met.

The reset pulse at the output of gate no. 7 drives inverter no. 8, which triggers the flip-flop composed of gate nos. 9 and 10. The A-counter resets the flip-flop when A6 goes to the 0 state on binary-clock count number 32. A count of 32 occurs 12 pulses after the preset state of 20, making the switched duration of the gate flip-flop equal to 6 horizontal lines. The 1-state output pulse from gate no. 9 is identified as the synchronous vertical drive pulse, V_X.

The vertical blanking pulse at terminal no. 7 is normally initiated by the vertical drive pulse, V_X, and is terminated 19 lines later when gate no. 1 decodes a binary count of 58. The output switches to state 0 when the A2, A4, A5, and A6 outputs from the A-counter simultaneously go to state 1. This proceeding corresponds to the binary state 58, which occurs at 38 pulses or 19 lines after the A-counter reset. The output from terminal no. 7 is high during trace, Q77 is turned-off, and the potential is equal to V_{reg}. When the vertical drive is initiated through gate no. 12 or no. 18, a 0 state input to gate no. 15 will toggle the flip-flop composed of gate nos. 13 and 15, so that a 0 is produced at the gate no. 13 output. Inverter no. 14 then drives Q75, Q76, and Q77 such that terminal no. 7 is switched low. The flip-flop composed of gate nos. 13 and 15 is reset to return terminal no. 7 to the high state by turning off Q77 when the output of gate no. 1 switches low. The output will switch when 19 lines have been produced.

CA3157 Integrated Vertical (IV) and Reconstituted Vertical (RV) Processors

Positive-going IV sync is applied to terminal no. 12 and to the Q66, Q67 differential comparator. A 2-volt (40% of V_{reg}) internal reference from a voltage divider at the base of Q66 sets the switching level of the differential comparator. Over-driving signal conditions are clamped by diode 83 directly to the 2-volt divider tap. An RC coupling to terminal no. 12 with a 1-volt base reference at Q67 is used to match the available IV drive and to initiate differential switching early in the vertical sync-pulse interval. This condition minimizes vertical jitter and satisfies the time required for the mode recognition circuit to count a minimum of 9 serrations in the vertical interval. The comparator further amplifies the IV signal in Q106 and Q64 to provide a clean positive pulse to the input of gate 38.

The B-counter and logic gates 38 through 42 process the incoming sync pulse from Q64 and provide a stable RV pulse 3 to 4 horizontal lines in width. Between vertical intervals, the binary state of the B-counter at the B1, B2, B3 output is 111. The outputs of gates 38, 39, and 40 are high until the IV pulse input to gate 38 goes to state 0 and causes gate 41 to clock the C-counter to 000. Gate 39 is then in control of the B-counter clock because gates 38 and 40 are disabled by B3 which is 0. The horizontal frequency output by the divide-by-2 circuit clocks the B-counter through gates 39 and 41 by means of the inverted horizontal timing pulse. When state 100 is reached in the B-counter, $\overline{B3} = 0$, and gate 39 is disabled to stop the H pulse from clocking the B-counter.

The RV pulse is identified by the $\overline{B3}$ output of the B-counter, and goes to the 1 state when the IV sync triggers the B-counter and the 0 state when the B-counter reaches state 100. The $\overline{B3}$ or RV pulse controls the reset of the C-counter and the logic of the RV processor, which consists of gates 11 and 28. if no sync has occurred, $\overline{B3}$ remains in the 1 state, as does the output of the C-counter logic gate 21.

Logic control of the out-of-phase detector is also supplied to gate 19 by the B3 output of the B-counter. In addition, the B1 output logic is a part of the out-of-phase detector and RV processor logic requirement to initiate a reset condition at the input of gate 23. In the asynchronous mode, gate 11 of the RV processor is in the 1 state as a result of the mode logic, $\overline{S}$, of gate 33. When the binary output of the A-counter is a binary 512, a total of 492 pulses have been clocked from state 20 to state 512. When the binary state is 512, $\overline{A10} = 1$ and gate 11 switches the output of gate 28 to 1, but only when $\overline{S} = 1$. Therefore, in the asynchronous mode, when $\overline{S} = 1$, 492 pulses or 246 lines of noise immunity occur before gate 28 is permitted to be switched by the RV pulse, which resets the A-counter and triggers the monostable oscillator. The output of gate 28 to inverter 29 initiates the reset of the A-counter while the monostable trigger is supplied to the input of gate 30. In synchronous conditions, $\overline{S} = 0$, and the RV processor is controlled at the input to gate 28 by the RV pulse.

It remains for the B-counter to be clocked to the 111 state following the RV vertical pulse that leaves the B-counter in the 100 state. When $\overline{B3}$ goes to state 0, the H pulse can no longer clock gate 39. At this point gate 40 is enabled so that

it can be driven by inverter 46 each time A5 of the A-counter changes state from 1 to 0. Note that the condition of B1 and/or B2 is 0, so that the output at gate 42 is kept at state 1 until the B-counter output reaches state 111. When this state is reached, the output of gate 42 switches to 0, and inverter 46 is prevented from initiating any further clock changes. The A5 condition for clocking the B-counter occurs on multiples of the binary number 32. Thus, some 35 horizontal lines of delay occur before the B-counter can be initialized to clock on the IV sync signal. The count of 35 lines is derived from 3 times 32 less the initial preset of 20 divided by 2 for clocks per line minus the period of 3 lines during the RV switching. The delay in returning the B-counter to 111 provides protection from double pulsing conditions at the IV input, such as strong co-channel interference.

CA3157 Out-of-Phase Detector and Reset Functions

The out-of-phase detector consists of the C-counter, inverter 20 and associated logic gates 19, 21, 22, 26 and 27. The reset logic is initiated by the out-of-phase detector and executed by the input logic to gate 23, which controls the reset of the A-counter if coincidence fails to occur in the detector. The out-of-phase detector compares the RV pulse to the synchronous related 525 pulse from the A-counter. With standard vertical sync, the 525 pulse and the RV pulse are present at the input to gate 27. If the pulse conditions are coincident, the C-counter is reset by gate 27, which switches the output of gate 26 to 1. If the RV pulse is not coincident with the A-counter pulse, the C-counter is clocked until 7 fields set the C-counter output to state 111. The C-counter is disabled from further clocking by gate 21, which switches gate 19 and inverter 20. This sequence sets the C-counter clock-enable input (CE) to zero. The C-counter is also enabled by B3 = 1 (no sync), which allows the counter to advance. An A-counter reset is initiated through the chain of switching gates 21, 22, 23, 25, 24 and 7. Gate 22 is enabled by the synchronous mode condition and, when switched by gate 21, enables gate 23. The condition for 7 fields of delay is based on the designer's practical judgment of a preferred choice to minimize jitter in the vertical trace under conditions of degraded vertical sync.

When all logic states at the input to gate 23 are 1, the gate 25 and 24 reset flip-flop is toggled, and the input to gate 7 is switched to 0 while the gate 7 output goes to the 1 state and resets the A-counter. Under conditions of normal synchronous detection and coincidence, the RV pulse resets the A-counter when B1 goes to the 1 state. The output from gate 22 is high under standard sync conditions, making $\overline{S}$ = 0. The RV pulse switches the output of gate 28 to state 0. Inverter 29 changes this 0 to 1 and applies it to the input to gate 23. The B1 condition is imposed to further minimize vertical jitter caused by fluctuations in the leading edge of the RV pulse. The B1 = 1 condition provides for an overlap of the RV pulse and the 525 pulse, reducing the possibility that the C-counter will clock unnecessarily under degraded-sync conditions. When gate 23 toggles the reset flip-flop, the flip-flop remains reset and maintains a 0 level at the input of gate 7 until inverter 81 switches the gate 24 input to 0 at the end of 16 microseconds. The conditions for reset at the input of gate 23 terminate when the C-counter is reset. The input to gate 21 is low, switching the output of gate 22 to a 0 state and disabling gate 23.

CA3157 Mode Recognition and Mode Selector Functions

The mode recognition circuit consists of the D and E counters and their associated logic gates. The purpose of the mode circuit is to provide synchronous (S) or asynchronous ($\overline{S}$) control-mode logic to the mode-selector (gates 12 and 18), the RV processor (gate 11), the out-of-phase detector, and the A-counter (gate 4). The mode-selector circuit selects either Vx or monostable oscillator drive based on S or $\overline{S}$ logic; gate 16 accepts either switching input type as drive for the vertical processor. The logic states of S and $\overline{S}$ are determined by the presence of a standard or nonstandard sync input at terminal no. 13, or by the forced-asynchronous condition at terminal 8. When nonstandard sync is detected, S = 0 and $\overline{S}$ = 1. After 7 fields having 8 or less serrations are counted in the D-counter, gates 32 and 33, acting as a flip-flop, enable the mode-selector, gate 18, and disable gate 12. An alternative method of switching the vertical processor to forced-asynchronous operation is to remove the ground from terminal no. 8. This method provides direct control of gates 32 and 33, thereby enabling gate 18 and disabling gate 12. In the asynchronous mode, the $\overline{S}$ input to gate 11 is at the 1 level. The other input, A10, goes to the 0 level when the A-counter reaches a binary count of 512. The resultant 1 level at the output of gate 11 enables gate 28 and allows it to directly trigger the monostable oscillator and control the A-counter reset flip-flop.

The E-counter is clocked by Vx, but is reset each time the D-counter counts 9 serrations from Q80 at the terminal no. 13 input. The E-counter is reset when outputs D1 and D4 go to a 1 level on the binary count of 9, the output of gate 44 switches to 0, and the output of inverter 45 goes to a 1 level. The Vx drive is inverted when the D-counter is reset. After Vx clocks the E-counter, the D-counter is reset, Vx goes to 0, and the output of inverter 45 goes to a 1 level. After 7 fields of nonstandard sync, the E-counter output at E1, E2 and E3 is 111. Gate 35 then switches gate 33 and the $\overline{S}$ output goes to 1. The forced-asynchronous condition directly controls the gate 32, 33 flip-flop by forcing a 0 level at the inputs to inverter 34 and gate 33.

CA3157 Monostable Oscillator

The gate 30, 31 flip-flop is toggled by the RV pulse or by the 684-count pulse of the A-counter through the output of gate 6. In asynchronous operation the output of gate 6 remains high (logic state 1) unless the gate 5, 6 flip-flop is toggled by the A-counter, enabling gate 30 to accept the $\overline{RV}$ trigger input from gate 28. In the absence of sync, a 684 count will toggle the monostable oscillator at a frequency of 46 Hz.

When gate 30 is triggered by $\overline{RV}$, the output of gate 31 goes to logic state 0, which is applied to the base of Q70. The Q71, Q72 Darlington is low or saturated at terminal 10 when the input to emitter-follower transistor Q70 is high. The differential pair Q73, Q74 constitutes a comparator circuit with the base of Q73 at 3.5 volts. When Q72 is turned off, the capacitor at terminal 10 charges and the voltage at the base of Q74 increasesd toward 3.5 volts. When the base of Q74 reaches 3.5 volts, transistor Q69 conducts and forward biases the base of Q68. With Q68 forward biased, the input to gate 30 is switched to ground, and the gate 30, 31 flip-flop is reset for the next $\overline{RV}$ pulse. Resetting of the gate 30, 31 flip-flop turns Q72 on and discharges the capacitor at terminal 10.

The mode-selector, gate 18, is switched by gate 30 of the monostable flip-flop. The length of switching time is determined by the charge time of the terminal 10 capacitor. With an external 68-kilohm resistor and a 0.015-microfarad capacitor, the initial voltage at terminal 10 is approximately 1.2 volts. The voltage drop across the 1.8 kilohm resistor is approximately 0.3 volt; the Q71, Q72 saturation voltage is approximately 0.9 volt. The equation for transient charge time is:

$$t = -RC \ln \frac{(E_b - E_c)}{(E_b - E_o)}$$

where the supply voltage, E_b, is + 12 volts; the comparator voltage, E_c, is 3.5 volts; and the initial terminal no. 10 voltage, E_o, is approximately 1.2 volts. For the given value of R and C, t = 245 microseconds. The R or C at terminal 10 can be varied to provide for a longer or shorter pulse width.

CA3157 Vertical Processor

The vertical processor is driven by the vertical-drive pulse from gate 16. This negative pulse is applied to the base of transistor Q16, inverted by the Darlington transistor pair Q17, Q79, and applied, as a positive pulse, to the base of Q91. The emitter-follower, Q91, charges a capacitor at terminal no. 3 (the 0.47 microfarad capacitor shown in Fig. 1) to V_{reg} minus the base-to-emitter voltage drop of Q91. After the vertical pulse has gone low, a constant current discharge from the current mirror Q89, Q90 provides a ramp drive to the differential amplifier consisting of Q92, Q93, Q94 and Q91. The rate of the discharge from terminal no. 3 is determined by the input current at terminal no. 2 and controls the height adjustment of the vertical scan. Transistor Q94 drives the current mirror Q96, Q97. Transistor Q96 drives the vertical output transistor Q98 with a positivie-slope sawtooth output at terminal no. 6. Terminal no. 5 is a negative feedback input to the differential amplifier at the base of Q91. The yoke current is sampled in a small series resistor and is coupled back to terminal no. 5 with appropriate RC waveform corrections to provide the desired vertical scan linearity. Twenty milliamperes of peak current is available at terminal no. 6 to drive the vertical-deflection output stage.

CA3157 Ratio Regulator

The CA3157 is intended to be operated from a nominal +12-volt regulated power supply. The regulator is simplified to a ratio type that provides 5 volts to the internal I^2L circuits, and is available as a bias source at terminal no. 4. A small resistor in the collector of Q88 is used to prevent damage to the integrated circuit if terminal no. 4 is momentarily shorted to ground. The base inputs of the differential amplifier pair Q85, Q86 are ratio-referenced to the + 12 and + 5-volt lines, respectively. For normal variations of loading at terminal no. 4, the current in Q86 changes to correct the voltage at the base of Q87 and, through Q88, maintains + 5 volts at the V_{reg} output. Additional current loading at terminal no. 4 is limited to 30 milliamperes.

CA3157 and CA3154 Application

The circuit of Fig. 1 is the preferred application circuit for the TV receiver application. To aid the TV designer in understanding how the CA3154 and CA3157 integrated circuits work in the H-V countdown system, additional details of circuit waveforms for the significant IC terminals in Fig. 1 are shown in Appendix III. These waveforms include those describing conditions at terminal nos. 3, 4, 6, 7 and 8 of the CA3154 and terminal nos. 3, 5, 6, 7, 9 and 11 of the CA3157.

The functional partitioning of the CA3154 and the CA3157 fulfill the designer's requirements for a compatible high-performance system. The CA3136 Synchronous Pix-IF Detector and CA3135 Luminance Processor are 12-volt integrated circuits that are compatible with the CA3154 and CA3157 and that meet the same high-performance requirements.

The advantages of the H-V count-down system are high stability and the "hands-off" operation that is appealing to the television viewer. Lower cost with higher degrees of frequency stability can be achieved with the 32-times horizontal frequency. Both IC-adjustable or ceramic filters are practical in combination with the CA3154 503.5-kHz oscillator. Advances in technology have made it possible to adapt both I^2L and linear IC processes to the CA3157 countdown system requirements; the success of this adaptation is evident in the high level of performance achieved.

Acknowledgment

Technical assistance in design and application areas was supplied by M.B. Knight, A.S. Sheng, and W. Sensenig.

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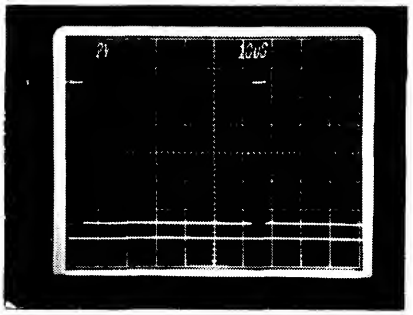
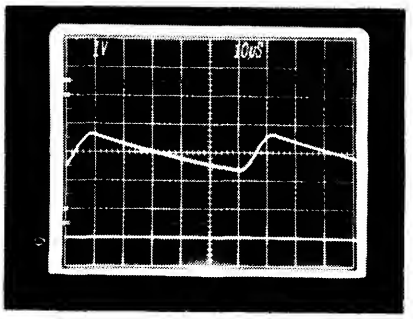
3. "Digital Vertical Sync System," S. Cox, M. Hendrickson, R. Merrel, Zenith Radio Corp., IEEE Trans. on Consumer Electronics, Vol. CE-23, No. 3, August 1977.
4. Zenith Service Manual, CM-127, 9-151, 9-151-01, and 9-152 legend for 3-plus chassis, Zenith Radio Corp.

Appendix I
Waveforms for Selected Terminals Shown in Fig. 1



CA3154, Terminal no. 3

92CS-31738



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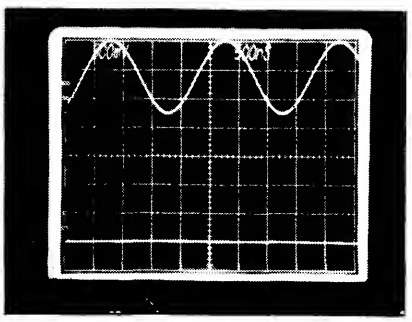
92CS-31739



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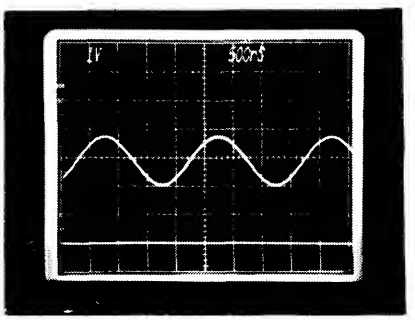
92CS-31729



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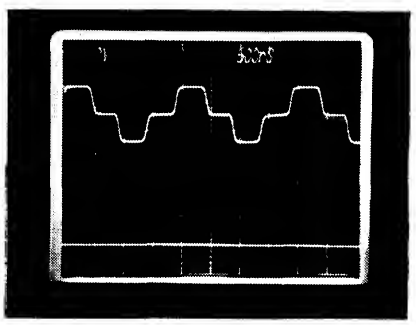
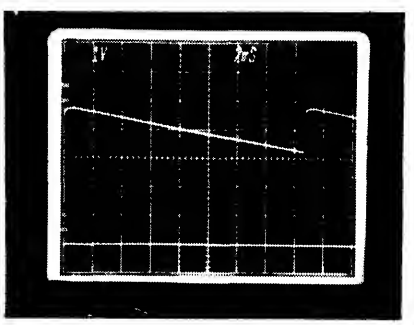
92CS-31730



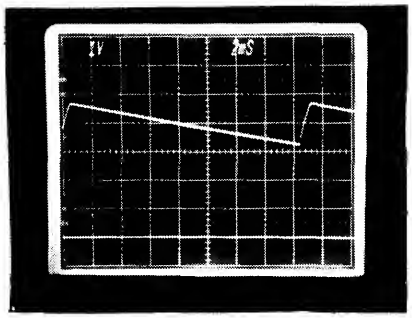
CA3154, Terminal no. 8

92CS-31731



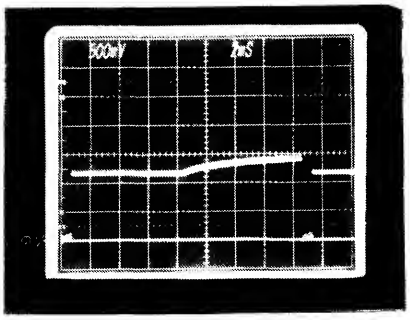
CA3157, Terminal no. 3

92CS-31732



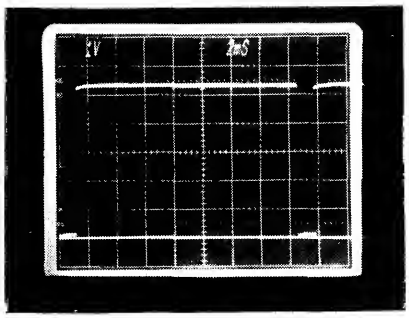
CA3157, Terminal no. 5

92CS-31733



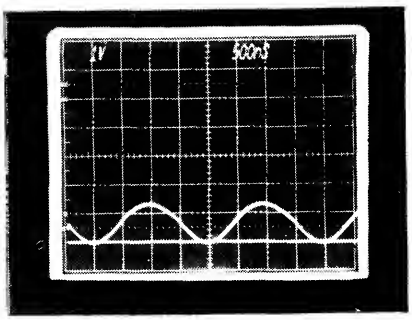
CA3157, Terminal no. 6

92CS-31734



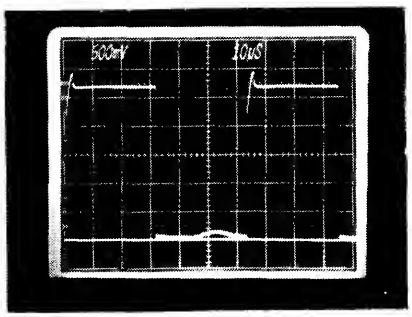
CA3157, Terminal no. 7

92CS-31735



CA3157, Terminal no. 9

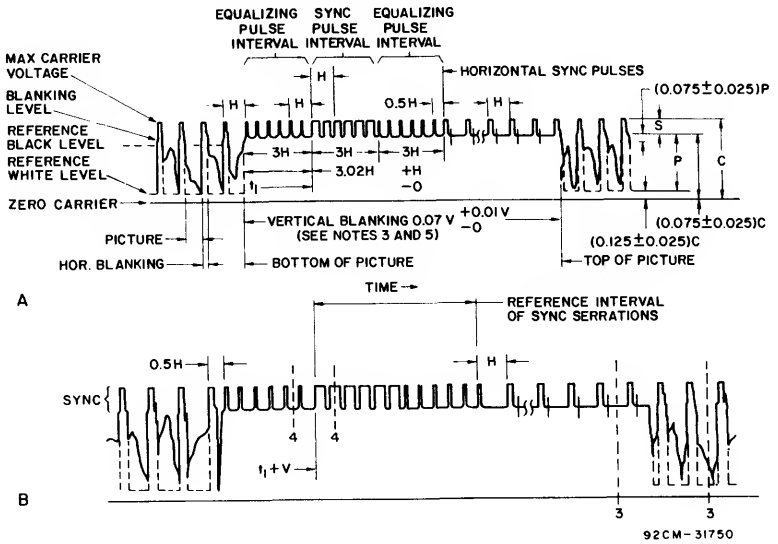
92CS-31736



CA3157, Terminal no. 11

92CS-31737

Appendix II
Referenced Timing Signals for the M-NTSC System



Notes:

1. H = time from start of one line to start of next line.
2. V = time from start of one field to start of next field.
3. Leading and trailing edges of vertical blanking should be complete in less the 0.1H.
4. Leading and trailing shapes of horizontal blanking must be steep enough to preserve minimum and maximum values of (x + y) and z under all conditions of picture content.
5. Dimensions marked with an asterisk indicate that tolerances given are permitted only for long-time variations, and not for successive cycles.
6. Equalizing pulse area shall be between 0.45 and 0.5 of the area of a horizontal synchronizing pulse.
7. Color burst follows each horizontal pulse but is omitted following the equalizing pulses and during the broad vertical pulses.
8. Color bursts to be omitted during monochrome transmission.
9. The burst frequency shall be 3.579545 megacycles. The tolerance on the frequency shall be ± 10 cycles with a maximum rate of change of frequency not to exceed 1/10 cycle/second/second.
10. The horizontal scanning frequency shall be 2/455 times the burst frequency.
11. The dimensions specified for the burst determine the times of starting and stopping of the burst but not its phase. The color burst consists of amplitude modulation of a continuous sine wave.

Appendix III
Significant Binary States of CA3157 A-Counter

Count No.	Counter Address A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	Ref. State
20						1	0	1	0	0	A-Counter preset
32					1	0	0	0	0	0	Vx 1 to 0, B-Counter to 101
58 (20 + 38)					1	1	1	0	1	0	Vert. blank pulse terminates
64				1	0	0	0	0	0	0	B-Counter to 110
96				1	1	0	0	0	0	0	B-Counter to 111
512	1	0	0	0	0	0	0	0	0	0	Async RV enable, gates 11 and 28
545 (525 + 20)	1	0	0	0	1	0	0	0	0	1	A-Counter sync count
704 (684 + 20)	1	0	1	1	0	0	0	0	0	0	A-Counter async default count

Dual Variable Op-Amp IC, the CA3280, Simplifies Complex Analog Designs

by H. Wittlinger
D. Nissman

The CA3280 IC consists of two variable op amps, each of which outputs a current (I_{out}) proportional to its differential input voltage (e_{in}) and its transconductance (g_m):

$$I_{out} = e_{in} g_m.$$

A device with such characteristics is designated an operational transconductance amplifier, OTA.

An OTA has all the characteristics of the more common operational voltage amplifier except that its output impedance ideally approaches infinity rather than zero. Thus, an OTA's forward gain is characterized by transconductance rather than voltage gain. Additionally, the CA3280 dual OTA provides a means to externally bias each of its amplifiers. The IC's transconductance parameters can be controlled and varied by adjustment of the amplifier bias current (I_{ABC}).

This design allows operational modes not easily obtained with other devices. For example, the OTA's isolation of input and output from each other and from the power supplies permits 4-terminal operation of the amplifier at frequencies down to dc. Such operation was previously only available with transformers, and only with ac.

Improved specifications

When operated into a suitable load resistor and with feedback, the CA3280 is useful in a wide variety of traditional op-amp applications, including those for its predecessor OTA, the CA3080.

But the CA3280 surpasses the CA3080 in several performance areas, including input error terms, output current drive, noise and distortion. Table I shows specifications for the high-performance version of the CA3280, the CA3280AG. Additional advantages come from the device's linearizing diodes and from its construction: The chip is designed with cross-coupling of critical circuitry. This interdigitation reduces amplifier dependence on thermal and process variations, and it assures excellent matching of the two amplifiers on chip. The gold-metallized silicon-nitride passivation of the 16-pin plastic-packaged device produces tenfold improvements in MTBF.

TABLE I — Specifications for the High-Performance OTA, the CA3280

CONDITIONS: 25° C, V_{SUPPLY} = ± 15 V

CHARACTERISTIC	I_{ABC}	MIN.	TYP.	MAX.
INPUT OFFSET VOLTAGE	100 μA		0.25 mV	0.5 mV
INPUT OFFSET VOLTAGE CHANGE	1 μA to 1 mA		0.5 mV	1 mV
TEMP = -55 TO +125° C	100 μA		3 μV/° C	5 μV/° C
NOISE VOLTAGE @ 1 kHz	500 μA		8 nV/√Hz	
PEAK OUTPUT CURRENT	500 μA	± 350 μA	± 410 μA	± 650 μA
SUPPLY CURRENT/AMP	500 μA		2 mA	2.4 mA
COMMON-MODE REJECTION RATIO	100 μA	94 dB	100 dB	
FORWARD LARGE-SIGNAL TRANSCONDUCTANCE	50 μA		0.8 mmho	1.2 mmho
OPEN-LOOP TOTAL HARMONIC DISTORTION @ 1 kHz, R_{LOAD} = 15 kΩ, V_{OUT} = 20 V_{p-p}	1.5 mA		0.4%	
BANDWIDTH R_{LOAD} = 100 Ω	1 mA		9 MHz	
SLEW RATE (OPEN LOOP)	1 mA		125 V/μsec	
OUTPUT RESISTANCE	100 μA		63 MΩ	

Linearization diodes

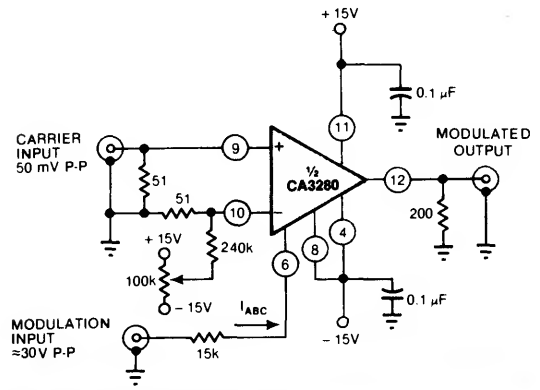
Each of the CA3280's OTAs incorporates an amplifier-bias-current (I_{ABC}) terminal; most electrical characteristics of a CA3280 circuit are externally controllable through adjustment of I_{ABC}. Important amplifier characteristics, such as transconductance, bandwidth, power dissipation, bias current, output current and input and output resistance, vary linearly with respect to I_{ABC}.

Each amplifier includes on-chip linearization diodes and diode-bias circuitry, which, when activated, permit a much wider input-signal range, reduce distortion, and allow higher output current. The diode-bias-terminal current (I_D) provides additional gain control.

The CA3280 can be used in voltage-controlled filters and amplifiers; such circuits are proliferating in electronic music, voice and sound synthesis, and fast-acquisition phase-locked-loop applications. OTA filter techniques utilize the linearly variable dynamic-impedance feature of the OTA.

Many OTA applications besides those for voltage-controlled filters employ gain control through I_{ABC}. For example, half of a CA3280 can be used to construct an amplitude modulator with a carrier frequency of 3 MHz and a modulating signal of 10 kHz, Fig. 1(a). The circuit shown is governed by g_m = (16 mmhos/mA)xI_{ABC}.

(a)



(b)

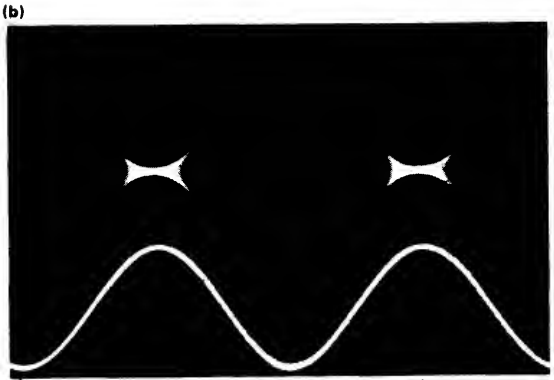


Fig. 1 - An amplitude modulator (a) produces the upper waveform shown in (b). The top trace shows the modulated output of a 3-MHz carrier (20 mV/div); the lower one, a 10-kHz modulating signal (10V/div).

High CMRR reduces circuit complexity

One of the more difficult problems in instrumentation is the conversion of a transducer's differential output signal to a single-ended signal suitable for further processing. Fig. 2(a) shows some of the techniques commonly used in this differential-to-single-ended conversion. With these systems, resistor ratios must be matched within 0.01% to obtain 80 dB of CMRR, excluding amplifier effects.

Use of a CA3280 produces a simpler, high-performance system. The inherent CMRR (94 dB min) of this OTA, coupled with its high input impedance (0.5 megohms) guarantees high common-mode rejection for low source impedance, Fig. 2(b). Note that this circuit's output, because it is a current, may be referenced to a level other than the amplifier's ground. A current output also enjoys greater noise immunity in high-EMI environments.

As shown, the configuration in Fig. 2(b) has a limited differential input-voltage range of only ±25 mV before signal compression occurs. This behavior, characteristic of all bipolar differential amplifiers, can be compensated for by using another of the CA3280's features, the linearizing diodes.

Linearizing diodes extend input ranges

When the IC's input is driven from a current source and the on-chip linearizing diodes are activated, Fig. 3(a), the CA3280 input transfer characteristic goes from the s-curve in Fig. 3(b) to the linear transfer curve shown in Fig. 3(c). Aside from the obvious improvement in linearity, the diodes also provide temperature compensation. The normal temperature coefficient of a bipolar differential amp is about -0.33%/° C; the diodes reduce this value by at least an order of magnitude. Use of the diodes also provides a second means of gain control in addition to I_{ABC}.

A simple way of considering this additional control is to assume that the diodes' dynamic impedance (R_D) shunts the input signal. The diode current I_D modulates R_D; in the CA3280, the scaling factor for this modulation is about 35 ohms/mA. Because there are two input diodes, the dynamic impedance is actually 70 ohms/mA. With two 10K input resistors, as in Fig 3(a), the actual signal input, e_{in}, equals (16 ohms/20k)xE_{IN}. For a load resistance of 15k, the amplifier gain is $g_m R_L$=16 mmhosx15k=240. Thus, a simplified basic transfer relationship can be derived for the amplifier gain: $A=K_1 R_L x(K_2/(R_1+R_2))$, where K_1=16 mmhos/mA and K_2=70 ohms/mA. If both current-programming resistors connect to the same supply, the gain remains independent of the supply voltage. Decreasing the supply voltages or diode currents diminishes only the CA3280's large-signal-handling capabilities.

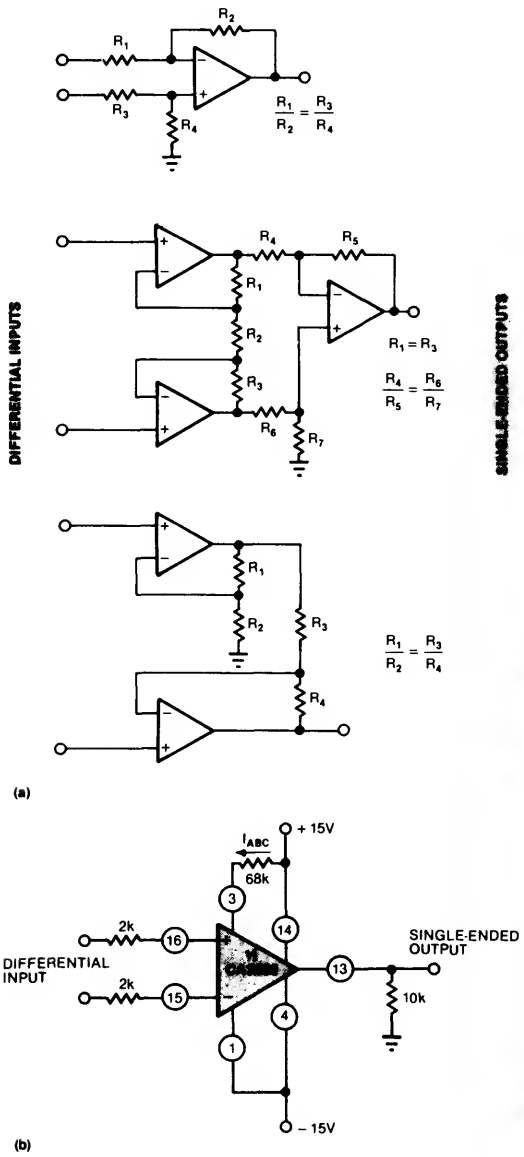


Fig. 2 - The common schemes used for high-CMR differential amplification (a) are considerably simplified with a CA3280 (b).

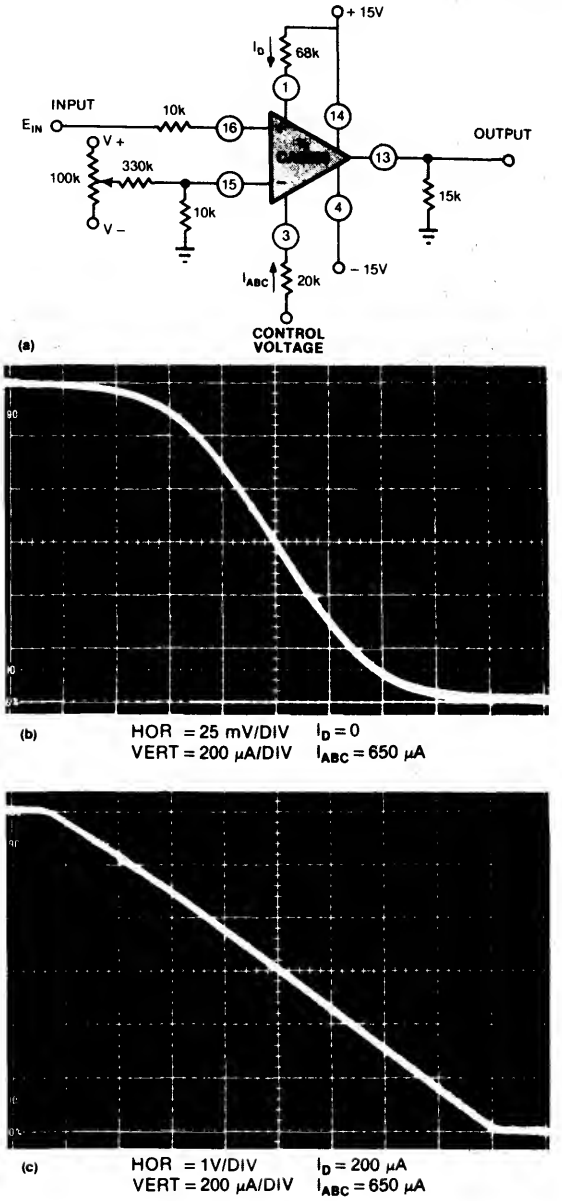


Fig. 3 - Activating the linearization diodes (a) changes the CA3280's transfer characteristic from an s-curve (b) to a linear curve (c).

ICAN-6818

Inexpensive multiplier

One application that uses the linearization diodes to great advantage is depicted in Fig. 4, where half of a CA3280 makes a temperature-compensated 4-quadrant multiplier. This type of multiplier, although not as accurate as many of the precision hybrid and monolithic units, does provide a low-cost circuit suitable for signal processing and wave shaping.

Operation of the multiplier depends on cancellation of the positive forward-current signal through R_f by an opposite-current signal from the CA3280. System transconductance is determined by R_1, R_2, R_{ABC} and R_D; R_f should equal the reciprocal of this number. Thus, only one value of programming current I_{ABC} can produce a canceling current when V_Y=0. If either or both of the inputs are 0, no output current will result. Depending on the value of V_Y, either the amplifier output current or the feedforward signal current dominates.

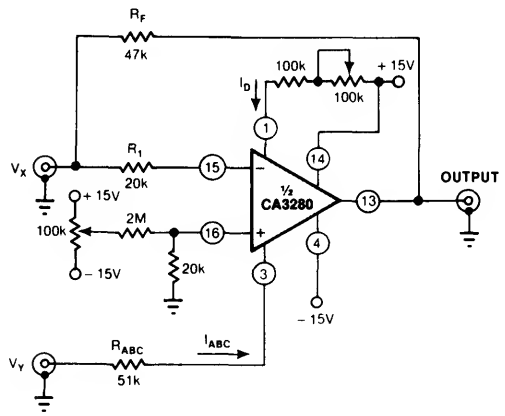


Fig. 4 - A single amplifier in the CA3280 makes an inexpensive 4-quadrant multiplier with a current output.

To obtain a differential-input 4-quadrant multiplier, both OTAs in the CA3280 can be used, Fig. 5. This circuit is the functional equivalent of the one in Fig. 4 except that an amplifier replaces R_f. Only one linearization network is used because both inputs are connected in parallel.

Higher V_X input voltages can be applied by increasing the input-resistor values. The V_Y signal must be symmetrical about ground and limited to the supply voltages.

Setup of either multiplier circuit is best accomplished with ac inputs. Once basic operation has been attained, dc procedures can be used to calibrate and set the scale factors.

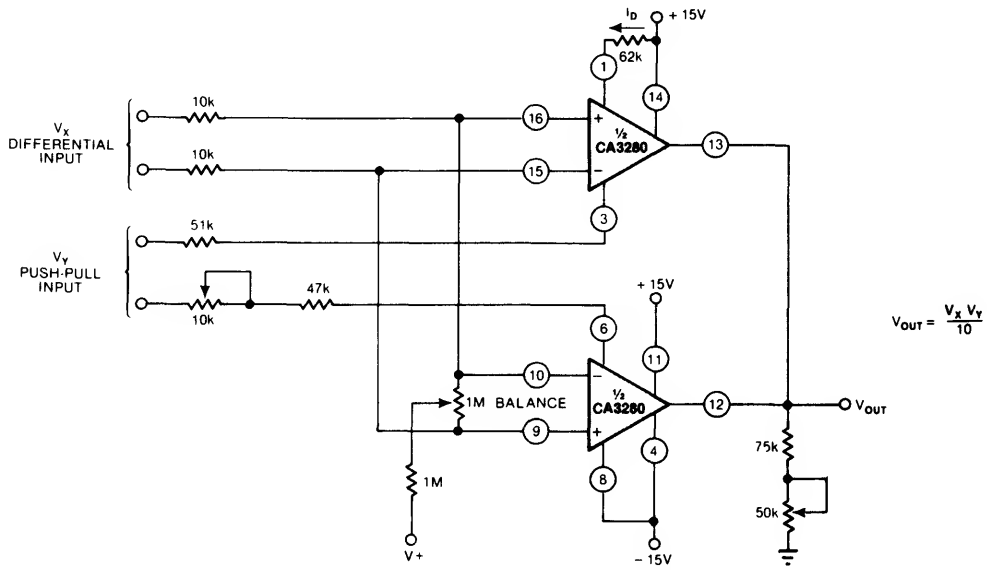


Fig. 5 - Use of both halves of a CA3280 in a 4-quadrant multiplier permits differential operation.

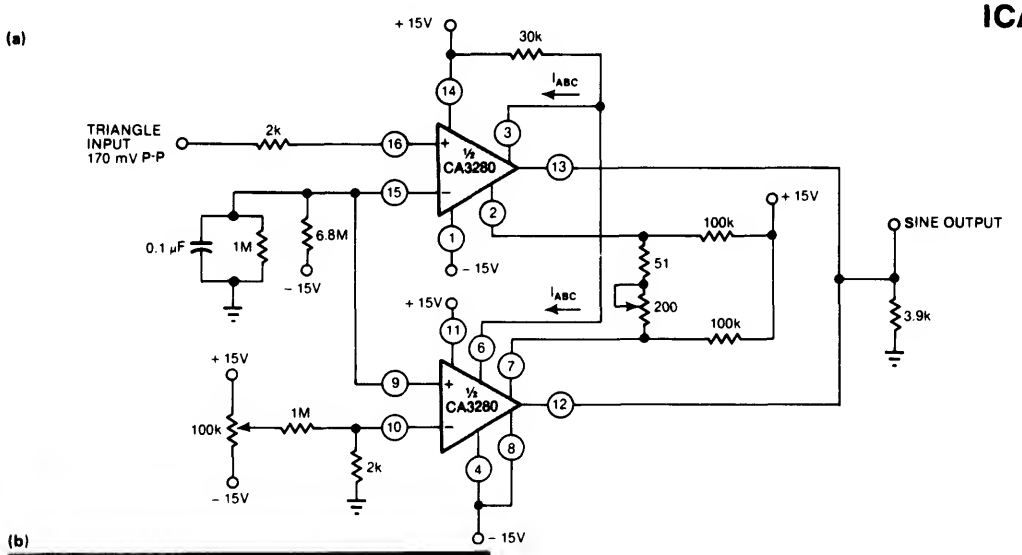


Fig. 6 - Coupling of the emitters of the OTA's differential input transistors permits construction of a triangle-to-sine converter with 0.37% THD (a). The residual distortion components can be seen in the top trace of (b) along with the sine output (2V/div) and the input triangle wave (1 kHz).

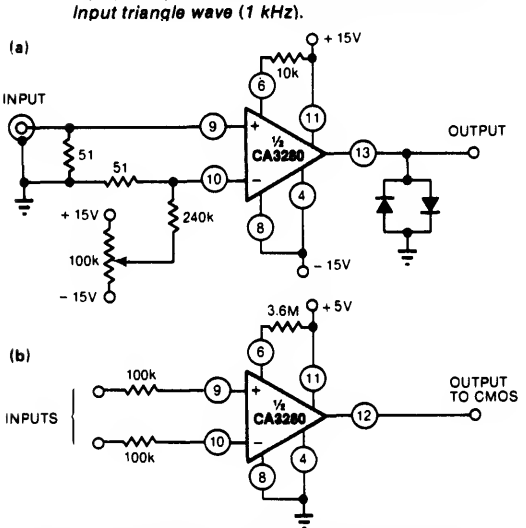


Fig. 7 - Programmability permits the CA3280 to serve as a high-speed comparator (a) or as a slower one at 20 μW (b).

Emitter outputs permit unique uses

One feature of the CA3280 has a more specialized application: The coupled emitters of each amplifier's differential input pair are available for user connection. One application for such emitter-coupled dual differential amplifiers is the triangle-to-sine converter diagrammed in Fig. 6. Two 100k resistors connected between the differential amplifiers' emitters and V+ reduce the current flow through the differential amp; this circuit permits the amplifier to fully cut off during peak, input-signal excursions. With trimming, the circuit's harmonic distortion is about 0.37%; selective-feedback techniques can reduce this figure to 0.05%. As Fig. 6(b) shows, most of the distortion stems from the discontinuity of the original triangle peaks.

Many comparators on one chip

The CA3280's programmability permits tailoring device speed/power characteristics for comparator applications. Fig. 7(a) shows the device operating in a high-speed mode with delay times less than 80 ns. The output signal is diode-clamped at ECL or TTL levels. Programming current is 3 mA; the total supply current is 9 mA.

Fig. 7(b) diagrams a micropower comparator. With a 5 V supply, propagation delay is 120 μs; total power consumption is only 20 μW.

ICAN-6823

CA3164E BiMOS Control Chip Extends Battery Life In Camera's Photoflash Circuit

by Carmine Salerno

Low standby current drain helps extend the battery life in portable consumer electronic products that must deliver only occasional bursts of power. The CA3164E control IC is a BiMOS chip that consumes less than 15 μA during standby; yet, it can provide 100 mA of chopped current to the dc-to-dc converter in an electronic photoflash circuit during the energy-reservoir charging cycle.

In the photoflash application, Fig. 1, the CA3164E drives the primary of step-up transformer T1 with symmetrically chopped current at a 500 to 2000-Hz rate. The bridge-connected diodes, D1 through D4, rectify the output of T1 and charge the energy-reservoir capacitor, C3, to approximately 280 V. The maximum charge of C3 is determined by the voltage-divider ratio R2:R3. A tap between these resistors provides a turn-off signal to pin 2 of the CA3164E. LED D6 is energized while C3 charges.

During the C3 charge cycle, capacitor C4 is also charged via D5, R4 and the primary of step-up transformer T2. When the manual triac-trigger switch (in the camera) is momentarily closed, the triac conducts and C4 is discharged through the primary of T2, generating a short 4-kV pulse across the secondary of T2. This pulse overcomes the ionization potential of the photoflash tube which, once fired, continues to draw current from reservoir-capacitor C3 until the charge is exhausted.

The CA3164E's chopper frequency, determined by R1, R5 and C5, is about 500 Hz with the components shown. The duty cycle is determined primarily by R7 and approximates 50% when R7 is 31.4 kΩ. Capacitor C3 recharges in about 20 seconds.

The bridge-type push-pull output of the IC can drive thyristors, transformers, speakers and piezoelectric transducers. The chip is suitable for many other consumer electronics applications: ionization and photoelectric smoke detectors, humidity alarms, remote wireless sensors, proximity switches and touch switches.

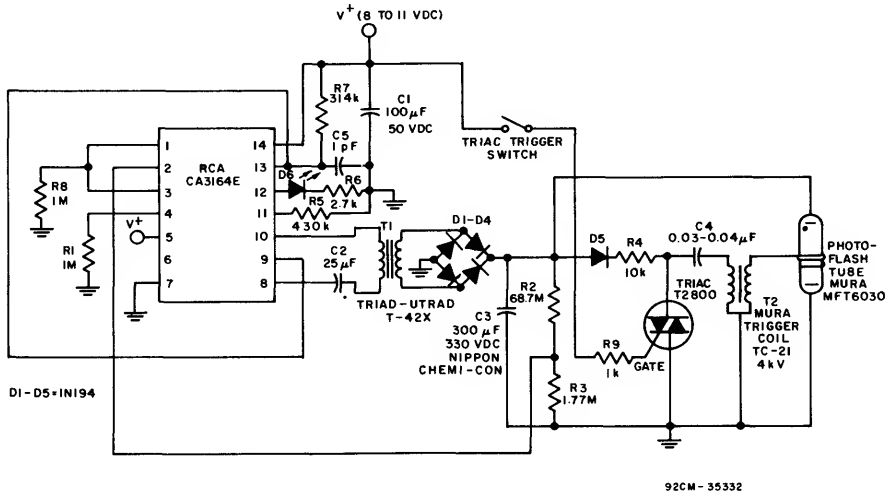


Fig. 1 - CA3164E in photoflash circuit.

Application of the CA1524 Series Pulse-Width Modulator IC's

by Carmine Salerno

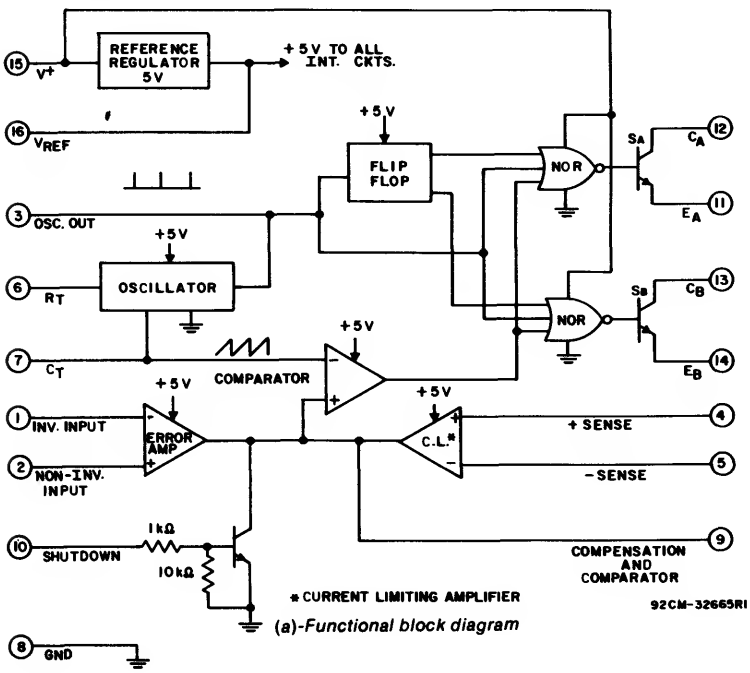
This application note reviews pulse-width modulated (PWM) circuits, and the RCA CA1524 series of pulse-width modulator IC's particularly intended for this type of application. It also includes descriptions of basic switching-regulator circuits, the generic CA1524 Series IC, its use in a variable switched power-supply application, together with a variety of its unique circuit applications.

The RCA CA1524, CA2524, and CA3524 Series, a family of integrated circuits containing a pulse-width modulator and related control circuits, are particularly applicable to switching regulators, flyback converters, dc-to-dc converters and the like. These IC's operate with a power supply in the 8-to 40-volt range for use in both low- and high-power regulators. The CA1524 series IC's contain the following circuit functions: 5-volt temperature-compensated zener reference, precision RC oscillator, transconductance error amplifier, current-limiting amplifier, control comparator, shutdown circuit, and dual-output transistor switches. These circuit functions make these devices attractive for a wide variety of other applications; e.g., low-frequency pulse generators, automotive temperature voltage regulators, battery chargers, electronic bathroom scales, etc.

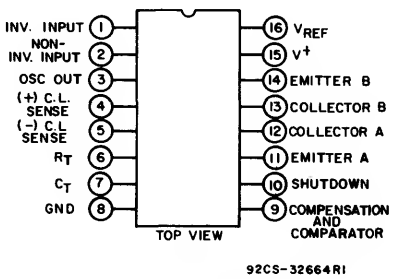
The CA1524 family of IC's is supplied in 16-lead plastic and ceramic (frit) packages, and is also available in chip form. Data on these types are found in RCA data bulletin File No. 1239.

CA1524 Series IC Features

The CA1524 PWM on-chip functions shown in the functional block diagram of Fig. 1 include an error amplifier, a comparator, an oscillator, a flip-flop, and a voltage regulator. The error amplifier senses the difference between the actual and the desired regulator output and applies this signal to the comparator's positive input. The output of this stage is in turn a function of the error signal and the oscillator's ramp voltage.



(a)-Functional block diagram



(b)-Terminal connection diagram

Fig. 1 - CA1524 series IC's.

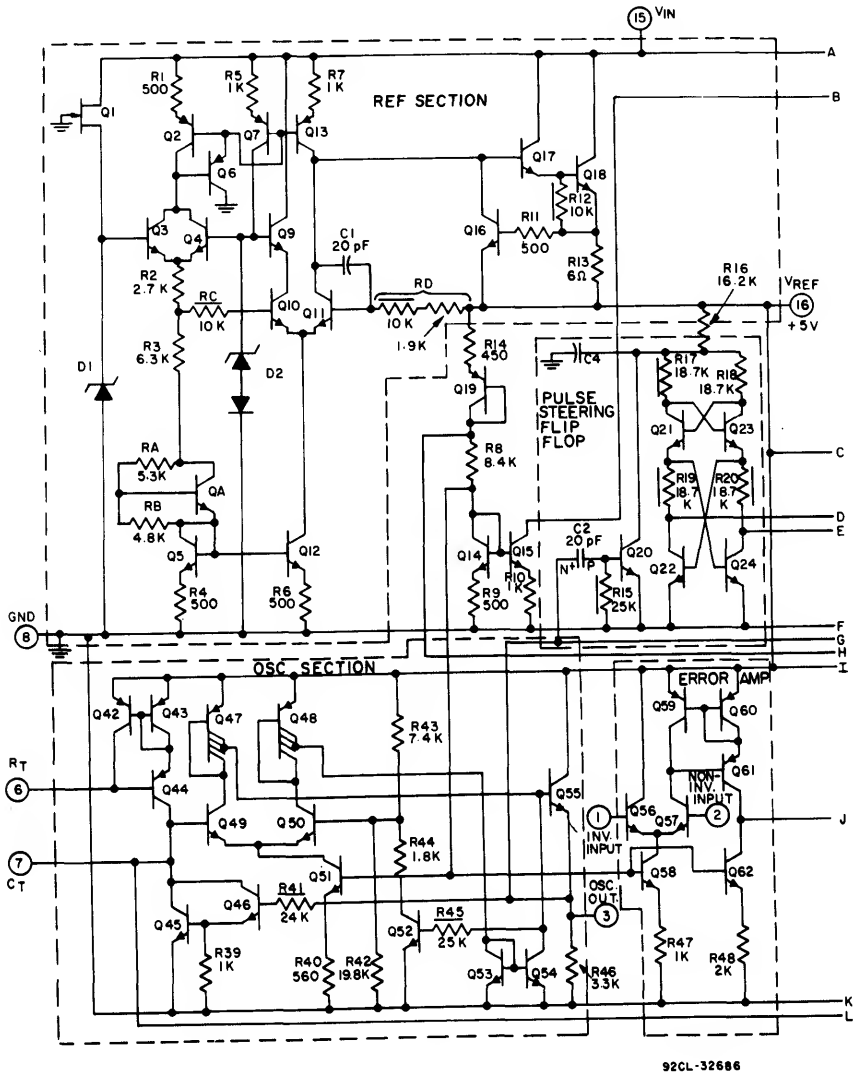


Fig. 2 - Schematic diagram of CA1524 Series IC (Cont'd on next page).

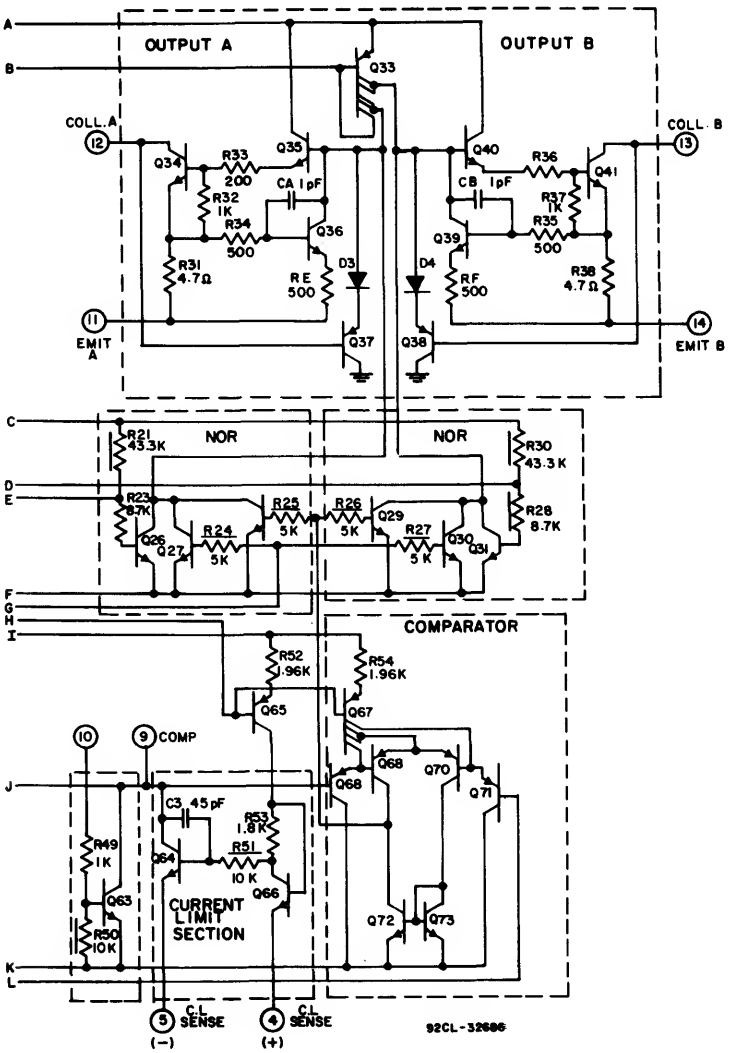


Fig. 2 - Schematic diagram of CA1524 Series IC (Cont'd from previous page).

The oscillator's output pulses alternately trigger the flip-flop, whose output ultimately provides the circuits push-pull drive signal via the NOR gates and the output transistors. The other NOR-gate inputs control the duration of the output pulses. Depending upon the oscillator's output level (high or low) and the comparator's high or low status, the "on" duty-cycle of the NOR gate can vary from 0 to 45 percent. It should be noted, that the NOR gates are on alternately. Thus, by connecting the output transistors in parallel, an effective on time of 0 to 90 percent and a wide voltage-regulation range can be attained.

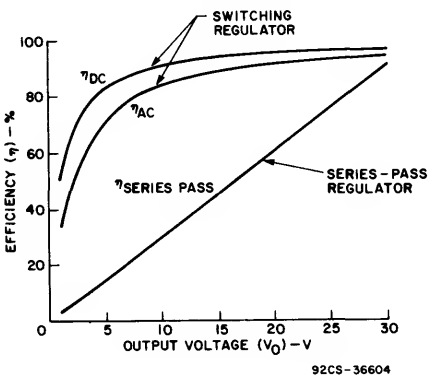
Comparative Operating Efficiencies in Series-Pass and PWM Types of Voltage Regulators

The series-pass circuit is a classical means of implementing the voltage regulator function; its simple and easy to design, but comparatively inefficient when required to operate over a range of supply voltages and output currents. The need to improve operational efficiency, in recent years, has been one of the major factors motivating engineers to use the PWM type of voltage regulator despite its greater circuit complexity.

Fig. 3 shows the high operating efficiency of the PWM type of voltage-regulator design e.g., using CA1524 and compares it with that of a conventional linear series-pass circuit. In a series-pass type of regulated power supply, the pass transistor is biased in the linear region, to permit good line and load regulation and dynamic response, but at a sacrifice in efficiency. This loss in efficiency occurs as a result of the power dissipated in the pass transistor, i.e., the product of the voltage drop and the current flowing through it. In a series-pass regulator, the output current is about equal to the input current, therefore, the overall efficiency ≅ the ratio V_O/V_{IN}.

It is, therefore, apparent that the input/output voltage differential must be kept at a minimum if high efficiency is to be achieved. Dissipation in the pass device is $(V_{IN}-V_{DD})\,I_{pass}$. $(V_{IN}-V_O)$ is typically 2 to 3 volts. There are additional small operating losses in the IC itself. By way of contrast, the pass transistor for a switching-regulator control circuit is driven between two states, "on" and "off", and since the linear region is not used, loss is essentially limited to the product of the saturation voltage and the current flowing through the pass transistor during its on state. There is a small additional loss that occurs during the on/off transitions.

Additional losses in the switching regulator include diode-voltage losses, inductor-transformer core losses, and copper losses. The overall efficiency is essentially independent of input voltage or input current. A worst-case theoretical value of the ac switching and dc transistor losses approaches a value equal to $V_O/(V_O + 2V)$ (assuming a diode V_{BE} and transistor $V_{CE(S)}$ of 1 V each). Therefore, a minimum input voltage of $V_O + 2$ V is needed to operate a switching regulator.



Pulse-Width Modulator (PWM) Switching Regulator	Linear Series-Pass Regulator
$\eta_{DC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O\,1} = \frac{V_O}{V_O + 1}$	$\eta = \frac{P_O}{P_{IN}}$
$\eta_{AC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O\,2} = \frac{V_O}{V_O + 2}$	$\eta = \frac{V_O I_O}{V_{IN} I_{IN}} \cong \frac{V_O}{V_{IN}}$

Fig. 3 - Efficiency curves for linear (series-pass) regulator and pulse-width modulated switching regulator (PWM).

CIRCUIT DESCRIPTION

The RCA-CA1524, CA2524, and CA3524 monolithic integrated circuits are designed to provide all of the control circuitry necessary for a broad range of switching regulator applications. On-chip functional blocks, shown in Fig. 1, include a zener voltage reference, transconductance error amplifier, precision RC oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating-output switches, and current-limiting and shutdown circuitry. A complete schematic is shown in Fig. 2.

Voltage Reference Section

The CA1524 Series devices contain an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50 mA output current. For higher currents, the circuit of Fig. 4 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5 volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

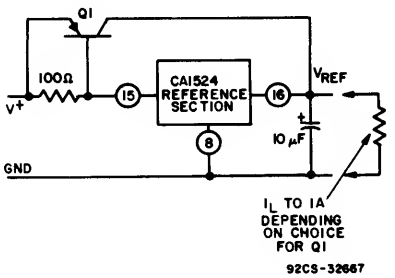


Fig. 4 - Circuit for expanding the reference-current capability.

Fig. 5 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 6 and 7, respectively.

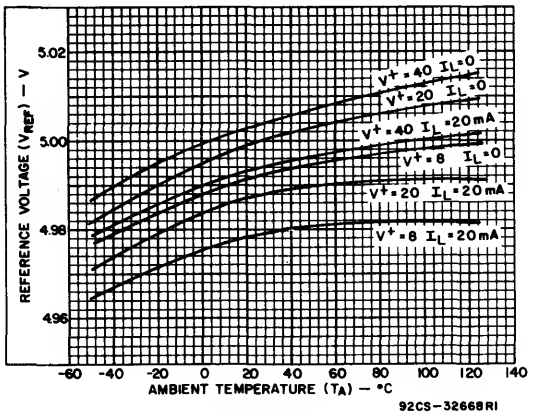


Fig. 5 - Typical reference voltage as a function of ambient temperature.

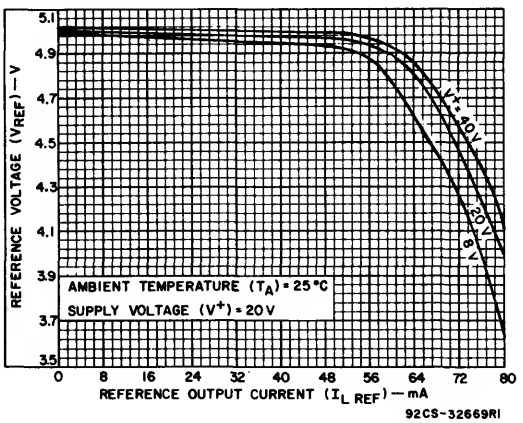


Fig. 6 - Typical reference voltage as a function of reference output current.

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor RT, establishes a constant charging current into an external capacitor CT to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to (5-2 VBE)/RT or approximately 3.6/RT and should be kept within the range of 30 μA to 2 mA by varying RT. The discharge time of CT determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5 μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which alternately enables the

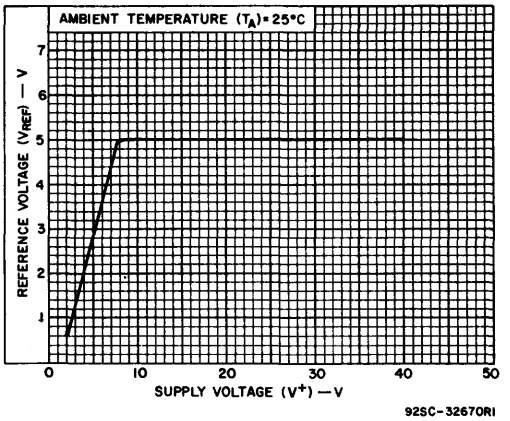


Fig. 7 - Typical reference voltage as a function of supply voltage.

output transistors. The output dead-time relationship is shown in Fig. 8, a curve which is useful when a value of dead time for a particular switching transistor has to be established. A larger value of dead time will assure that both output transistors in push-pull, bridge, or forward converter configurations will not conduct simultaneously.

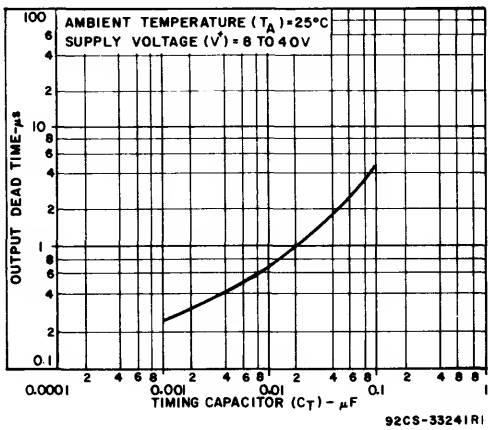


Fig. 8 - Typical output stage dead time as a function of timing capacitor value.

If a small value of CT must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF (but no greater then 1000 pF), from terminal 3 to ground.

This shunt capacitor will expand the dead time from 0.5 μs to 5.0 μs when required. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2 kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 9 may be used.

This diode clamp will limit the output voltage of the error amplifier; it also limits the error amplifier's source output current to about 200 μA. Curves for selecting the values of

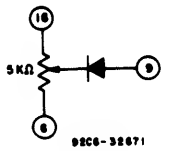


Fig. 9 - Circuit for expansion of dead time.

the oscillator resistor (R_T) and the oscillator capacitor (C_T), as a function of oscillator period (t), are shown in Fig. 10.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_T C_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals.

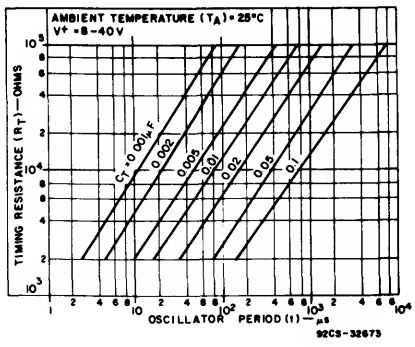


Fig. 10 - Typical oscillator period as a function of R_T and C_T.

For example, to obtain an oscillator period (t), select C_1 = 0.1 μF and R_T = 10 kΩ. Based on these values the output dead time is 0.7 μs. For series regulator applications, the two outputs can be connected in parallel to provide an effective 0-90% duty cycle with the output stage frequency being equal to that of the oscillator. Since separate output terminals are provided, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 11.

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅ 5 MΩ). The gain is:

$$A_V = g_m R = 8\ I_C\ R/2KT = 10^4,$$

where $R = \frac{R_{out} R_L}{R_{out} + R_L}$, $R_L = \infty$, $A_V \cong 10^4$

Since R_{out} is extermely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 12.

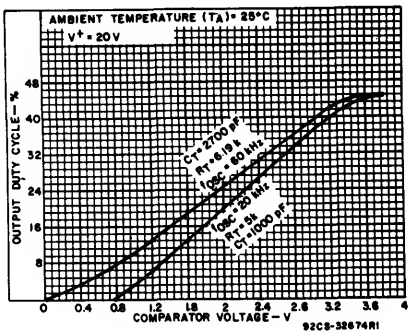


Fig. 11 - Typical duty cycle as a function of comparator voltage (at terminal 9)

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 12. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000 pF capacitor and a variable series 50 kΩ potentiometer from terminal 9 to ground. The compensation point is also a

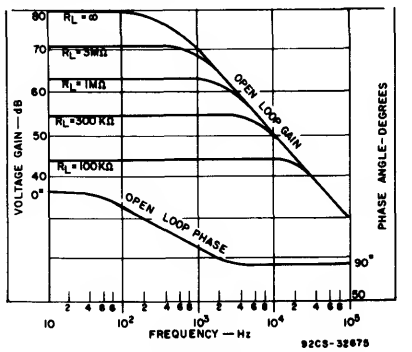


Fig. 12 - Open-loop error amplifier response characteristics.

convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for

conventional regulator applications if divided as shown in Fig. 13. If the error amplifier is connected as a unity-gain amplifier, a fixed duty cycle application results.

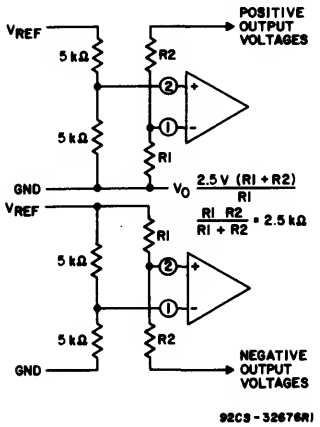


Fig. 13 - Error amplifier biasing circuits.

Current Limiting Section

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE(Q64)} + i_{(Q65)}\,R_{53} - V_{BE(Q66)}$$
$$= i_{(Q65)}R_{53} \cong 200\ mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a ± 1 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by R51, C3 and Q64 produces a roll-off pole at approximately 300 Hz.

Due to the low gain of this circuit, there is a transition region as the current-limit amplifier takes over pulse-width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current-limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminals 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (see Fig. 37). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Fig. 14. This circuit can reduce the short-circuit current (ISC) to approximately 1/3 the maximum available output current (IMAX).

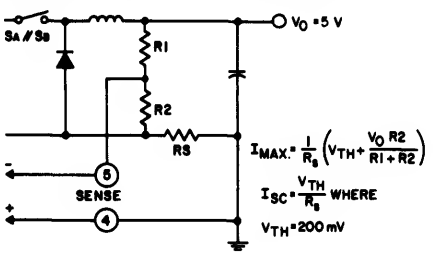


Fig. 14 - Foldback current-limiting circuit used to reduce power dissipation under shorted output conditions.

Output Section

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 15 and 16 respectively.

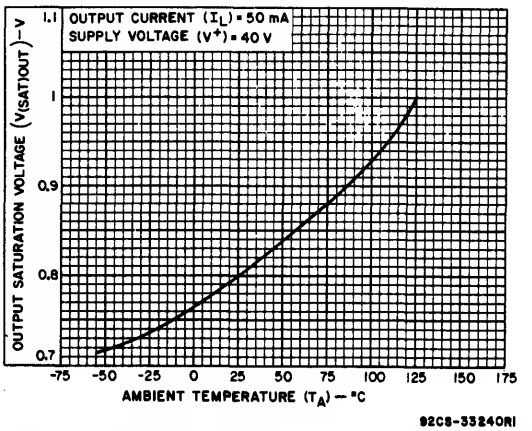


Fig. 15 - Typical output saturation voltage as function of ambient temperature.

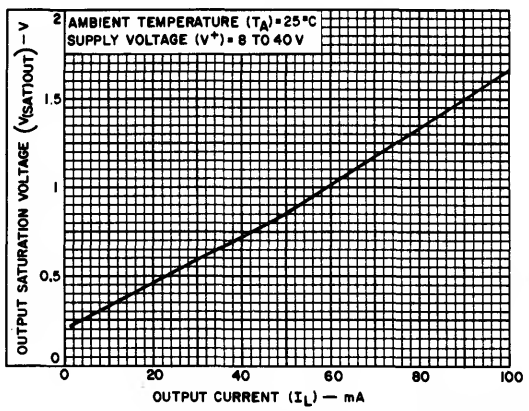


Fig. 16 - Typical output saturation voltage as a function of output current.

There are a number of possible output configurations in the application of the CA1524 to voltage regulator circuits, they fall into three basic classifications:

1. Capacitor diode-coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of these configurations are shown in Figs. 17, 18, and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load-current requirements.

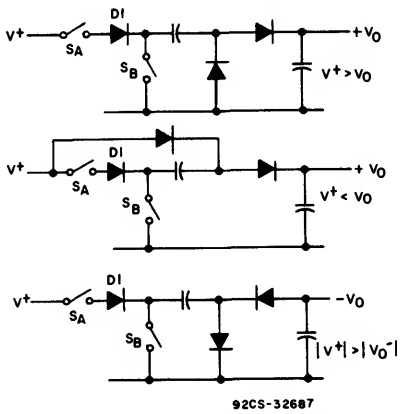


Fig. 17 - Capacitor-diode-coupled voltage-multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch SA).

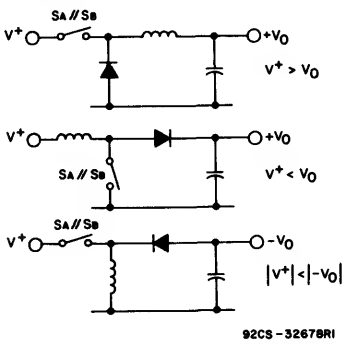


Fig. 18 - Single-ended inductor circuits where the two outputs of the CA1524 are connected in parallel, i.e.; SA//SB.

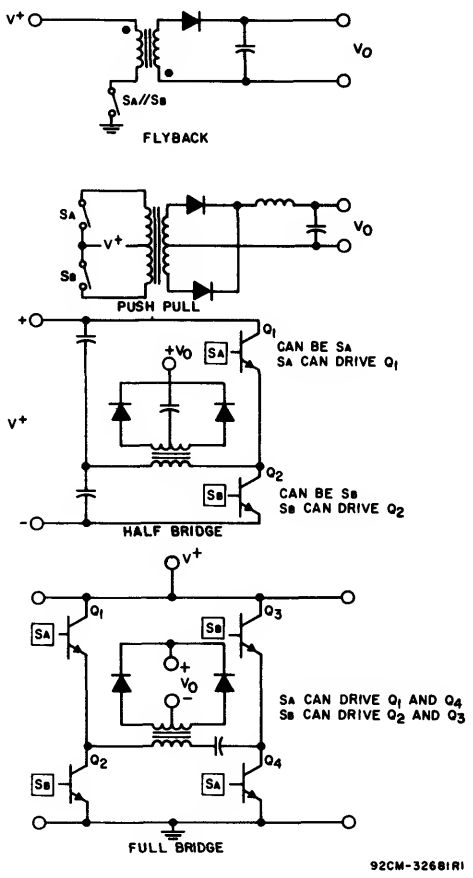


Fig. 19 - Transformer-coupled outputs.

Capacitor diode — coupled voltage multipliers are particularly useful in those low-power applications where inductive components are undesirable. Although the efficiencies of these voltage multipliers may not be as good as their inductive component counterparts, they are more efficient than the series-pass circuit.

GENERAL APPLICATIONS CONSIDERATIONS

The CA1524, in addition to having all the control circuits for switching regulator applications, employ two output NPN transistors. These transistors are internally current-limited and can be used in a variety of switching regulator configurations.

Three such modes are:

1. Single-ended single-stage configurations for forward and flyback converters.
2. Single-ended parallel-output stages for switching regulators.
3. Dual or individual stage configurations for push-pull, 1/2 bridge circuits, etc.

Single-Ended Applications

The single-ended configuration provides for simple regulator designs in which an LC and diode filter network provide the DC output voltage. The PWM controlled duty cycle can vary from 0 to 45%.

The duty cycle variation depends on the divided reference voltage applied to the error amplifier terminals. This voltage, in turn, adjusts the comparator's trip level to control the ON-time. Fig. 11 shows the duty cycle variation vs. the error amplifier output voltage (pin 9) for the CA1524.

If the outputs are connected in parallel, the duty cycle can range from 0 to 90 percent,a normal mode for switching regulators. For flyback operation, care must be taken to prevent the on time from exceeding 45% to allow for retrace in the flyback transformer.

Dual-Ended Applications

The dual-ended configuration can be used for the following applications:

1. Push-pull circuits.
2. Voltage multipliers; (capacitor-diode filters)
3. Half-or full-bridge circuits.

The oscillator has a dead-band feature to ensure against both output transistors conducting simultaneously. This dead band applies not only to the internal transistors, but for any additional drivers used for push-pull applications.

When using push-pull and bridge circuits, the dead time becomes important. Since the frequency of the oscillator is $1/R_TC_T$, a good method for establishing dead-band time is to select f first, C_T second, and then R_T. The value of C_T determines the dead time or discharging rate of C_T. The curves in Figs. 8 and 10 are used for this purpose. The oscillator provides a ramp at the C_T terminal with an equivalent dead time pulse at Pin 3 for slaving multiple units. This terminal can also be used as an oscilloscope sync. With an output resistance of 2 KΩ at Pin 3, capacitive loading of this terminal will be adequate for most applications, but for larger systems some type of external dead time adjustment must be employed. To provide an expansion of the dead time without loading the oscillator, the simple 5-kΩ potentiometer and diode arrangement shown in Fig. 9 can be used. The output frequency of each individual output stage is approximately half that of the oscillator frequency. When the stages are connected in parallel, $f_{osc} = f_{out}$.

The selection of components--capacitors, diodes, inductors, transformer cores, etc., depends primarily on the operating frequency of the switching regulator. It is important, therefore, that care be exercised in the selection of these components. Capacitors should have low equivalent series resistance (ESR) and low equivalent series inductance (ESL), because high ESR is the principal cause of capacitor ripple, and high ESL causes high-frequency ringing in the MHz region. Most capacitor manufacturers rate capacitance at 120 Hz, a frequency quite different from the 20-100 kHz operating frequency of PWM regulator circuits. Because the characteristics of capacitors may change with change in frequency, the careful selection of close-tolerance capacitors will tend to offset any degradation in PWM regulator performance resulting from the difference in the frequency rating of capacitors vs PWM regulator circuit operating frequency.

Free-wheeling diode clamps must have fast turn-on and low distributed capacitance. The dc resistance of inductors should be kept low to minimize the effects of added losses that may occur at high load currents. In addition, the selection of the size and type of transformer core will also depend on the input voltage range and on the output voltage and current requirements.

BASIC SWITCHING REGULATORS

Fig. 20 shows the basic switching regulator, the Buck or Step-Down type. In this type of regulator V_O is always $\leq V_{IN}$.

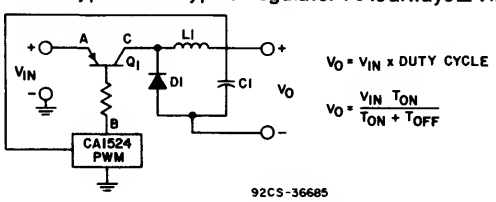
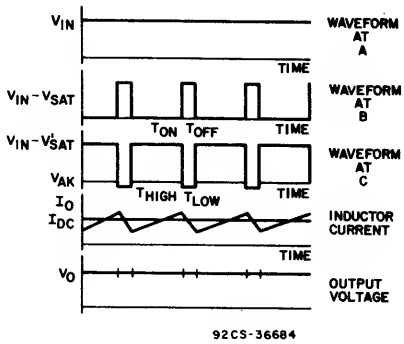


Fig. 20 - Buck (step-down) regulator.

The simplified waveforms for this regulator are shown in Fig. 21.



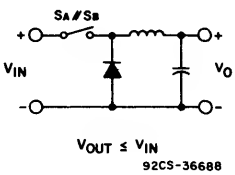
V_{IN} = Unregulated DC Voltage
V_{SAT} = Saturation Voltage of CA1524 Output Transistor
$V'_{(SAT)PASS}$=Saturation Voltage of Switching Pass Transistor
V_{AK} = Diode on Voltage
I_O = Output Inductor Current with it's DC Component
V_O = Regulated Output Voltage

Fig. 21 - Simplified waveform for buck (step-down) regulator

The Buck Regulator shown in Fig. 20 operates by chopping an unregulated DC voltage. The frequency of the circuit waveforms remains constant but the duty cycle is varied to effect regulation. The output LC filter, together with the free-wheeling diode D1, smoothes the chopped waveform. With VO set at some selected level by means of the reference voltage, the sample of the output voltage applied to the input of the CA1524 error amplifier adjusts the duty cycle in response to changes in load currents. When transistor Q1 is turned on diode D1 is non-conductive and current flows from V_{IN} through L1 to +Vo. When Q1 is off, the reserve energy in C1 provides the necessary current to the load. The overall output regulation depends primarily on the characteristics of the CA1524 and on the design of the output filter.

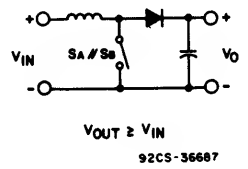
Switching regulator circuits are categorized for single-ended and dual-ended (bridge) applications. The basic circuits shown in Figs. 22 through 30 include an inductive element. In these circuits S_A represents transistor A, S_B transistor B, and $S_A//S_B$ indicates that both transistors can be connected in parallel. A description of the single-ended and dual-ended bridge configuration is given in subsequent pages.

Single-Ended Applications



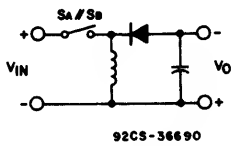
For low-power applications up to 100 watts.

Fig. 22 - Buck or step-down regulator



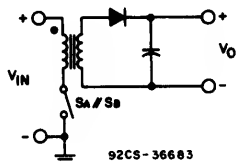
For low-power applications up to 100 watts.

Fig. 23 - Boost or step-up regulator

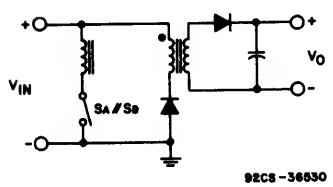


For low-power applications up to 100 watts.

Fig. 24 - Variation of the boost or step-up regulator resembles the flyback regulator and can be either step-up or step-down.



Flyback Converter

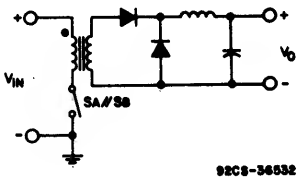


Flyback Converter with Clamp Winding.

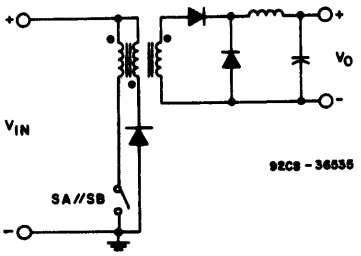
The clamp winding returns excess stored energy to the line, thereby preventing avalanche in the switching transistor.

For low-power applications from 50 to 100 watts.

Fig. 25 - Flyback converter (operating model for this converter is the boost regulator).



Forward Converter

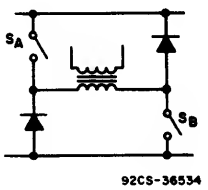


Forward Converter with Diode Clamp.

For low-to-medium-power applications from 100 to 200 watts.

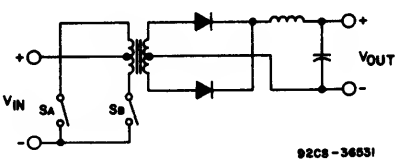
Fig. 26 - Forward converter (operating model for this converter is the buck regulator).

Dual-Ended (Bridge) Applications



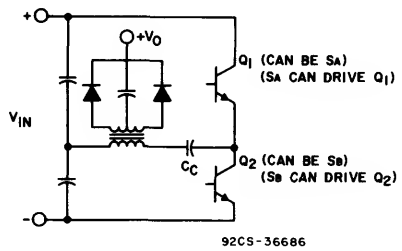
For low-to-medium-power applications from 100 to 200 watts.

Fig. 27 - Flyback or forward converter with a clamp winding.



For medium-power applications from 200 to 500 watts.

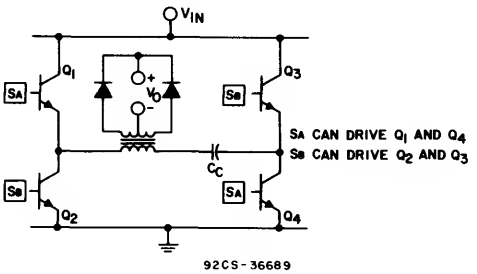
Fig. 28 - Push-pull or DC-to-DC converter.



Capacitor Cc (1.0μF-to-5.0μF range) minimizes transformer saturation problems. Diode clamps can be used across each transistor to reduce the effects of destructive switching transients.

For medium-to-high-power applications from 200 to 1000 watts.

Fig. 29 - Half-bridge circuit.



Capacitor Cc and diode clamps have same function as in the half-bridge circuit. In the full-bridge circuit full l ne voltage can be applied to the primary winding to approximately double the power output of the half-bridge circuit.

For high-power applications from 500 to 2000 watts.

Fig. 30 - Full-bridge circuit.

REGULATOR APPLICATIONS

The Variable Switcher

The following review of some of the characteristics and unique design features of a variable switching pulse-width-modulated (PWM) circuit will provide the equipment designer with some of the basic principles of a PWM circuit and its associated circuitry, and a better understanding of the CA1524 Series IC's intended for this type of application.

Although most switching regulator designs and applications imply a fixed output voltage, the CA1524 Series can be applied to a variable-output-voltage power supply.

This type of circuit provides many advantages--

1. Excellent overall efficiency for the full output range; generates less heat, thereby reducing cooling requirements.
2. Input current level ≈ maximum output current level.
3. Limited dependence on VIA (i.e., VIN ≥ VO max. + 2) at the power supply's maximum output-current level.
4. Light weight due to small, light cores.
5. Space saver.

and some disadvantages--

1. Low output voltage due to the limited lower-end range of the error amplifier (i.e., Vout min ≠ 0, but = 7V in this particular application).
2. Losses in efficiency when output-current levels are within the range of the no-load dissipation for the IC and pass transistor.
3. Time lag in changing voltage levels at no load or light loads. This time lag is due to two conditions:
   A. VC cannot change instantaneously; and
   B. CT remains charged since it is not performing its function of supplying current to the output load when the free-wheeling diode conducts.

Basic Circuit Operation

The circuit diagram of the CA1524, used as a variable-output-voltage power supply is shown in Fig. 31. By connecting the two output transistors in parallel, the duty cycle is doubled i.e.; 0-90°. Transistor Q1, RCA 8203B PNP Darlington Transistor, is used as the switching pass element. Its base is driven by the CA1524's outputs. Variability is obtained by first presetting the error amplifier inverting input (terminal 1) to 3.4 volts by appropriate selection of values for resistor network R3, R4, and R5, in accordance with the maximum output voltage desired, e.g.; this particular supply was adjusted so that Vout (max.) = 30 volts. By varying the internal reference voltage level over the amplifier's input range, an output voltage at the comparator input (Pin 9) of 0.5 volt to 3.8 volts is achieved. This output voltage will cause the ON time of the output section to vary accordingly. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage. The operating frequency of the regulator with RT = 16 KΩ and CT = 3300 pF is 23 KHz (T = 43.5 μs). The output voltage is directly related to the duty cycle and can be determined by the following equation:

$$V_O = \frac{V_{IN} - V_{(SAT)}t_{on}}{T}$$

where ton is the "on" time in μs, T is the oscillator period in μs; and Q1 is operating in a saturated mode.

The following table shows both the calculated and measured data for the regulator circuit of Fig. 31.

VO (ILOAD = 3A)	VIN −VSAT	t	ton (Calculated)	ton (Measured)
(Volts)	(Volts)	(μs)	(μs)	(μs)
30	32.5	43.5	40.15	40.50
20	32.5	43.5	26.77	26.45
10	32.5	43.5	13.88	13.70

As the load current increases, the level of the input voltage to the D5-L1-C3 filter network decreases slightly due to an increase in the saturation voltage of Q1. This change in load causes the ON time of Q1's base to increase in proportion to the decrease in voltage at Q1's collector. This decrease in voltage, in turn, adjusts the output voltage at C3. Resistor R7 controls the output voltage level.

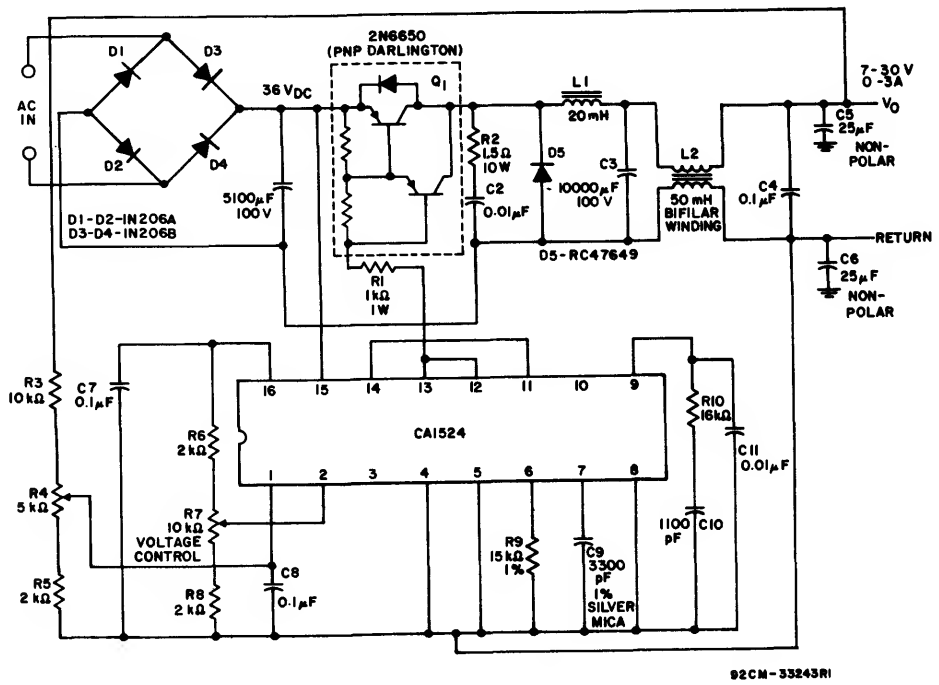
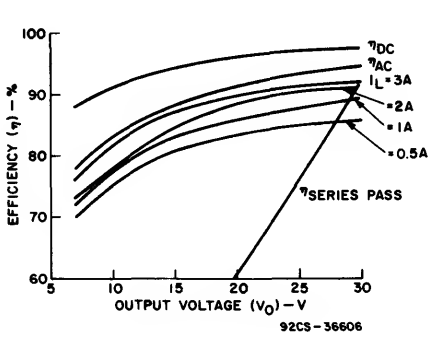


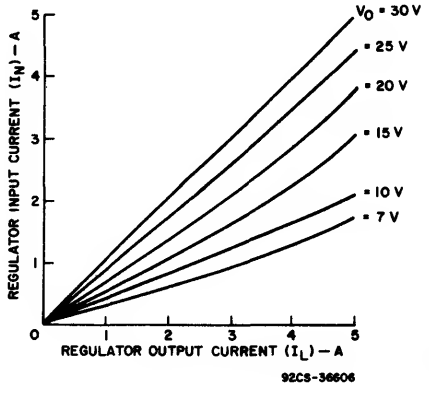
Fig. 31 - The CA1524 used as a 0-to-5 ampere 7-30 volt laboratory supply.

The efficiency curve for the variable output-voltage power supply is shown in Fig. 32 at load currents in the range of 0.5 ampere to 3 amperes over the full output-voltage range (7-30V). The efficiency of the variable switcher falls short of the ideal due to the losses incurred during the fall time of Q1's collector voltage. Use of a lower frequency would improve efficiency, but would require more expensive inductive and capacitive components. Even though the efficiency values shown in Fig. 32 are appreciably lower at the lower output voltages, the overall efficiency of the PWM variable supply is superior to that of the linear variable supply.

A major factor In the improved efficiency of the switching regulator is that output current does not have to be equal to input current as the output voltage swings between the end points of its range. The curves in Fig. 32(b) show the relationship between the output current and the input current over the full voltage range and demonstrate how the switching regulator accomplishes its high level of efficiency. At some combinations of output voltages and currents, the

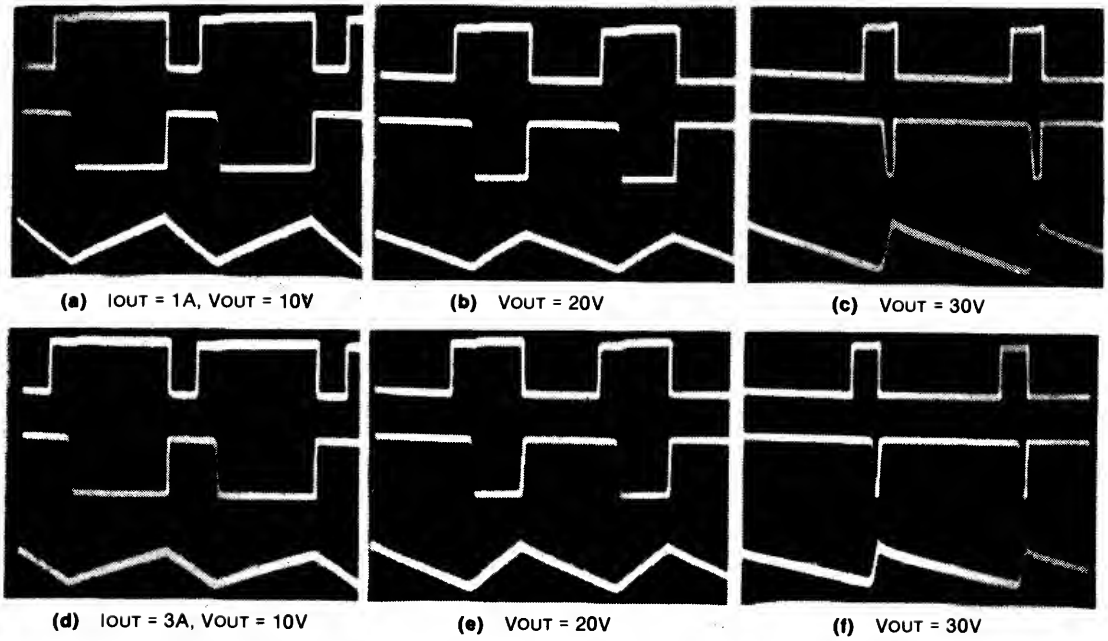


(a)



(b)

Fig. 32 - Efficiency curve for the variable output-voltage power supply shown in Fig. 31.



(a) I_{OUT} = 1A, V_{OUT} = 10V **(b)** V_{OUT} = 20V **(c)** V_{OUT} = 30V

(d) I_{OUT} = 3A, V_{OUT} = 10V **(e)** V_{OUT} = 20V **(f)** V_{OUT} = 30V

Notes:
All Photos: V_{IN} = 33V DC, Horizontal — 10 μs/Div
Vertical Scale Factors —
Upper Trace: CA1524 Output Voltage (Pins 12, 13) = 20V/Div
Middle Trace: Q_1 Collector Voltage = 20V/Div
Lower Trace: L_1 Current = 0.5A/Div, **(a), (b), (d), (e);** 0.1A/Div, **(c), (f)**

Variable-output switching power-supply designs employ pulse-width modulation techniques to achieve high performance. Note that "on" times of Q1 and the CA1524 are more dependent on the circuit's output voltage than by the output current to the load.

Fig. 33 - Typical voltage and current waveforms for CA1524 PWM regulator operated with P-N-P pass transistor and series LC-and-diode filter network.

large reservoir energy capacitor (C3) supplies the difference between the required load current and available input current (see Fig. 31). Note that the switching regulator has a higher efficiency for dc than ac -- due primarily to the additional losses caused by the input bridge rectifers D1 through D4 in Fig. 31. However, the advantage of the linear regulator is also apparent, it can provide output voltage down to nearly zero volts.

Fig. 33 shows the variation in ON time as a function of output loadings as measured at the base and collector of Q1 respectively. The regulated output voltages are 30, 20, and 10 volts, respectively with load currents of from 3 amperes to 1 ampere. The lower curve is the inductor current for the same voltages and loads. Note the change in the duty cycle and inductor current-level waveforms in response to the short ON time required to supply the 30-volt output-voltage level.

Radio frequency interference (RFI) is usually generated with any switching regulator and certain networks must be added to minimize this interference. R_2 and C_2 (Fig. 31) provide a snubber network for the switching current transients of diode D5 to reduce the level of the RFI generated. The output filter network L2 and C4 through C6 provides a bifilar coil which additionally supresses the switching noise. Varistors and input L-C filters can also be employed.

Pulse-Width Modulator (PWM) Supply Details

The CA1524 provides all sense and control functions in the variable-output-voltage power-supply design of Fig. 31. In this application, the IC's two alternately-switched output stages (pins 12 and 13) are connected in parallel to drive the switching transistor (Q1). The PWM IC provides an "on" drive-signal to Q1 that, in effect, spans a 0 to 90 percent duty cycle. (The IC's output transistors can each provide a 0 to 45 percent duty cycle during their alternate "on" periods, but when the outputs are connected in parallel their separate "on" times effectively add serially.) This 0 to 90 percent duty-cycle span makes possible the design's wide output-voltage/ current range without manual switching.

Other supply features include high operating efficiency (70 to 80 percent) over the full output-voltage/current range. This high efficiency leads to fewer heat-dissipation problems; therefore, the design is easier to cool and its reliability is higher than that of conventional linear designs. Additionally, because the circuit switches at a relatively high frequency (approximately 23 kHz), circuit capacitors and inductors are small, and the combination of small-size components with low power dissipation permits a compact overall design.

The PWM supply does present a few disadvantages. For example, output voltages of less than 7 volts cannot be attained because the on-chip error amplifier of the PWM

device has a limited low-end range. And efficiency suffers when the output load-current levels are low enough to nearly equal the active devices' no-load dissipation levels. In addition, a time lag occurs in voltage regulation with no load or light loads because C3 does not supply load current when the commutating diode D5 tries to conduct.

Component and Wiring Considerations

Besides being simple in concept, the regulator in Fig. 31 is easy to construct and align. Layout isn't critical except in the ground returns where high circulating currents could cause problems. Note the indicated chassis and earth grounding points. The circuit diagram shows two separate return lines, one for all components in the power section and one for the control section. This arrangement is essential to assure good line and load regulation as well as minimal output noise. Keep the dc output well away from the switching circuits (switching occurs at 23 kHz).

To align the supply of Fig. 31, first set the PWM error-amplifier's inverting input (pin 2) to approximately 33 volts by means of R7. (This voltage is the maximum value for the voltage-control potentiometer). Then adjust the output of R4 to pin 1 to 3.4 volts. This value yields a maximum supply output of 30 volts. When the voltage-control potentiometer is varied from minimum to maximum, the IC's comparator input voltage at pin 9 varies from 0.5 to 3.8 volts. This voltage controls the PWM's on-to-off ratio and, therefore, the conduction time of switching transistor Q1. During operation, the control voltage is set to the desired supply output voltage, and the output to the PWM feedback network consisting of R3 through R5 controls the timing.

OTHER APPLICATIONS

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 34 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 35 to convert +15 Vdc to -5 Vdc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R_2, for an output voltage range of -0.5 V to -20 V with an output current of 40 mA.

Flyback Converter

Fig. 36 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

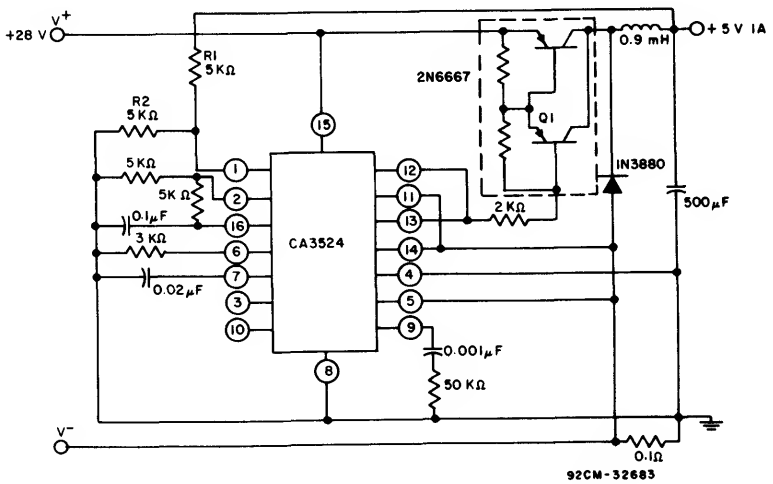


Fig. 34 - Single-ended LC switching regulator circuit.

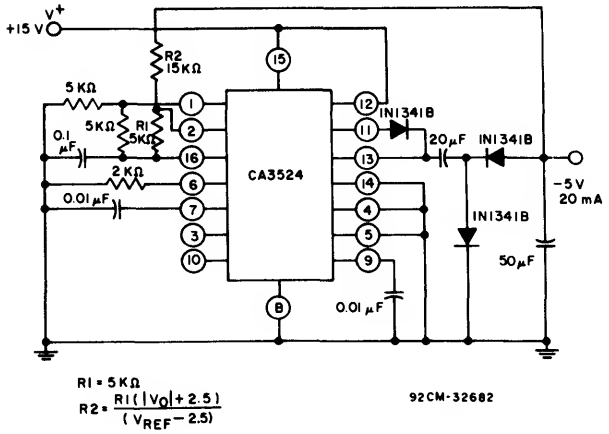


Fig. 35 - Capacitor-diode output circuit.

TABLE I — Input vs. Output Voltage, and Feedback Resistor Values for I_L = 40 mA.
(For capacitor-diode output circuit shown in Fig. 35)

Vo (V)	R2 (kΩ)	V+ (min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

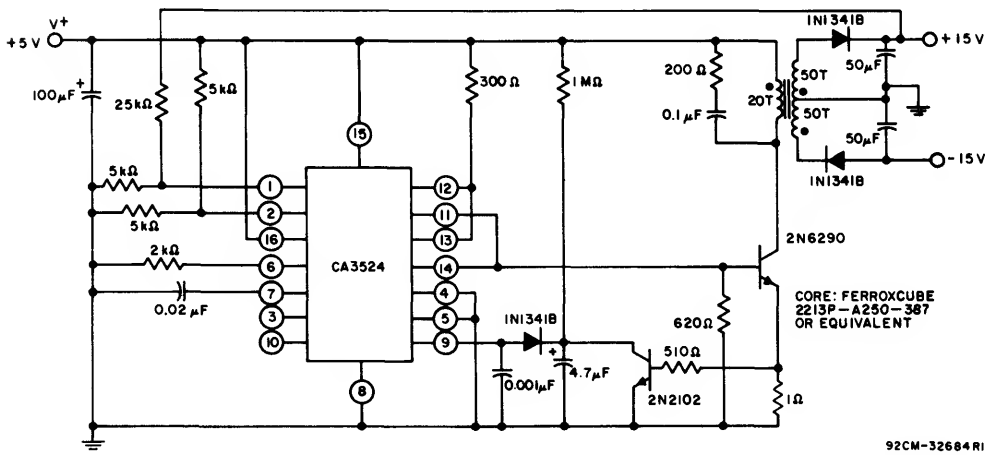


Fig. 36 - Flyback converter circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 37. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

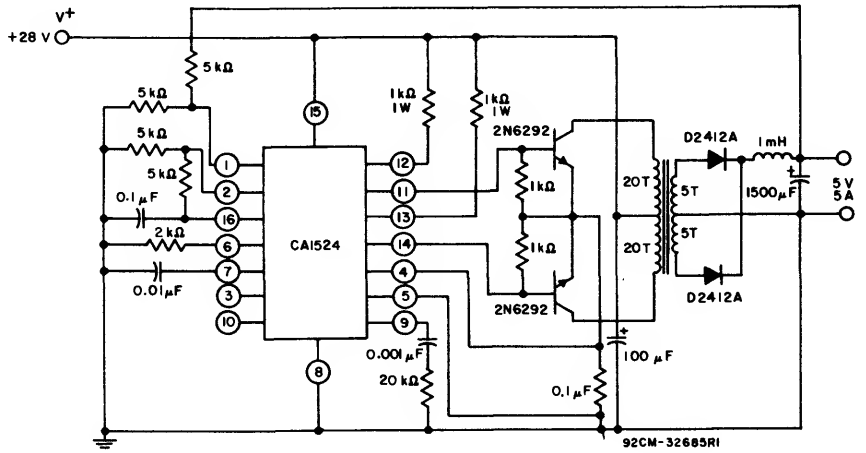


Fig. 37 - Push-pull transformer-coupled converter.

Low-Frequency Pulse Generator

Fig. 38 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5 V (or 2.5 V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R1; R2 controls duty cycle.

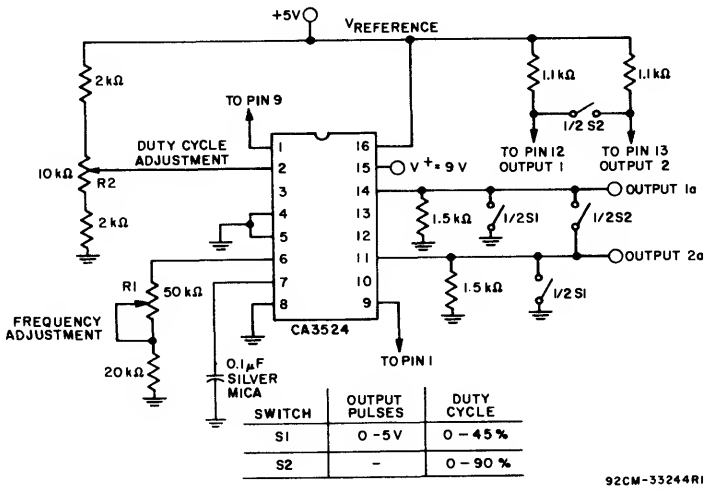


Fig. 38 - Low-frequency pulse generator.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 39 and 40 uses half (Q_2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q_1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

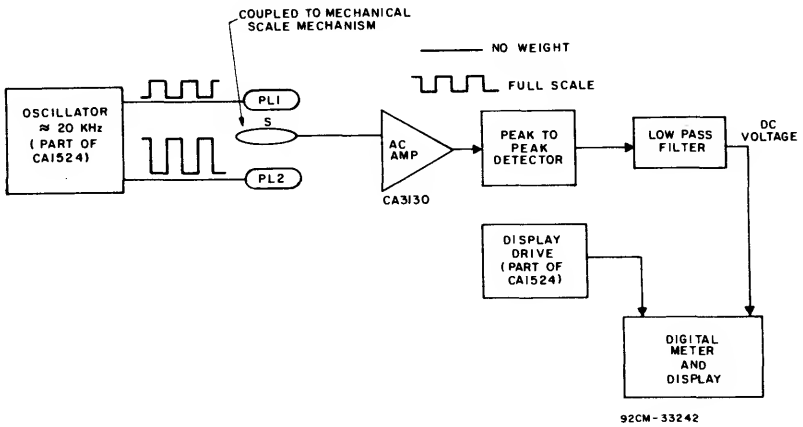


Fig. 39 - Block diagram - digital readout scale circuit.

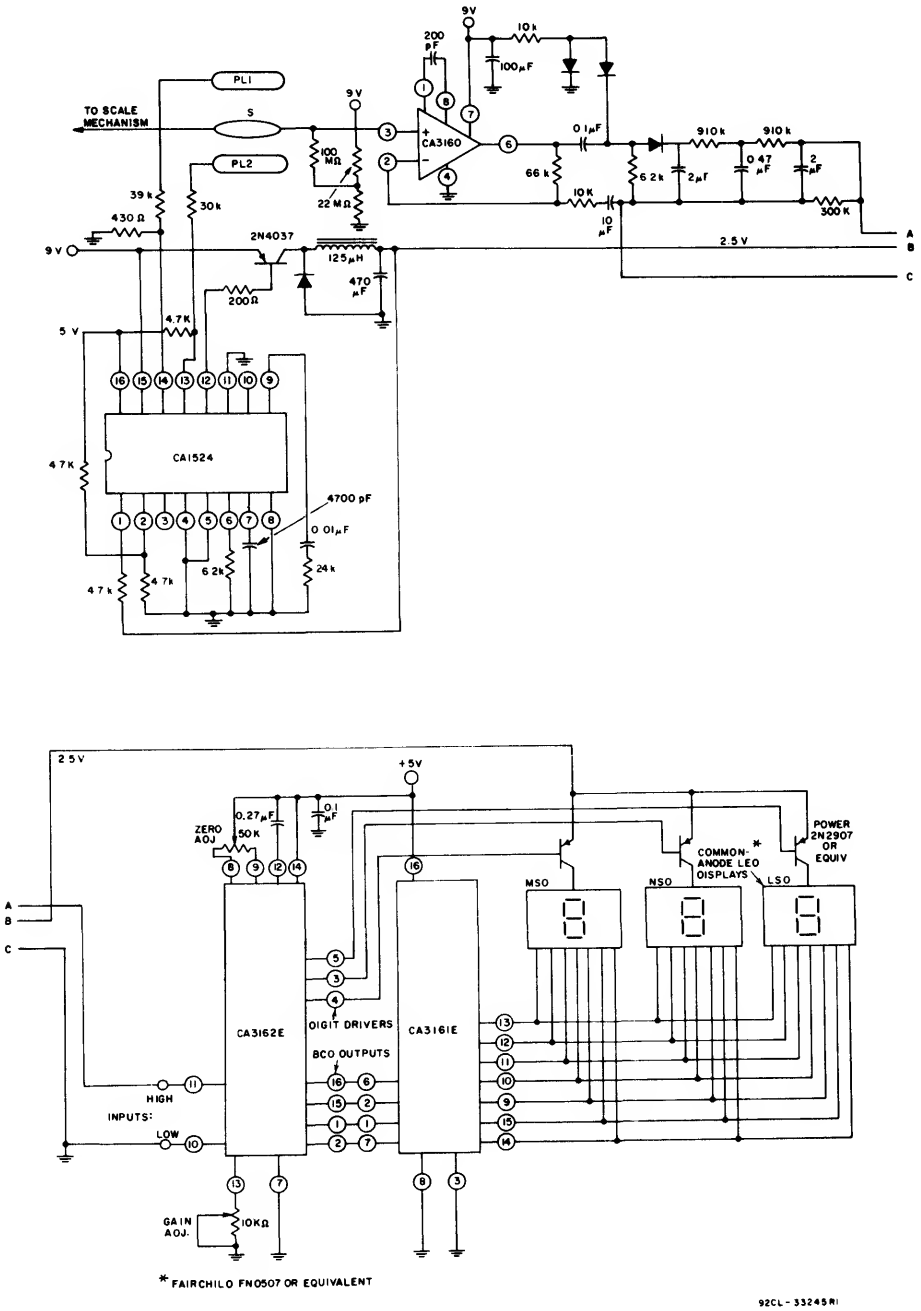


Fig. 40 - Schematic diagram of digital readout scale.

REFERENCES

For additional information concerning regulator designs and pulse-width modulator applications, and for a list of integrated circuits and power transistors suitable for series switching applications, refer to the following publications:

1. RCA Solid State Publication MSR-310, "CA1524 Series IC's Offer Efficiency in Power-Supply Design".
2. RCA Data Sheet for the CA1524, Regulating Pulse-Width Modulator, File Number 1239.
3. RCA Application Note, ICAN-6605, "Power Devices in Off-the-Line High-Frequency Inverter/Converter Circuits". R. Minton, I. Martin, and J. Vara.
4. RCA Application Note, ICAN-6743, "900 Watt, Off-the-Line, Half-Bridge Converter Using Only Two 15-Ampere SwitchMax High-Voltage Power Transistors", R.B. Jarl and K.R. Kemp.
5. RCA Application Note, ICAN-6843, "A 450 watt, 40kHz, 240VAC to 5VDC Forward Converter Using a New Type of Transistor", R.B. Jarl and W.R. Witte.
6. EDN Design Ideas, EDN Publication, December 16, 1981, "Pulse-Width Modulators Measure Weights", C.P. Salerno and P.J. Stabile, RCA Solid State Division, Somerville, N.J.
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8. "A General Unified Approach to Modeling Switching Converter Power Stages", R.D. Middlebrook and S. Cun, IEEE Proceedings, June 1976.
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Application of the CA080 BiMOS Op-Amp Series in Low-Cost Instruments and Audio Circuits

by G.M. Harayda
J.A. Chesek

The CA080-series op amps offer lower input bias and offset currents, higher input impedances, and wider bandwidths than their BiFET counterparts and other pin-compatible op amps. Intended for low-cost test instruments, data-acquistion and audio amplifiers, the CA080 series features both PMOS and bipolar technology on a monolithic chip housed in an eight-lead DIP or TO-5 case.

The front end of the amp consists of MOSFETs in a differential-input configuration, which provides the unusually high input impedances, typically on the order of 1.5×10^{12} ohms, thereby minimizing loading effects. Low power consumption, 42 mW for a single amplifier channel, makes the op amp ideal for portable equipment. The input bias current is less than 15 pA. The input offset current is typically 5 pA; the circuit provides pinouts for external offset-voltage null-compensation circuitry (CA080, CA081, CA083).

Besides low power consumption, the CA080 series provides high gain, wide bandwidth and low input noise voltage. Unity-gain bandwidth is close to 5 MHz, typical open-loop gain is 106 dB, and slew rate is on the order of 13 V/μs. Noise is less than 40 nV/$\sqrt{Hz}$ at 1 kHZ and 38 nV/$\sqrt{Hz}$ at 10 kHz. Common-mode rejection is typically 86 dB. The device is easily capable of generating a ±25-V output-voltage swing—enough to drive a large variety of power-output devices.

There are four versions of the CA080 series: the CA080 externally phase-compensated single op amp, CA081 internally phase-compensated single op amp and the CA082 and CA083 internally phase-compensated dual op amps; Table I shows typical BiMOS specifications.

Table I – Typical BiMos Specifications

Specifications	CA080/081
Input bias current	50 pA max.
Input offset current	30 pA max.
Slew rate	13 V/μs
Bandwidth	5 MHz
Noise at 1 kHz	40 nV/$\sqrt{Hz}$
Noise at 10 kHz	38 nV/$\sqrt{Hz}$
Input impedance	1.5×10^{12} ohms

Applications

BiMOS devices are ideal for many different application areas, including the front end of ac voltmeters, audio preamplifiers, notch filters and low-current amplification circuits. The ultrahigh impedance characteristic of the CA081 is especially useful in ac-voltmeter applications, Fig. 1, where the meter must have minimal loading effect on the circuit being measured. Because of the CA081's wide bandwidth and fast slew rate, the meter operates up to 0.5 MHz. Because of the device's low input bias current, the use of the 22 megohm resistors will not significantly affect the

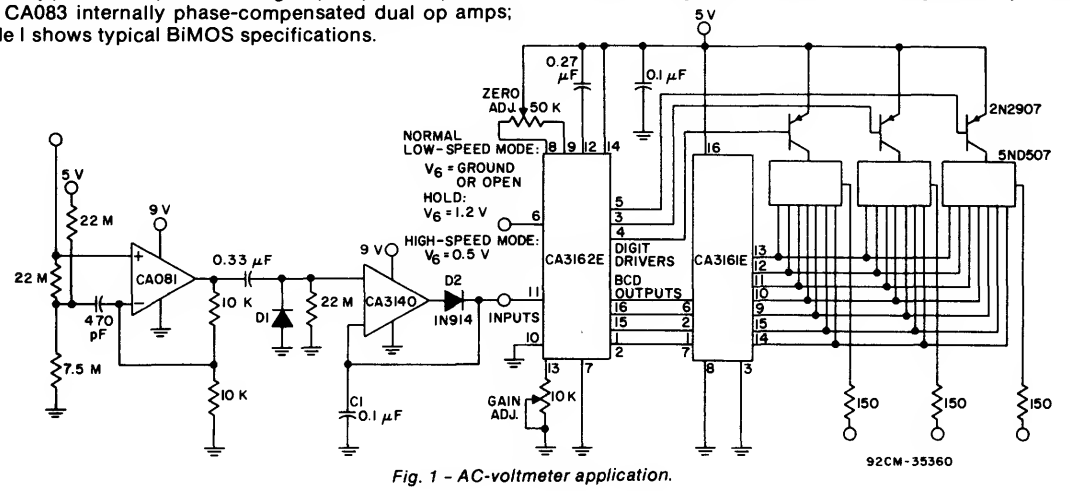


Fig. 1 - AC-voltmeter application.

quiescent output voltage of the bootstrap input circuit. This input circuit minimizes loading of the circuit under test by providing approximately 22 megohms input resistance and 15 pF input capacitance over this frequency range.

In addition, because of its very low bias currents, the CA081 is effective in making nanoampere measurements, Fig. 2. In this circuit, the current gain is a function of the ratio of R_2/R_1. For the values shown, the current gain is 1000. Thus, if the load current is 100 nA, at the output of the current amplifier circuit, the meter reads 100 nA from the supply. This measurement technique can be applied in many low-current measurement situations.

Note that the dotted components show a method of decoupling the circuit from the effects of high output-load capacitance, and eliminating the potential for oscillation in this circuit. Essentially, the high-frequency feed is provided by the capacitor, while the dotted series resistor decouples the load from the feedback loop.

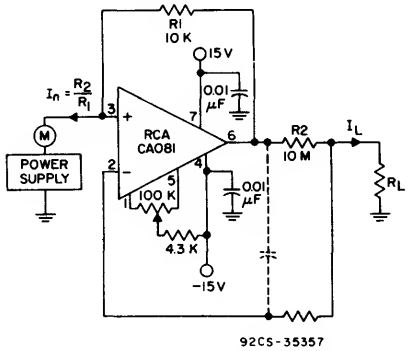


Fig. 2 - Circuit used in making nanoampere measurements.

High-Q notch filters

The low input bias current of the CA080 devices will prove an advantage in high-Q notch filters. Because of the device's minimal input currents, large-value resistors can be used in the RC filter network, minimizing the capacitance values required and decreasing the cost.

As Fig. 3 illustrates, the notch filter consists of both a low-pass filter network (R_1, R_2, C_3) and a high-pass filter (R_3, C_1, C_2) network. The values shown are for a center frequency of 60 Hz. The quality of the notch — the Q of the filter — is a function of how closely the components are matched.

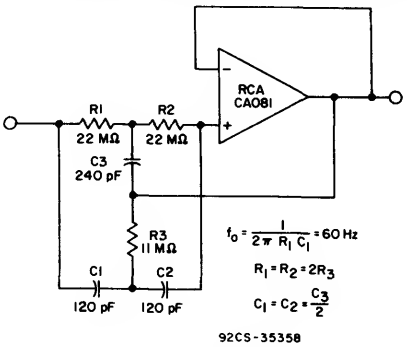


Fig. 3 - High-Q notch filter.

The BiMOS circuits will also prove useful in audio preamp applications. Fig. 4 shows one channel of a stereo preamplifier, complete with RIAA phonoequalization, tone controls, and enough gain to drive a majority of commercial power amplifiers. The total harmonic distortion of the CA080 series when driven to produce a 6-V output is less than 0.06% in the frequency range from 100 Hz to 100 kHz, and less than 0.035% in the audio-frequency range from 150 Hz to 40 kHz.

In the circuit shown, the 220-kilohm resistor, the 0.00375-μF capacitor, the 27-kilohm resistor, and the 0.01-μF capacitor network provide phonoequalization in the negative-feedback loop of the first amplification stage. A simplified tone-control circuit is provided by 100-kilohm pots and other RC filters in the negative feedback loop of the second amplification stage. The 5-kilohm pot across the output of the first amplification stage controls the volume of the preamp.

The positive supply voltage for the CA082 is connected at pin 8, while the negative supply voltage is connected at pin 4. This arrangement applies to both the TO-5 and DIP-packaged versions. The DIP-packaged CA083, however, receives +V at pin 9 and -V at pin 4.

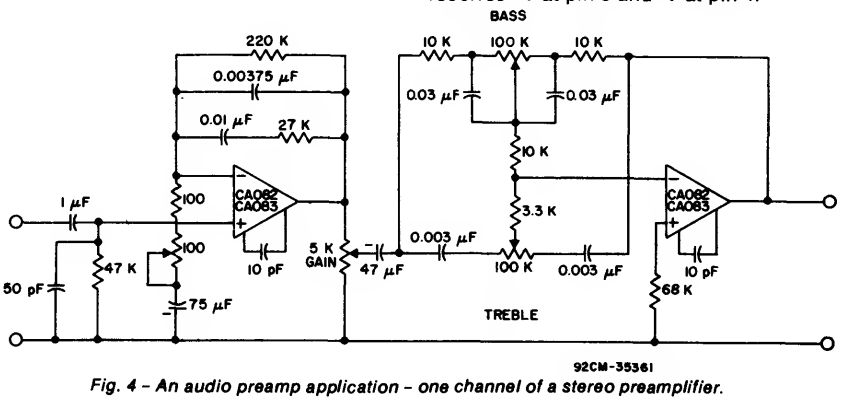


Fig. 4 - An audio preamp application - one channel of a stereo preamplifier.

ICAN-6956

CMOS/SOS Flash A/D Converter, the CA3300, Operates at Video Speed on Low Power

by M. Glincman

Flash converters relying on bipolar technology have been extremely large, expensive, and power-consuming. But flash converters that combine CMOS with a silicon-on-sapphire process will provide for video-speed analog-to-digital converters that can make impressive improvements in size, power consumption, and cost.

The first of these converters, the CA3300, is a 6-bit analog-to-digital converter with ±½-LSB accuracy, latched three-state output, and 15-MHz sampling rate (66-ns conversion time). Two CA3300s can be stacked to make a video-speed 7-bit converter, or three can be combined with a high-speed, high-accuracy digital-to-analog converter, a binary adder, control logic, and an op amp to produce a very-high-speed 12-bit A/D converter.

Because the device is CMOS/SOS, power consumption runs as low as 50 mW with a 5-V supply. (A single 4 to 12-V source is sufficient.)

CMOS construction also allows high packing density. The typical 6-bit converter requires 2^6-1, or 63, voltage comparators in parallel to quantize all analog voltage levels—CMOS allows all 63 comparators, plus one additional comparator for an overflow bit, to be packaged on one 125 x 93-mil chip.

The CA3300 has no clock, so it must be clocked externally. The clock frequency selected determines how much power the device must consume. A frequency of 11 MHz (approximately three times the video color subcarrier frequency of 3.58 MHz) will require a 5-V supply and at least 50 mW of power. To operate at four times the color subcarrier (15 MHz), the supply voltage will have to go up to 8 V and power dissipation up to 200 mW. Higher frequencies, from 15 to 18 MHz, can be obtained with voltages from 8 to 10 V, though power dissipation at 10 V will be about 500 mW typical.

The heart of the CA3300 flash A/D converter is a comparator that uses a commutating capacitor in series with an auto-balancing amplifier, Fig. 1. Sixty-four of these comparators are used to produce a 6-bit-plus-overflow conversion.

The comparator works in two phases: The first phase ($\phi 1$), called the auto-balance phase, occurs during the high cycle of the input clock. Switches 1 and 2 are closed. Since the amplifier is shorted from output to input by switch 2, it biases itself and one side of the commutating capacitor at the transfer trip point, approximately $\frac{1}{2}V_{DD}$. At the same time, switch 1 brings the reference tap voltage, derived from a resistor chain, to the other side of the commutating capacitor. The voltage across the capacitor becomes V_{REF} tap-$\frac{1}{2}V_{DD}$, and the comparator is primed for phase 2 ($\phi 2$), or the sample-unknown phase.

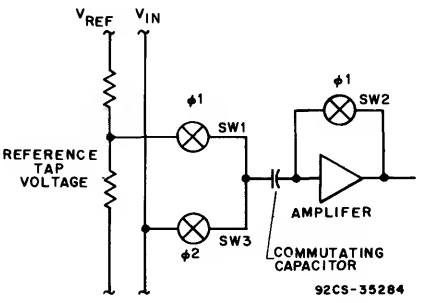


Fig. 1 - The heart of the CA3300 flash A/D converter: a comparator employing a commutating capacitor in series with an auto-balancng amplifier.

With care taken to break before make, switches 1 and 2 are opened while switch 3 is closed. Since the amplifier is a CMOS device and is no longer shorted, the capacitor is effectively floating at this end. The voltage at the amplifier now becomes $V_{IN} + V_{CAP}$. All comparators whose reference-tap voltage is less than V_{IN} will see an input voltage higher than the amplifier trip points, thereby driving the amplifiers involved to a zero. All comparators whose reference-tap voltage is more than V_{IN} will see an input voltage less than the amplifier trip points, thereby driving the amplifiers involved to a one.

All the ones and zeros can now be latched and decoded into a 6-bit binary code plus overflow, effectively completing one conversion cycle. The reference input is effectively a resistor chain with 63 20-ohm links and two 10-ohm links. Using 10-ohm links at the ends of the chain shifts the normal 0 to 1-LSB quantizing error to -½ to +½-LSB quantizing error. Since both ends of the reference ladder are available to the user, the reference voltage can float anywhere between V_{SS} and V_{DD}. Just 2.5 V are needed across the ladder. While ratiometric conversion is possible, the bandwidth of the reference input is significantly less than the bandwidth of V_{IN}, which means that only signals less than 200 kHz should be used when modulating the reference ladder.

Each CMOS comparator in the CA3300 will commutate at the clock frequency between a data-sampling or sample-unknown state ($\phi 2$) and an error-correction or auto-balance state ($\phi 1$), during which the comparators are reset to zero and the converted data is latched, then decoded for transfer

onto a data bus. Consequently, the user should anticipate a 50% duty cycle with a free-running clock and continuous analog-signal sampling, Fig. 2(a). This is especially true at video speeds.

Note also that a gain error will crop up above 5 MHz, and increase linearly with increased clock frequency. Gain should be corrected at the intended frequency of operation.

For sampling high-speed nonrecurrent or pulse data, the converter may be clocked in one of two ways. The faster way is to keep the device in $\phi 2$ during the standby state. The device can then be pulsed through $\phi 1$ in up to 33 ns. The output data becomes valid at the end of the $\phi 1$ pulse, Fig. 2(b). Note, however, that the time between sampling must not be longer than 10 μs since the commutating error-correction capacitor at the input of each comparator will eventually droop.

The second approach to sampling high-speed nonrecurrent or pulse data is to keep the converter in the auto-balance state during the standby period, which can be indefinite. When sampling the unknown, two $\phi 2$ pulses are needed to obtain valid data. The maximum speed is now reduced to the equivalent of one complete clock cycle, 66 or 67 ns, Fig. 2(c). The major drawbacks to this approach are an increase in power dissipation, since the auto-balance state has a higher current drain than the sample-unknown state, as well as an increase in delay time to obtain valid data.

Fig. 3 shows the complete circuit diagram of the 6-bit flash analog-to-digital converter, using the auto-balancing com-

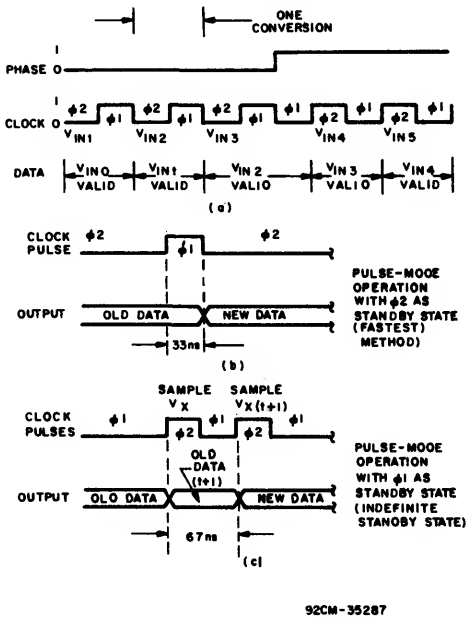


Fig. 2 - CA3300 operating waveforms.

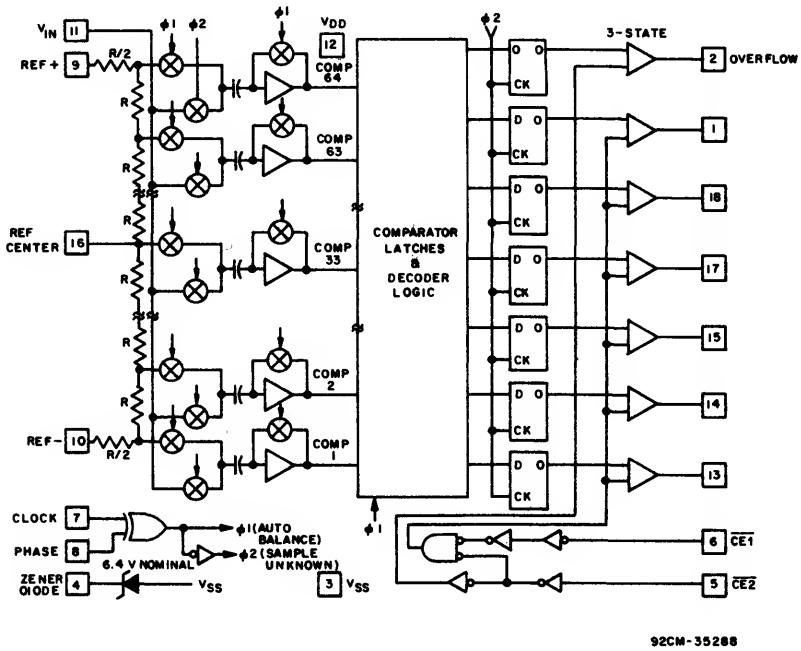


Fig. 3 - Complete circuit diagram of the 6-bit flash analog-to-digital converter using the auto-balancing comparators.

parators. Several additional control signals are included to aid the user. Two chip-enable signals, $\overline{CE1}$ and CE2, make it possible to connect not only the three-state output buffers directly to a data bus but also two devices into a 7-bit configuration, Fig. 4(a) and (b), or into a parallel configuration that doubles the speed.

A phase-control signal, which complements the clock signal inside the chip, changes the conversion phases as they relate to the input clock, Fig. 2(a). This signal is useful either in the faster configuration or in simply setting up the proper clock phase for loading data into storage. An on-board 6.4-V zener is provided for use as a reference. However, the user may go to any external voltage source whose value is within the working range of the device—i.e., 2.5 V up to, and including, V_{DD}.

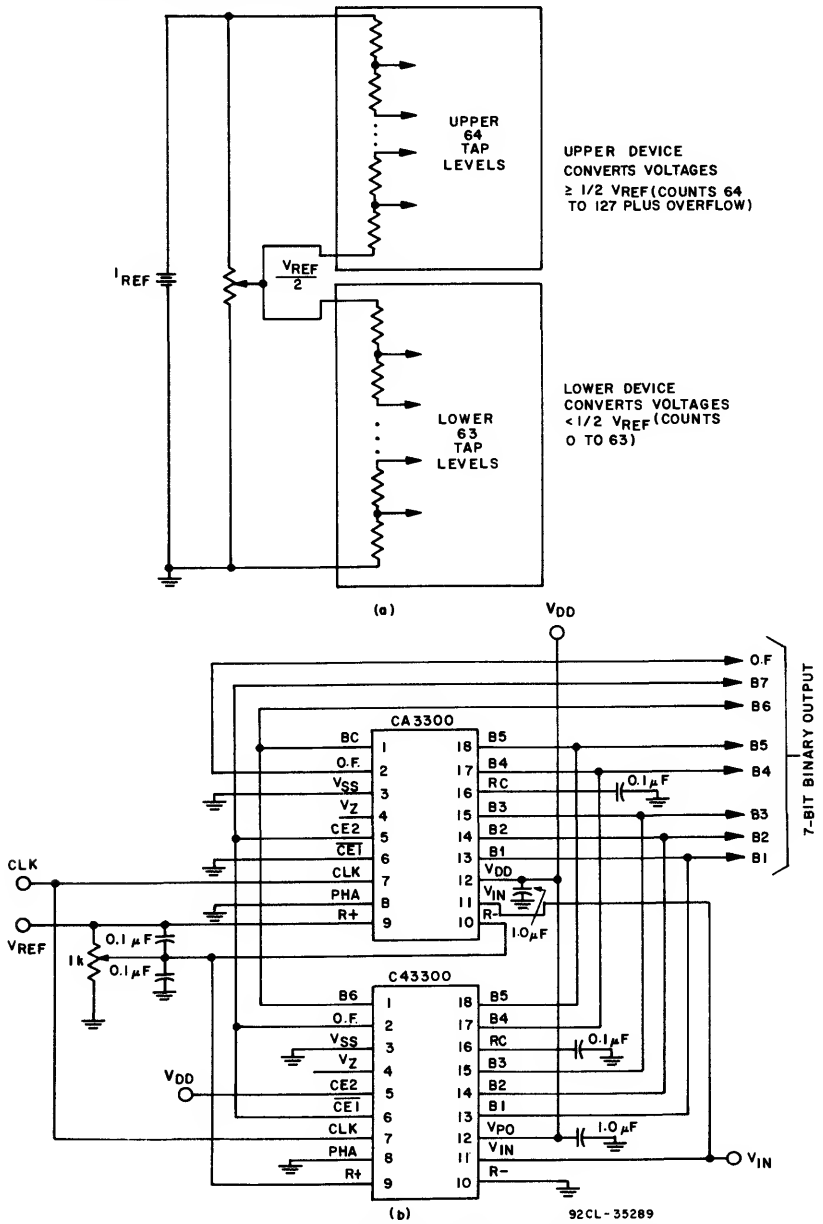


Fig. 4 - Two of the 6-bit flash converters can be stacked in a totem-pole arrangement to provide 7-bit conversions (a). The top device provides the MSB sequence, while the lower device provides the LSBs. This is accomplished by grounding $\overline{CE1}$ on the top device, leaving it perpetually open, and using the overflow bit to sequence $\overline{CE1}$ on the bottom device (b).

The CA3300 has a wide input-voltage working range—from 2.5 V up to the supply voltage. Even so, many signals will require amplification or attenuation and/or dc shifting (for negative voltages). Special consideration will have to be given to the signal amplifier's slew rate, output current, and settling time. For a V_{PP} of 5 V and an analog input frequency of 4 MHz, the minimum slew rate needed to track an ac signal is found by:

$$\text{Slew rate} = V_{PP} \times \pi \times \text{freq.}$$
$$= 5\pi \times 4 \times 10^6$$
$$= 62.8\ V/\mu s.$$

Given the slew rate and an effective capacitance load of 100 pF, the minimum output currents needed from the amplifier are found by:

$$\frac{dv}{dt} = \frac{\text{Output current}}{\text{capacitor load}}$$
$$= I/C$$

Therefore, I_{min} = Slew rate x C
$$= (62.8 \times 10^6) \times (100 \times 10^{-12})$$
$$= 6.28\ mA$$

When the amplifier is converting transient events, its settling time should occur within one clock cycle. Normally, settling to within 0.5% will represent an error of less than 1/3 LSB. With a single-pole rolloff of 6 dB per octave for an amplifier, 0.5% settling is obtained within 5.5 x time constant. That is, the amplifier's unity-gain bandwidth should be at least 5.5 times the clock frequency; for a 15-MHz clock rate, that would be 82.5 MHz.

To obtain 7-bit resolution, two CA3300s can be wired together. Necessary components include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls, all of which are available on the CA3300.

The first step in connecting a 7-bit circuit is to "totem-pole" the ladder networks, as illustrated in Fig. 5. Since the absolute resistance value of each ladder may vary a bit, external trim of the midreference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from

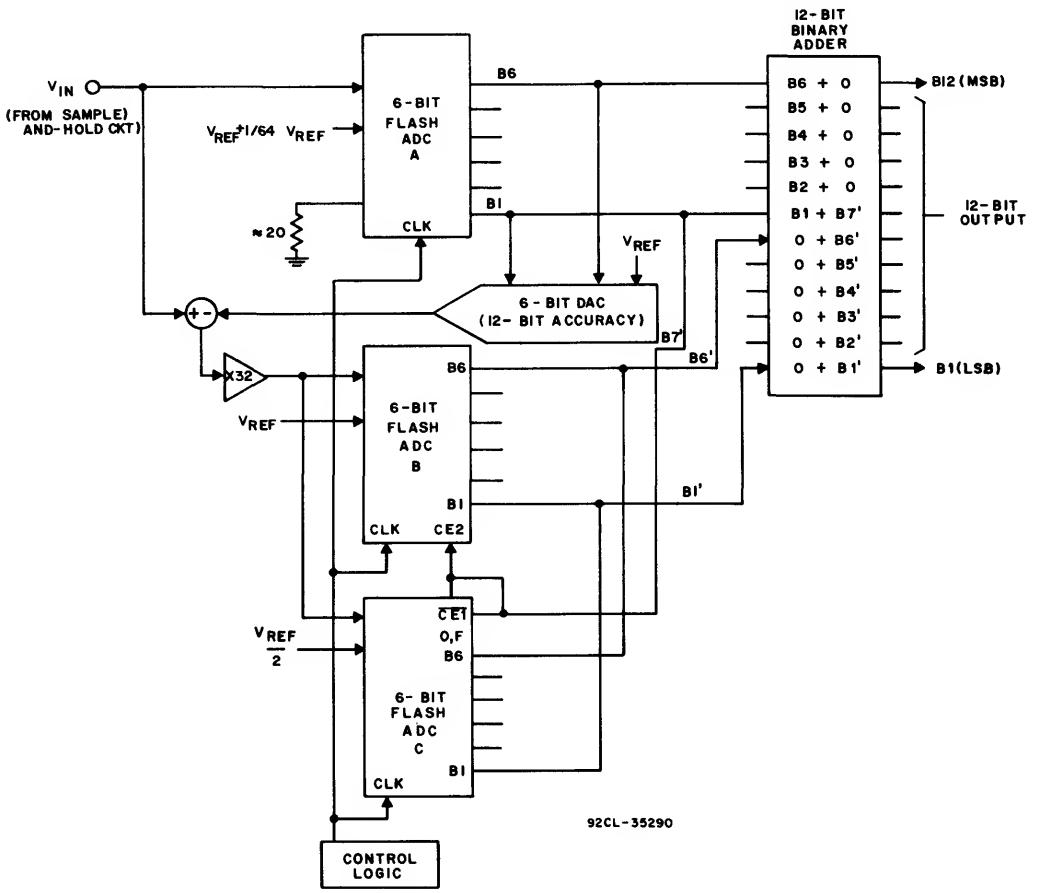


Fig. 5 - Circuit diagram of a high-speed 12-bit A/D converter.

the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the $\overline{CE2}$ control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit A/D converter is shown in Fig. 4(b).

To obtain 8 to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits, three A/D converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Fig. 5. In the feed-forward conversion method, converter A does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a 20-ohm resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, the first CA3300 will require a 6.5-V reference.

RCA CA3210 Horizontal, Vertical and Regulator Control Integrated Circuit

A. R. Balaban, S. A. Steckler, R. Fernsler

RCA Laboratories, Princeton, N.J. 08540

The RCA CA3210 deflection integrated circuit generates horizontal and vertical drive signals, generates the control signal for the receiver's voltage regulator, regulates the IC supply, controls IC and receiver startup, corrects for VCR skew error, and preamplifies the vertical scan signal. A triggered pulse width circuit generates a constant duration horizontal drive output independent of external RC components. Combined integrated injection logic and bipolar technology is used to implement all digital and analog functions on a 10 square millimeter chip.

Circuit Description

The automatic frequency and phase control loop used for television horizontal line synchronization is an ideal clock source for a vertical countdown system. The frequency and phase stability of the properly applied line-derived clock results in improved interlace and eliminates the vertical hold control. Line-synchronized signals are also presently used for the discrete generation of control signals for SCR or transistor-based power supply regulators. Combining the horizontal, vertical, and regulator functions on a single monolithic IC chip takes advantage of their commonality and eliminates over 70 components in the related circuits. Specifically, RCA CA3210 deflection processor shown in Fig. 1 performs the following functions: a) generates horizontal and vertical drive signals which are phase-locked to the video derived sync; b) generates the control signal for the receiver's voltage regulator; c) regulates the IC supply; d) controls the IC and receiver startup; e) corrects for VCR skew error; and f) preamplifies the vertical scan signal. Combined integrated injection logic and bipolar technology is used to implement all digital and analog functions. The 24-pin integrated circuit measures 10 square millimeters and typically dissipates 220 milliwatts including the shunt regulator power.

Horizontal Circuits

Fig. 2 is a block diagram of the horizontal system. Two phase-locked loops accommodate the conflicting bandwidth requirements of the deflection and synchronizing circuits. Good noise performance requires narrow bandwidth, but wide bandwidth is required to minimize horizontal output delay variations. This two-loop approach separates the horizontal output device circuitry from the synchronizing loop, so the two bandwidths can be independently optimized. The first loop consists of a phase detector, compensation filter, voltage-controlled oscillator, synchronous frequency divider, frequency selector and controller. In the phase detector (Fig. 3), a horizontal-rate square wave at B is sampled during the sync interval. The filtered output is proportional to the phase difference of the two signals and is used to control the 16 fH oscillator to maintain synchronization. The phase detector is keyed on when the sync input is high, causing Q1 to saturate and Q2

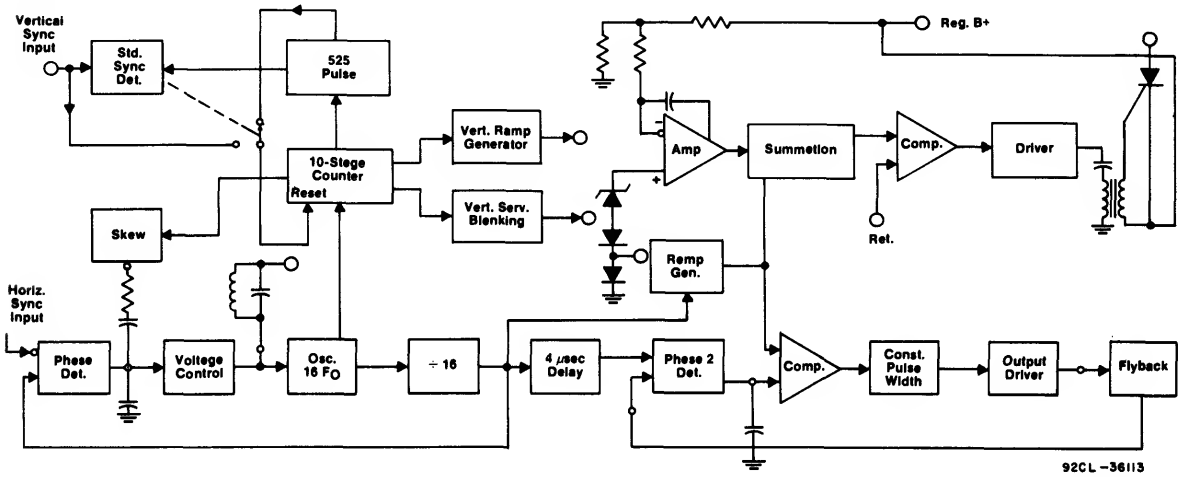


Fig. 1 - RCA CA3210 block diagram.

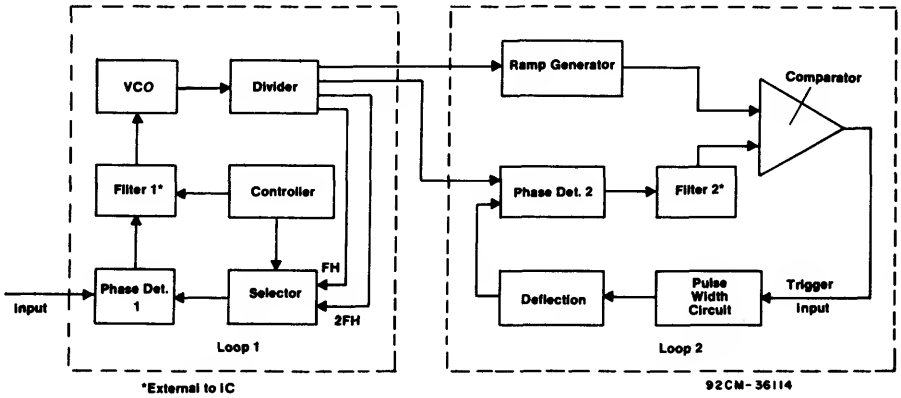


Fig. 2 - Horizontal system block diagram.

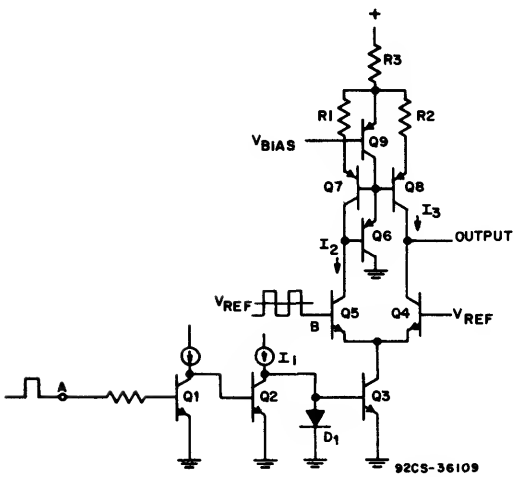


Fig. 3 - Phase Detector I circuit.

to be nonconductive. Current I1 is replicated at the collector of Q3 by the matching of D1 with Q3. If signal B is low, current flows through Q4 and sinks output current. If signal B is high, current flows through Q5 to the source mirror Q6, Q7, Q8, Q9, R1, R2, R3. To minimize current errors through the mirror, current source Q9 is forced off when Q5 is conductive and the mirror enabled, and Q9 is turned on when Q4 is conductive and the mirror disabled. When Q5 is on, currents I2 and I3 flow through summing resistor R3, reverse biasing the base-to-emitter junction of Q9. When I2 decreases to zero, the voltage at the emitter of Q9 changes in the direction that turns Q9 on. The output of Phase Detector 1 drives the voltage-controlled oscillator after passing through Filter 1 (Fig. 2). Fig. 4 is the block diagram of the voltage-controlled oscillator. The oscillator's center frequency is determined by the parallel-tuned circuit, and amplifier A1 provides the regenerative gain in the feedback loop. The output of A1 feeds a 90-degree phase shifter, and then a splitter that produces two components PH1 and PH2 that are 180 degrees out of phase with each other. PH1 and PH2 are fed through gain-controlled amplifiers A2 and A3 to a summing point and then back to the tank circuit. Depending on which phase of the summed signal is fed back to the tank, the tank is paralleled with an inductive or capacitive impedance. If the parallel impedance is inductive the resonant frequency of the tank will increase, or if it is capacitive, the resonant frequency will be decreased.

The output of the oscillator drives a 4-stage IIL divider circuit, which consists of a ripple counter stage and three synchronous counter stages. The divider generates signals that feed Phase Detector 1 (Fig. 2), the loop 2 circuits, the voltage regulator driver, and the vertical circuitry. Two divider outputs, fH and 2fH, feed the frequency selector circuit. Vertical signals control both the selector circuitry and Filter 1 time constants. During most of the vertical scan time, signal fH is routed to Phase Detector 1, and the Filter 1 time constant is selected for a slow loop 1 response time. For the remaining part of the vertical scan, signal 2fH is fed to Phase Detector 1 and the Filter 1 time constant is selected to give the loop a fast response time. This dual time-constant feature allows the system to phase synchronize rapidly with nonstandard signals generated by equipment such as video cassette recorders. Loop 2 corrects for deflection drive timing variations. Phase Detector 2 generates an error signal which is proportional to the timing difference between the flyback pulse generated in the deflection circuit and the divider output signal fH driving Phase Detector 2. The error signal is filtered and fed into the noninverting input of the comparator. The ramp generator operating at a frequency of fH feeds the other input of the comparator. The comparator output changes when the ramp voltage passes through the DC output level of Filter 2.

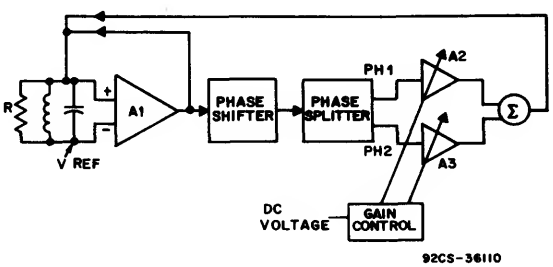


Fig. 4 - Voltage controlled oscillator circuit.

The comparator output drives the constant pulse-width circuit, which in turn drives the deflection circuit. Fig. 5 shows the pulse-width circuit which generates a triggered constant pulse-width signal. When counter output C switches high, the comparator is disabled, inhibiting the input to 'AND' gate A, and switch S1 is closed. At this time the voltage on the capacitor, which was equal to the reference voltage on the comparator's inverting input, starts charging toward the positive rail through the resistor and S1. The capacitor continues to charge for the length of time (T) that counter waveform C is high. At the end of the charging period, the comparator is enabled, switch S1 opens, and the capacitor maintains its present voltage V2. Since V2 is higher than the reference voltage, the output of the comparator is high, enabling 'AND' gate A. When the trigger input switches high, switch S2 is closed initiating the discharge of the capacitor through the resistor and S2. T1, the time it takes the capacitor to discharge from V2 to the reference voltage, is dependent on the charge time T. The discharge interval is therefore constant, dependent primarily on the sync-locked counter interval and independent of the trigger input.

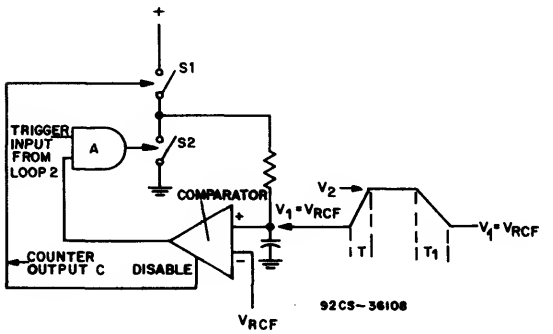


Fig. 5 - Pulse-width circuit.

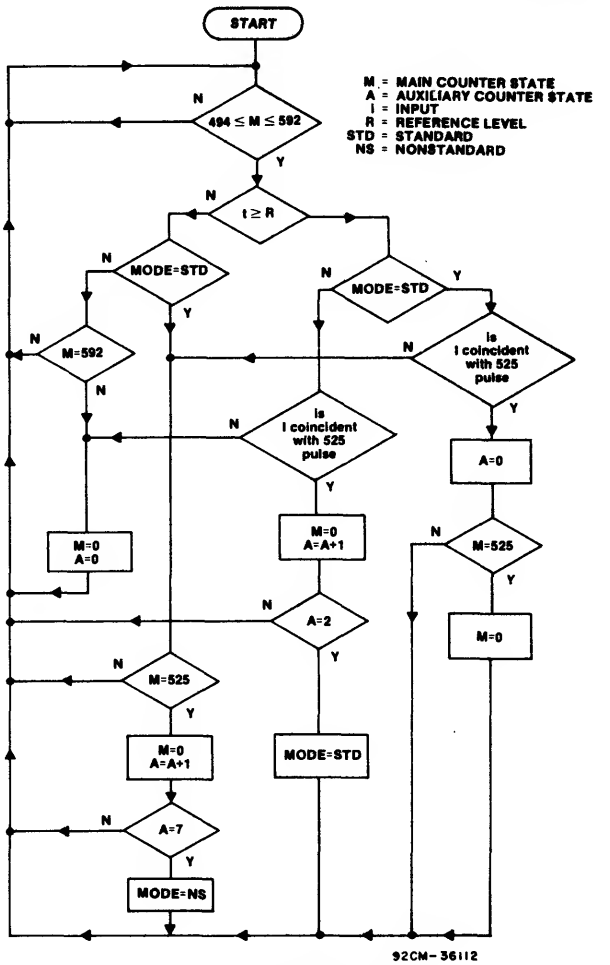


Fig. 6 - Vertical logic flow chart.

Vertical Circuits

The vertical synchronization system uses the integrated input from the sync detector and clock signals from the loop 1 divider to generate a synchronized output for driving the vertical ramp generator. The system will synchronize to both standard NTSC and nonstandard signals. The flow chart in Fig. 6 describes the operation of the integrated circuit logic. All numbers in the chart are counts of the 2fH clock starting at the vertical counter reset pulse. The system looks for sync between the counts of 494 to 592. If there is no input during this interval, the system free runs at a frequency of 53 Hz (2fH/592). In the free-run or nonstandard mode, sync inputs during the 494 to 592 window impulse sync the vertical. The system uses the criteria of two sequential sync pulses coincident with the 525 count to switch into the standard NTSC mode. Just after the system has switched to the standard mode, the input signal must coincide with one out of the next five sequential pulses to remain in the standard mode. Thereafter, it requires one out of seven coincidences to remain in the standard mode. If this criteria is not met the system reverts back to the free-run mode. The vertical countdown circuitry generates control signals used to blank the video, reset the vertical ramp generator, and control the loop 1 filter and selector.

Voltage Regulator Circuits

The voltage regulator system shown in Fig. 7 regulates the receiver's low and high voltage supplies. Resistors R1 and R2 divide the SCR regulated output voltage and apply it to the input of comparator A1. Comparator A1 switches when the magnitudes of its noninverting and inverting inputs are equal. The output of A1 is integrated and summed with the horizontal rate ramp voltage generated in loop 1, and fed into the noninverting input of A2. The output of A2 drives the external SCR gate, turning the device on when the noninverting input of A2 exceeds VR2. When the SCR is conductive, current flows from the power source through the turn-off circuit and SCR to charge the capacitor. The SCR becomes nonconductive when the turn-off circuit tries to reverse the current through the SCR during horizontal retrace. The output voltage is a function of the percentage of the time during each cycle that the SCR is conductive. Since the timing relationship of the horizontal ramp and the turn-off circuit is fixed, varying the DC output of the integrator into the summing circuit varies the time when the noninverting input of A2 equals VR2, changing the conduction time of the SCR. The SCR can conduct for a maximum of 75 percent of the horizontal cycle when the power line voltage is low, or can be totally nonconductive.

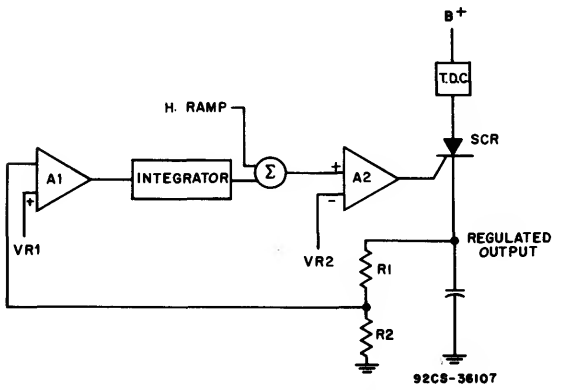


Fig. 7 - Voltage regulator.

Internal Shunt Regulator

The shunt regulator maintains the IC's main supply rail at constant voltage. As the voltage V+ (Fig. 8) increases from zero, the zener voltage eventually becomes conductive, and current flows through R1, R2 and R3. As the voltage across R2 increases, transistor Q1 becomes conductive, maintaining a fixed voltage between the collector and emitter of Q1. Increasing voltage V+ still further increases the voltage across resistor R3, eventually turning on Q2. At this point, voltage V+ becomes regulated due to the varying conduction of shunt transistor Q2. This is shown as voltage V3 in Fig. 10.

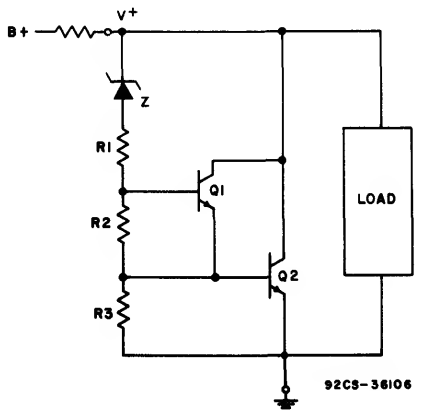


Fig. 8 - Shunt regulator.

Startup Circuit

The startup circuit shown in Fig. 9 prevents the integrated circuit from operating until the chip-supply voltage has reached 8 volts. After the circuit starts, should the chip supply decrease to 4 volts, the startup circuit will turn off the IC. As the supply voltage increases to about 0.7 volts, transistors Q1 and Q2 saturate. Node A voltage is now low, transistors Q4, Q5 and Q6 are off, and R3 is effectively in parallel with R2. As the voltage continues to increase to V1 (Fig. 11), the zener diode starts conducting and node B voltage increases until Q3 turns on, regeneratively turning off Q1 and Q2. Now Q7 and R5 conduct, turning on transistors Q4 through Q12 and D1 and enabling loads 1, 2 and 3. When Q8 becomes conductive, its emitter voltage increases, turning off Q7. As the supply voltage increases, the zener diode D1 and all transistors except Q1, Q2 and Q7 remain conductive. As the supply voltage decreases, the zener diode eventually becomes nonconductive, but transistor Q3 remains saturated since its base voltage is maintained through resistors R2, R3 and R4. Node B voltage decreases turning off Q3, saturating Q1 and Q2. Node A voltage decreases, regeneratively turning off all the remaining devices when the supply voltage reaches V2. Fig. 10 shows this hysteresis characteristic. This circuit therefore has an upper trip point where loads 1, 2 and 3 are supplied current, and a lower trip point where these same loads are disabled when their current sources are cut off. When the supply voltage is replaced by an energy-storage capacitor and a large value resistor the total combination becomes a relaxation oscillator powering the IC from the capacitor until the horizontally-derived B+ is of sufficient value to power the IC. During the time interval t1 to t2 (Fig. 11) the horizontal predriver and SCR driver switches as current is supplied to all the internal loads. If this is not sufficient time for the voltage to build up on the horizontally-derived B+ supply to power the IC, the internal loads disconnect as previously described, and the capacitor is allowed to charge again. In this sense it is a controlled-dump circuit that is largely independent of line impedance and magnitude, and is tolerant over a wide range of load-current variations.

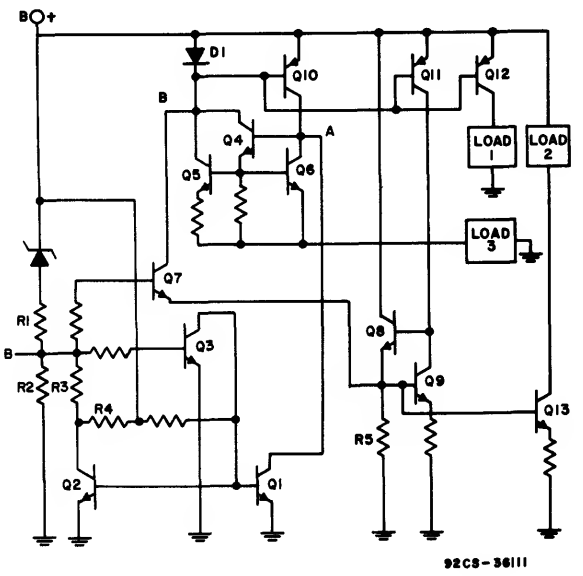


Fig. 9 - Startup circuit.

Acknowledgment

Many individuals in several RCA divisions have contributed to the successful concept-through-product implementation of the deflection IC. The authors particularly thank D. Luz, J. Peer, S. Vinekar, and D. Willis for their constructive ideas, L. Varettoni for his diligent device engineering efforts and C. Plevyak for his meticulous layout and digitization work.

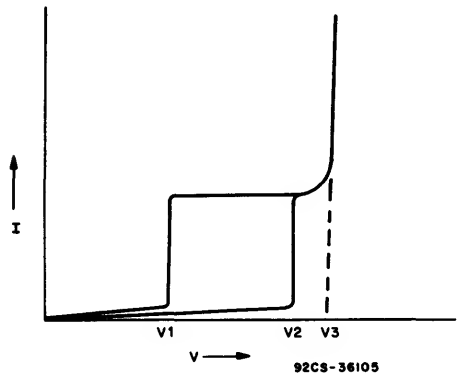


Fig. 10 - Startup hysteresis.

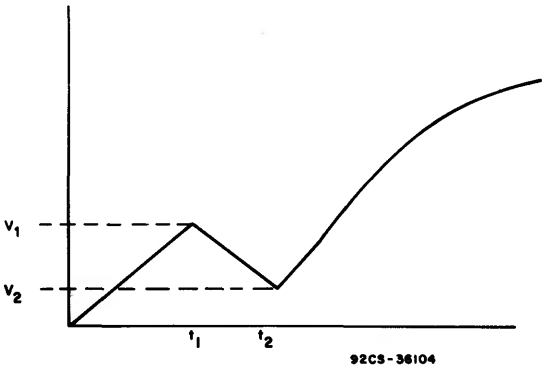


Fig. 11 - Startup retry.

ICAN-7169

Videodisc's Video and Audio Demodulation, Defect Detection and Squelch Control

by G. D. Pyles/B. J. Yorkanis

Video and audio signals for the VideoDisc player are recovered via appropriate demodulation of FM carriers. The integrated circuit, RCA CA3215, designed to perform the demodulation also performs several other functions essential to the performance of the VideoDisc player. Detection of defects in the FM carrier, defect-pulse generation, carrier recognition, squelch logic, and baseband-signal amplification are all achieved by one 16-pin IC and peripheral components (Fig. 1). The device was specifically designed for application in the VideoDisc player and, as such, it efficiently replaces extensive discrete circuits.

Audio and video baseband signals are recorded on the disc as FM modulation of carriers at 716 kHz (mono) and approximately 5 MHz, respectively. The audio channel is rather straightforward — 716-kHz carrier, maximum deviation ±50 kHz, audio bandwidth of 20 Hz to 15 kHz with 75μs pre-emphasis. The video channel is more complex in description — sync tip (-40 IRE) is 4.3 MHz, blanking (0 IRE) is 4.87 MHz, black level (7.5 IRE) is 5.0 MHz, white level (100 IRE) is 6.3 MHz, and video bandwidth is 3 MHz with luminance pre-emphasis (maximum of 21 dB at 3 MHz). Deviation clip levels are 3.9 and 6.9 MHz (-66, +144 IRE). Figure 2 is a spectrum representation of these signal and parameter specifications.

Despite the gross differences between the video and audio signals, the CA3215 custom-designed integrated circuit for use in the VideoDisc player satisfactorily fulfills both applications.

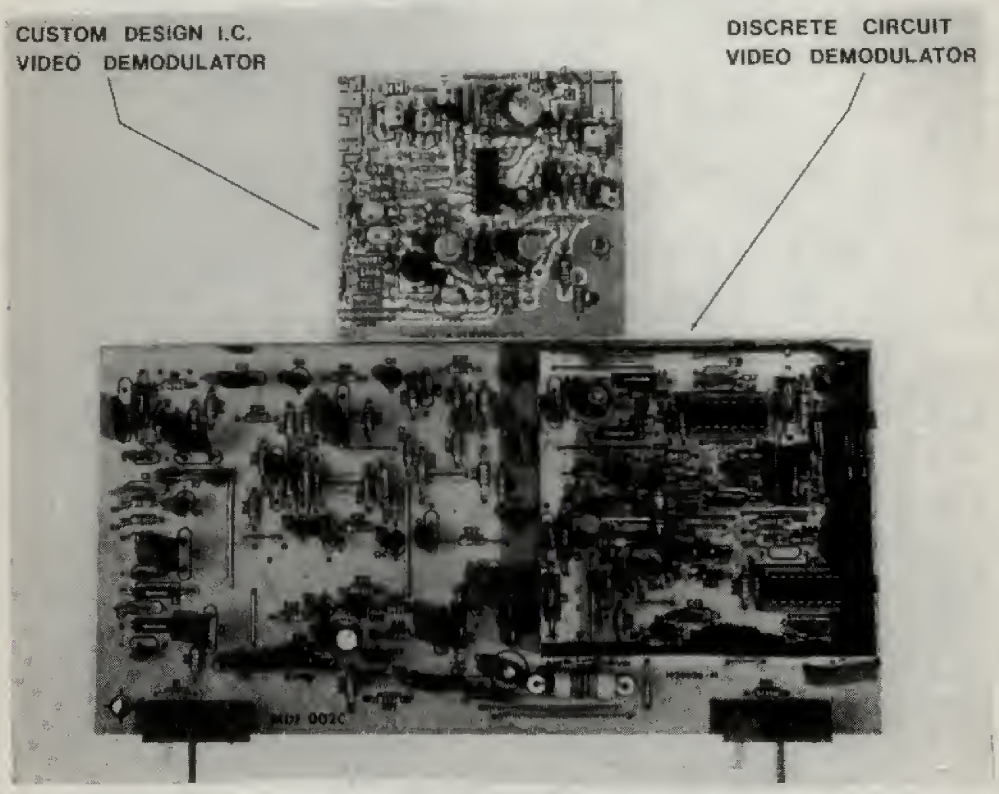


Fig. 1. RCA CA3215 Custom IC and discrete circuit equivalent for video demodulation. The RCA CA3215 custom-designed integrated circuit for the VideoDisc player performs the extensive tasks required for video and audio signal recovery. Significant reduction in size and complexity along with substantial cost reduction make the IC a vital part of the VideoDisc player.

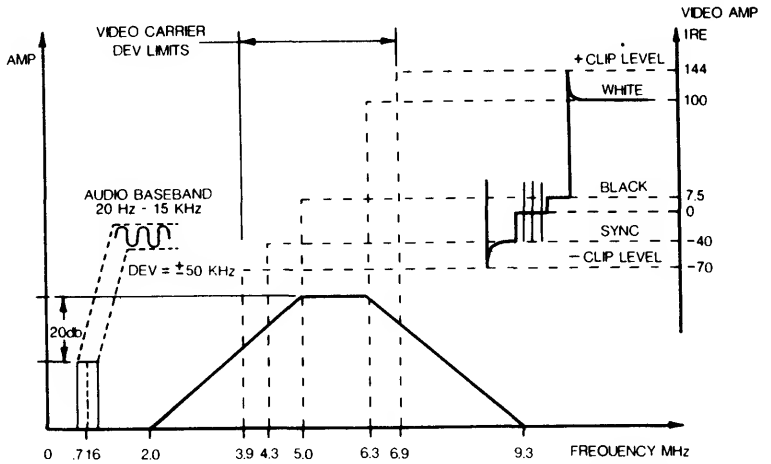


Fig. 2. Frequency spectrum. The signals recovered from the disc contain frequencies extending to nearly 10 MHz. Selective filters input the appropriate FM carriers and sidebands to the video and audio PLL demodulators to recover the baseband information. Note the wide tracking required by the video demodulator due to large overshoots caused by pre-emphasis. These extreme deviations are limited in the modulation process to a maximum change of 3 MHz.

Demodulator

The principle of demodulation for both video and audio signals is a phase-locked loop (PLL). Figure 3 shows the functional blocks as connected in the IC and to the external circuits to perform as a demodulator. The same configuration applies to both video and audio signals with only external components adjusted to appropriately agree with the FM signal parameters and the modulation information, video or audio. The phase detector and voltage-controlled oscillator are fundamental in this PLL demodulator. With the addition of an external loop filter, these two functions in a closed-loop system provide a demodulated output response, namely,

$$H_{(j\omega)} = \frac{K_0 K_d F_{(j\omega)}}{j\omega + K_0 K_d F_{(j\omega)}} \qquad (1)$$

Where $H_{(j\omega)}$ is the closed-loop output response, $F_{(j\omega)}$ is the loop-filter response, K_0 is the voltage-controlled-oscillator (VCO) conversion gain and K_d is the phase-detector conversion gain. The latter two are significant constants determined by circuits designed internally in the IC. The design intricacies are beyond the scope of this article but a general description of performance properties enhancing the application in the VideoDisc player is appropriate.

The phase detector is a multiplier type. A doubly balanced construction provides good cancellation of the two input signals (FM signal and VCO reference) in the output. This is especially important in the video demodulation application where the upper baseband signal is close to the carrier frequency. The conversion gain (K_d) is designed to avoid saturation but adequate to combine with the VCO conversion gain (K_0) to give an overall loop gain sufficient for design optimization in both applications.

The VCO is a RC-type multivibrator noted for good linearity of voltage-to-frequency conversion and having a wide dynamic range. Again, this is particularly important in the video demodulator application — refer to Fig. 2 and note the required tracking range. The VCO center frequency is set by adjustment of an external timing capacitor. The rate of voltage change (dV_c/dt) across the capacitor, which determines the consequent frequency, relates to the current in the capacitor as

$$I_C = C_C \frac{dV_c}{dt} \qquad (2)$$

where the current, I_C, is controlled by current sources in the multivibrator. The sources are controlled by error voltage from the phase-detector output. The steering of the current by the phase-detector output results in instantaneous frequency control of the VCO to track the input frequency.

The integrated PLL demodulator also has a limiter circuit that precedes the input of the phase detector. The prefiltered FM carrier typically may vary 20 dB in level, but with adequate C/N to provide a good picture or sound. The limiter serves as a gain block with constant level output compensating for the variations, and it provides a constant level input to the phase detector, resulting in a constant phase-detector conversion gain and good AM rejection.

In summary, the fundamental operation of demodulation is as follows. The pre-selected FM carrier inputs to the IC PLL demodulator. A gain-block limiter enhances performance by accepting a large dynamic range of input levels. A doubly balanced phase detector and a voltage-controlled oscillator with wide dynamic range, connected in a closed loop, track the input signal via control of current sources in the multivibrator oscillator that have a linear sensitivity to the averaged phase-detector output error signal. The instantaneous phase error between input signal and VCO is the demodulated output signal. Addition of an external loop filter to the loop gain constants K_0 and K_d provides design flexibility to optimize the PLL response for both video and audio applications.

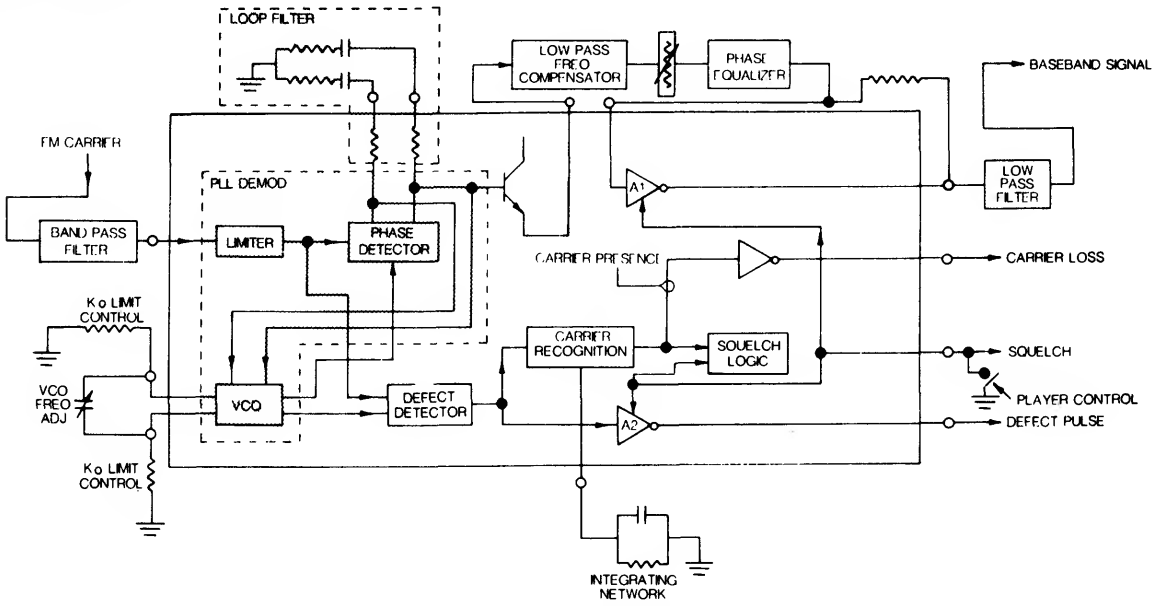


Fig. 3. Functional block diagram of the RCA CA3215 custom-designed IC used as video and audio demodulators in the VideoDisc player.

Defect detection

Similar to the disturbance or interference experienced in a radio or TV receiver, signals from the VideoDisc sometimes exhibit disruptions or distortions in the FM carriers to the demodulation circuits. Unless corrected, the abnormalities, termed defects, result in undesired disturbances in video and/or audio. The VideoDisc player incorporates circuits to detect and correct for defects in video and audio. The correction to video is covered in another article. The audio correction will be covered in this article along with the means for defect detection.

The defect-detection circuit, as part of the IC performing demodulation, is dependent on the performance characteristics of the PLL demodulator. Reference to Fig. 3 shows the two inputs to the defect detector to be the same as those to the phase detector — the limited FM signal and the VCO. The defect-detection mode is essentially monitoring these two inputs to validate that they indeed have the correct relation to demodulate as coherent video or audio information. If not, a defect-gate pulse is generated to enable corrective circuits.

One of the criteria for defect recognition is based on the signal relations in the operation of a PLL demodulator using a phase detector as previously described. The input-output relationship of the phase detector.

$$E_0 = K \cos (\Phi_2 - \Phi_1) \qquad (3)$$

shows the output E_0 to be zero with the input relations at 90° and increasing negatively or positively for differences greater than or less than 90°, respectively. In other words, the PLL closed loop maintains a phase lock with the two signals in quadrature at zero error voltage and will maintain lock with an increasing error voltage ±90° from quadrature. Beyond these extremes, the loop will lose lock and fail to perform properly as a demodulator. The defect-detection circuit is designed to recognize these two extremes and generate a defect-gate pulse upon recognition. Restated, if the input signal exceeds deviation limits or a rate of deviation to cause the PLL to lose lock, a defect-gate pulse is generated.

A second condition causing defect-pulse generation is momentary loss of the input signal. The limiter output is essentially zero with only the VCO signal present at the defect detector, resulting in a defect-gate pulse for this momentary loss. This response holds true for losses as short as one-half cycle of the input frequency.

A third condition causing defect-pulse generation is excessive noise present on the carrier, that is, a poor carrier-to-noise (C/N) ratio. This condition causes a failure mode in the same manner as the first case in that the noise is randomly phase additive to the carrier, and hence causes random excursions that exceed the ±90° degrees relation.

Figure 4 is a graphical presentation and functional response table of the defect-detection circuit as described. The input relations between the VCO and input signal are read in a time-serial manner. Any exceptions to the relation (positive input when the VCO goes positive) result in a defect-gate pulse output.

Audio defect correction

As mentioned, the VideoDisc player incorporates circuits to reduce audio disturbances caused by signal input conditions. These are not part of the demodulator IC but depend on its derived pulse to accomplish correction. The amplified demodulated output is passed through a track-and-hold circuit, which gates off when a defect pulse appears. The gated state causes the output audio to remain at the level prior to disruption. Although this breaks the coherence momentarily, it is normally not detected in complex waveforms. The small discrepancy is much less noticeable than

the large outputs of defects that normally exceed signals greater than 100-percent modulation amplitudes. This track-and-hold technique is very effective in reducing "tick-and-pop" disturbances, especially noted during low-modulation passages.

Squelch logic and recovery of carrier recognition

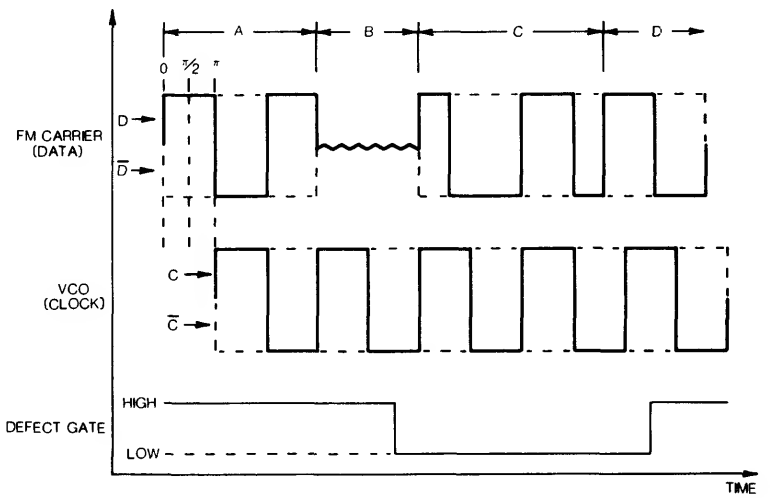
One of the operational conditions of the player is to blank the TV screen and mute audio when the player lever is in the PAUSE or LOAD position, or during initial turn on, and maintain this condition until the lever is returned to PLAY and a good picture and audio are recovered.

This squelched state acts on the amplifiers in the demodulator IC to reduce the gain to zero. The amplifiers are particularly designed to reduce gain with a minimum change in DC quiescent level present in the video or audio signal. The overall result is that the operating quiescent level is maintained, but demodulated output (principally noise) is blocked to avoid spurious inputs to the video or audio processing circuits that follow. Secondly, the defect-gate pulse is inhibited to avoid a recirculating substitution mode. Thirdly, the video conversion and time-base correction system uses squelch to precondition its servo loop for rapid acquisition.

The state of squelch (true, logic 1 as low; false, logic 0 as high) is determined by logic circuitry from two inputs — carrier recognition and the player's function-control switch. The squelch output port serves as a bidirectional data port. When the player-control switch is closed, this switch closure acts as an input to the squelch-logic circuit to hold its output at a low level. When the switch is open, it allows the output of the squelch logic to be passed to squelch circuitry. Carrier recognition necessary for the logic function is developed by integrating the pulses at the defect-detector output. A high rate exists for no carrier, but this rate becomes low or essentially zero for a good carrier. An external network integrates the pulses and sets a threshold for the rate below which carrier recognition is established. Based on the foregoing, the explanation of the squelch and not-squelch response is as follows.

Assuming a condition of play, the logic circuit and memory are set in a condition to respond only to the simultaneous presence (logical product) of forced squelch (switch closure) and loss of carrier. Squelch is begun by a user operation that closes a control switch and pulls squelch low. Simultaneously, the stylus lifts from the disc, causing loss of carrier. The flip-flop sets and conditions the logic circuit to now respond only to the inclusive logical sum of two variables — recovery of carrier and squelch. The latter (squelch) is read as false, due to the previously set condition of the flip-flop.

Return to play requires a user command, which releases the control switch that initiates squelch. With the opening of this switch, the stylus drops to the disc but squelch is maintained by the latched state that has been set by the flip-flop. This latched state inputs to the logic circuit as



FUNCTIONAL TABLE		
CASE	INPUT RELATION	DEFECT GATE
1.	$\Delta\phi = > 0 < \pi$	HIGH (NO)
2.	$\Delta\phi = \leq 0$	LOW (YES)
3.	$\Delta\phi = \geq \pi$	LOW (YES)
4.	D = 0; C = X	LOW (YES)

Fig. 4. Defect detection. Signal input conditions, A and D, are normal input-phase ($\Delta\phi$) relations between VCO and input signal. Case 1 shows the functional response of no defect gate. Condition B, Case 4, is a loss of input signal — note that a defect gate is generated. Condition C goes through relations of Case 2 and 3 after signal is recovered, holding the defect-gate low. Note the input half-cycle (D and $\overline{D}$) is read for each half-cycle of clock (C and $\overline{C}$). A generated defect starts one clock half-cycle late, but this is compensated for by group delay in baseband phase-corrector circuits.

squelch being false (logic 0, high). Carrier is recovered when the stylus contacts the disc, hence the logic sees carrier recognition as true. This changes the output state to "not squelch" and play resumes. This resets the flip-flop and conditions the memory and logic circuits to respond only to the logical product of forced squelch and loss of carrier.

Design considerations

The design considerations for the demodulators logically had to start with the modulation characteristics of the FM signals, stated earlier. Secondly, the C/N ratio of the signals from the disc had to be considered and they are reasonably predictable. These two fundamental considerations suggest an appropriate noise bandwidth for the demodulation loop. In both cases, video and audio, this becomes the determining factor establishing the loop-tracking performance, S/N ratio, and loop response best suited for the application. Optimization of each of these required compromises yielding the overall best performance for each application. We designed each demodulator within constraints by selection of loop-gain constants (VCO and phase detector) and the PLL loop filter.

The video demodulator was chosen to be a first-order loop due to the wide tracking requirements (recall that encoded signal clip levels are 3.9 to 6.0 MHz) and large baseband bandwidth (3 MHz). The gain constants, as designed in the IC, are adjusted down by external resistors (see Fig. 3, K_o limit control) to give tracking performance slightly greater than deviation requirements, but limited to a range that will enhance defect detection — recall that defect detection results when the loop fails to track. Also, a good S/N ratio and response were achieved by this loop.

The audio demodulator was chosen to be a second-order type-two loop. Within the modulation parameters and input signal C/N ratio constraints, this type of demodulation loop allowed a choice of loop-filter design, in combination with the conversion gain, yielding a minimally compromised performance.

A New Low Level Luminance Processing System

J. P. Bingham, RCA Laboratories,
M. N. Norman and R. L. Shanley, RCA Consumer Electronics, Indianapolis,
B. Yorkanis, RCA Consumer Electronics, Somerville

The functions of peaking, gain control, subcarrier removal and black-level clamping which are normally required in consumer color television receivers are typically handled in the low level luminance signal-processing system. A novel design is described here which accomplishes these functions in an optimum manner, and which, in addition, features nonlinear picture quality enhancement as well as variable, phase-corrected peaking.

The RCA Colortrak color television series features many novel and advanced functions. This note will be directed toward explaining the operation and unique aspects of the low level luminance signal-processing subsystem found in this new receiver line.

A block diagram of a color receiver of the Colortrak type is shown in Fig. 1. In the Colortrak luminance signal-processing subsystem, the following functions are performed:

a. Variable, phase-corrected peaking control by DC level.
b. Nonlinear transient compression in the white direction.
c. Regulation by ambient light of chroma and contrast.
d. Contrast control by DC level.
e. Brightness control by DC level.
f. Black-level clamping.
g. Vertical and horizontal blanking.
h. Sync separation.

Most of the active elements of the subsystem have been incorporated into a single low level luminance integrated circuit design; namely, the RCA CA3143 for video input with positive-going sync and the RCA CA3144 for negative-going sync. Integration of the subsystem has permitted an order of signal-processing sophistication which has heretofore been too costly for consumer applications.

Peaking

An important function of the complete Colortrak signal-processing system is the provision of an overall optimum video transient response, as seen at the kinescope.

Many experiments described in the literature have indicated that an optimum overall video-transmission system transient response should possess a single preshoot and equal overshoot,[1] and should be free of all other precursors and following ringing. In addition, the overshoot amplitude should be in the vicinity of 10-20% of the transition size, as shown in Fig. 2.

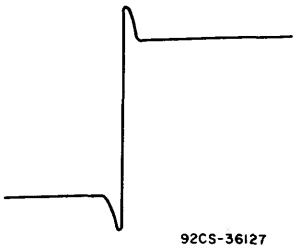


Fig. 2 - Desirable transient response.

If we further assume the requirement of a 3.58-MHz trap, and if, in addition, assume that the receiver response is the determining factor influencing the total transmission system transient response, we are led, by Fourier transform theory, to the receiver amplitude characteristic shown in Fig. 3. An overall flat envelope delay response is also necessary to preserve transient symmetry.

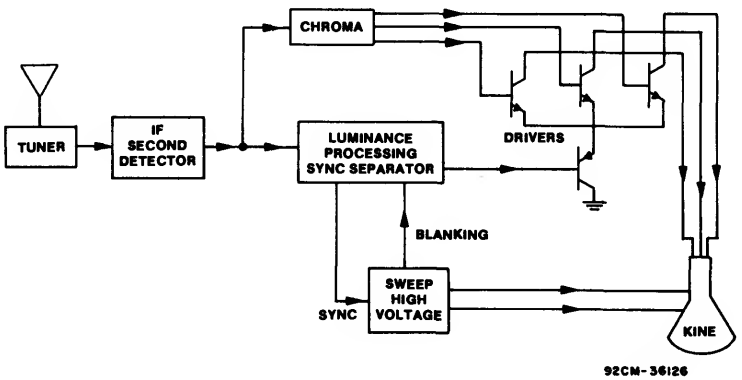


Fig. 1 - Receiver diagram.

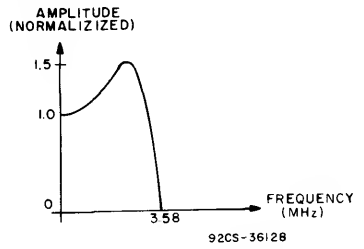


Fig. 3 - Ideal receiver amplitude response.

In a receiver which is to work well with signals "enhanced" at the transmitter, as well as with signals contaminated by noise and ghosts, it has been found desirable to incorporate a viewer-adjustable peaking control. Again, to preserve average transient symmetry, it is desirable to maintain a linear phase response over the peaking control range. The family of amplitude characteristics of Fig. 4 illustrates the receiver-response range which accomplishes this end, and which minimizes any tendency towards "ringing" on edges.

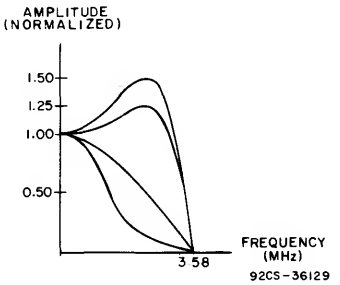


Fig. 4 - Receiver response range.

In the Colortrak line, this range is realized by tailoring the total receiver response, excluding the peaking circuitry, to a nominally cosinusoidal shape with a null at 3.58 MHz, as in Fig. 5. The peaking circuitry adds or subtracts complementary high passed signals, and thus permits a response adjustable over the range shown. These complementary high passed signals are obtained through the use of transversal, or tapped delay line, filter.

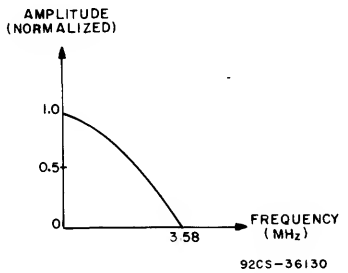


Fig. 5 - Cosinusoidal frequency response.

A block diagram for one possible transversal filter system implementation is shown in Fig. 6. Here, the input signal is delayed in turn by two equal delay elements T_1. The center tap signal is mixed with inverted half-weighted outer tap signals to form the high frequency signal. This process can be understood by recalling that,

if e_o, e_{-1}, and e_{+1} are the Fourier transforms of the signals at the center tap, input, and last tap, respectively, then

$$e_{-1}=e_o\, e^{jwT}$$

and $$e_{+1}=e_o e^{-jwT}$$

so that $$e_H=e_o\,(1-\tfrac{1}{2}\,(e^{jwT}+e^{-jwT}))$$

or $$e_H=e_o\,(1-\cos wT)$$

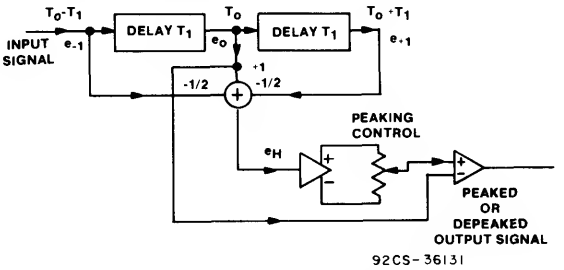


Fig. 6 - Simple transversal filter.

e_H is thus the Fourier transform of the signal formed by passing e_o through a linear phase filter with the frequency response shown in Fig. 7. This high frequency signal is then either added or subtracted from the center-tapped signal to form the peaked or de-peaked output signal.

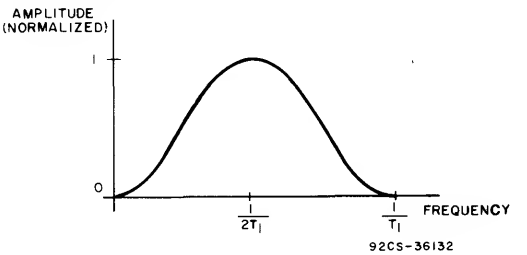


Fig. 7 - Hi-pass filter response.

A system which avoids the need for dual-polarity high frequency signal is shown in Fig. 8. Just as the high passed signal e_H was obtained by subtractively matrixing e_o, e_{-1}, and e_{+1}, a low passed signal e_L is formed by adding the signals e_{-1}, e_o, and e_1. e_H here is formed as before. An

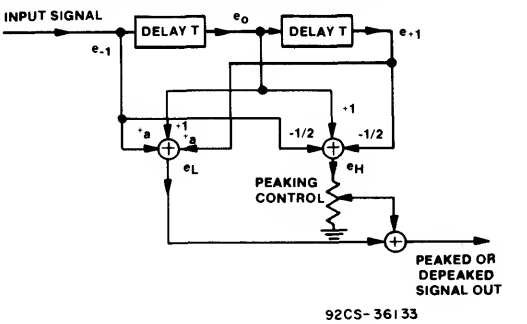


Fig. 8 - Transversal filter system.

adjustable amount of e_H can be added to e_L to yield an output signal which is rolled off, flat, or peaked. This basic approach to variable peaking is used in the Colortrak system, and can be implemented as shown in Fig. 9.

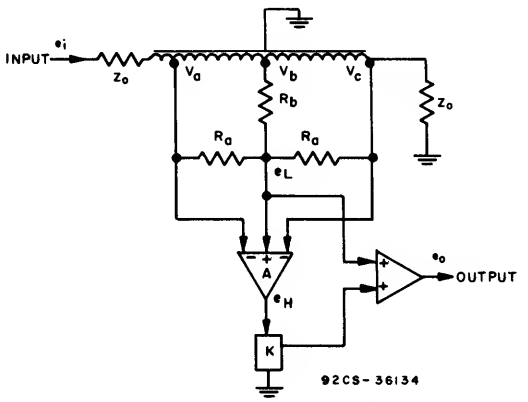


Fig. 9 - Luminance peaker system.

As illustrated, the usual luminance wire-wound delay line can be fitted with two extra taps, so that signals V_a and V_c, symmetrically disposed about the main signal V_b, are available. V_a, V_b, and V_c are linearly added to form e_L. e_H is formed at the output of adder-inverter A. K is an adjustable gain control which can be used to vary the amount of peaking. The transfer characteristics of this system are derived in Appendix I.

Nonlinear Transient Compression

Our linear phase transversal filter peaker creates symmetrical preshoots and overshoots around smooth and symmetrical input transients. This peaking is accomplished at a point in the video transmission system between gamma correction at the transmitter and complementary nonlinear expansion in the kinescope. Because the kinescope has an essentially square-law transfer characteristic, large symmetrical input transients will produce asymmetric transients in beam current and light output. This effect is shown in Fig. 10. Besides creating an unnatural, overpeaked, and asymmetric effect on large signal swings, this effect is undesirable because it produces large peak current flow, and consequent broadened electron beam profile in the kinescope. The broadened beam profile tends to simulate the effect of a low pass filter, and thus counteracts the desired benefits of peaking.

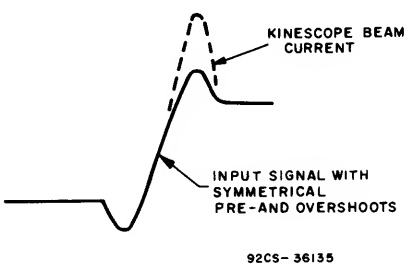


Fig. 10 - Effect of gamma upon overshoot magnitude.

These negative effects have been minimized in the Colortrak system by incorporating nonlinear diode elements in the transversal filter matrixing circuitry, as shown in Fig. 11. Without the diodes, Fig. 11 is identical to the peaker system we have already seen in Fig. 9. That is, a low passed signal e_L would be formed by linearly adding the contributions from all delay line taps, while the high passed signal e_H is formed by subtracting the outer tap signals from e_L.

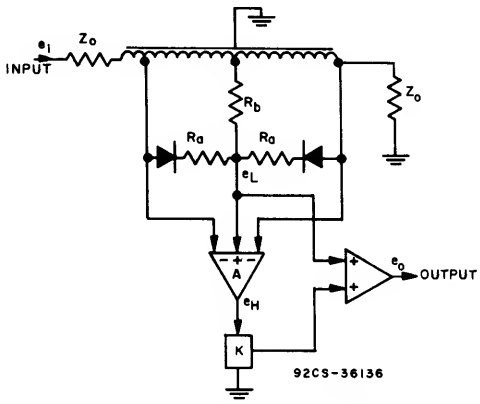


Fig. 11 - ColorTrak peaker system.

With the addition of the diodes, and for small-signal amplitude differences between taps, no linear addition of outer tap signals to e_L occurs. Thus, e_L becomes a wideband signal, and e_H is formed as explained previously. For larger amplitude signal differences between taps, the diodes conduct, e_L is effectively low passed, and the amplitude of e_H is reduced. With proper diode polarity, the magnitudes of white-going preshoots and overshoots are restricted, and matching between signal-processing system and kinescope is achieved.

The choice of an appropriate diode type is important. Typically, the turn-off time of the diode should be at least an order of magnitude less than the delay line tap spacing. Further, the volt-ampere characteristic of the diode should be matched with the peak-to-peak signal in order to complement the nonlinear kinescope transfer characteristic. This effect is best accomplished with a soft knee, which increases compression gradually with transition amplitude.

Control Action

Along with achieving a suitable overall transient response, an important function of the low level signal-processing system is the provision of control functions which permit the viewer to adjust brightness and contrast to suit ambient conditions. In the Colortrak line, regulation of contrast and color saturation is accomplished by varying the dc bias applied to variable gain stages in the luminance and chrominance processing IC's. The attenuation curves of these stages are shown in Fig. 12.

Because the curves for these two functions are identical, it is possible to interconnect the contrast and chroma control circuits as shown in Fig. 13, in a way which minimizes the need to reset chroma after every contrast control adjustment. The luminance control dc bias is obtained from the wiper of the 6.5K luminance preset pot, while the chroma control dc bias is obtained from the chroma preference pot wiper. The preset pot is factory adjusted for proper signal level-out of the low level processing IC, while the contrast

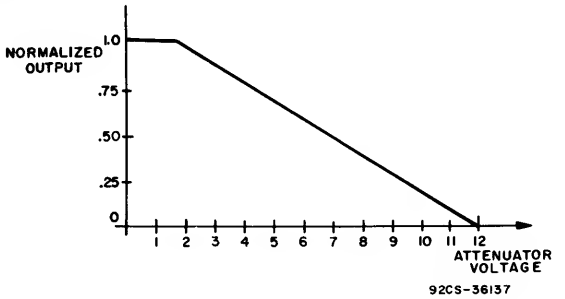


Fig. 12 - Luminance and chrominance attenuators.

and chroma preference pots are viewer-adjustable. Thus, adjustment of the viewer contrast pot varies both chroma and luminance control voltages and causes color saturation to match luminance level, while adjustment of the chroma control has no interactive effect on the contrast setting.

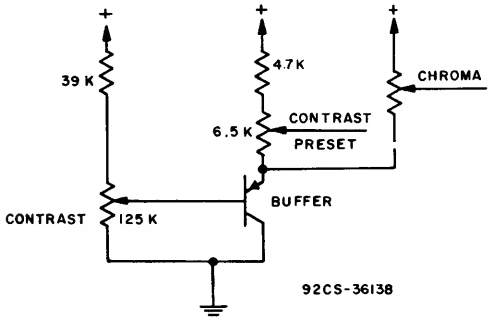


Fig. 13 - ColorTrak control circuit.

To permit good color tracking, and to eliminate saturation dependency on scene content, the receiver must have good dc gain and stability. This desirable characteristic is achieved in the Colortrak line through the application of clamping during the front and back porches of the blanking interval. The circuit of Fig. 14 is used to inhibit clamping at all other times. In this instance, the inhibit mode is activated when the clamp inhibit transistor is saturated. This takes place during active scan, when the negative horizontal retrace pulse line goes positive, or during a sync pulse interval, when the sync pulse line also goes positive.

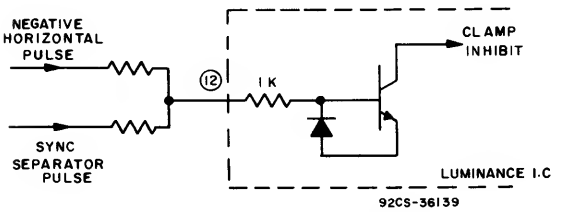


Fig. 14 - Clamp inhibit circuit.

Ambient Light Sensing

An additional feature of Colortrak provides automatic regulation by ambient light of contrast and chroma settings. The circuit shown in Fig. 15 illustrates how a simple ambient light-compensation circuit is used to modify the action of the contrast and chroma controls.

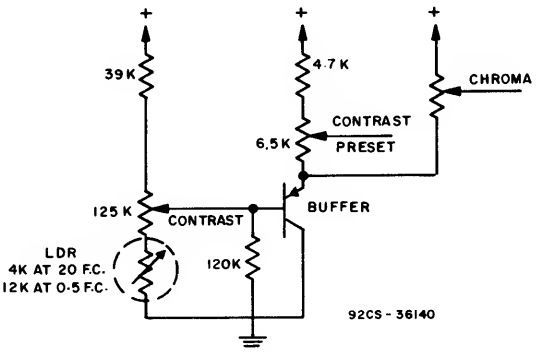


Fig. 15 - Ambient light compensation.

The Integrated Circuit

For completeness, the block diagram of the RCA CA3143/CA3144 low level luminance processing integrated circuit is shown in Fig. 16. In this system, the input signals from the delay line taps are fed to pins 1, 2 and 3. e_H, formed at the output of the subtraction amplifier, is varied in amplitude via the external peaking control, and added to e_L to form the peaked signal e_o. e_o is varied in level via the external contrast control, and, after ac coupling through pins 4 and 6, is clamped on front and back porches. The signal is then inverted, biased via the external brightness control, and then buffered to pin 7, the output terminal. Final matrixing with color difference signals to form R, G, and B signals is accomplished in the kine driver stages.

Summary

In summary, the RCA Colortrak luminance processing system achieved, almost ideally, the traditional functions of peaking, contrast control, dc restoration, and retrace blanking. In addition, new functions have been introduced, such as nonlinear transient compression and ambient light tracking, which provide a picture quality which until recently could only be achieved with a high order of system complexity and expense.

The development of the Colortrak luminance system was a combined interdivisional effort of RCA. RCA Laboratories developed the basic peaking concepts, the Solid State Divison built the IC, and the Consumer Electronics Division implemented the total system in a form suitable for the consumer market.

Reference

1. F. F. Brown, "Television: The Subjective Effects of Filter Ringing Transients".
Journal SMPTE, Vol 78, April 59. pp 249-255.

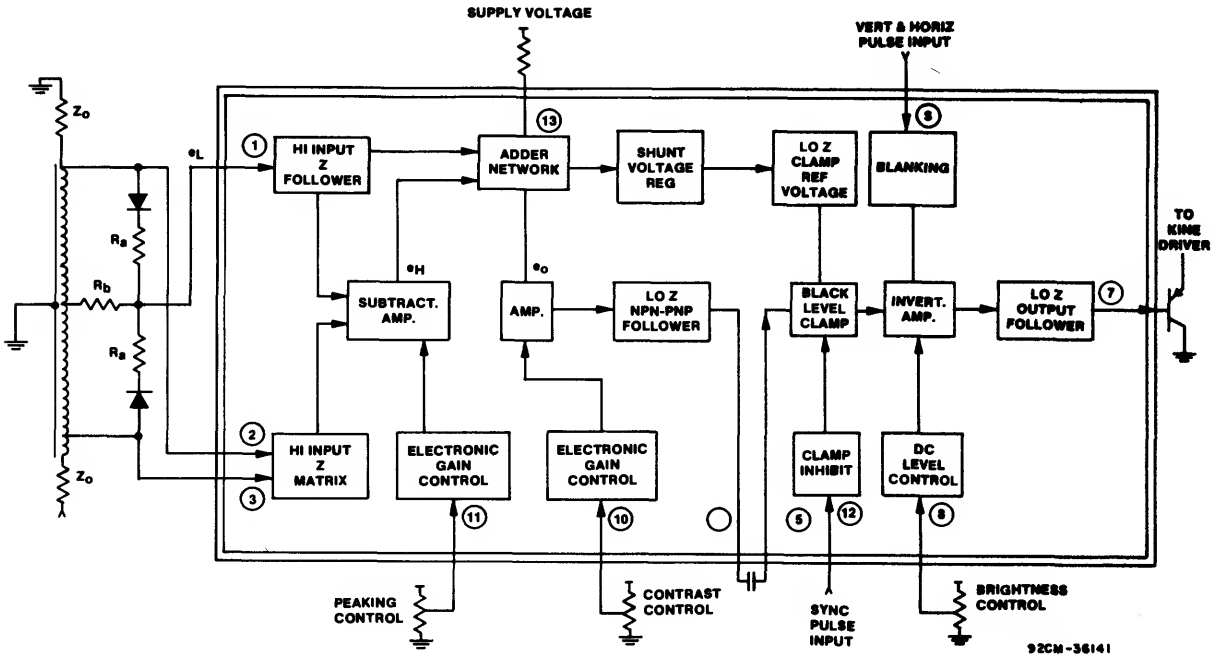


Fig. 16 - Luminance processing integrated circuit.

The variation of the transfer characteristic associated with e_o as a function of K is shown in Fig. 17.

When $K = \frac{2R_b}{R_a}$ the transfer characteristic is flat. When

$$K < \frac{2R_b}{R_a}$$

the transfer characteristic is depeaked at frequency $\frac{1}{2T}$.

When $K > \frac{2R_b}{R_a}$

the transfer characteristic is peaked at frequency $\frac{1}{2T}$.

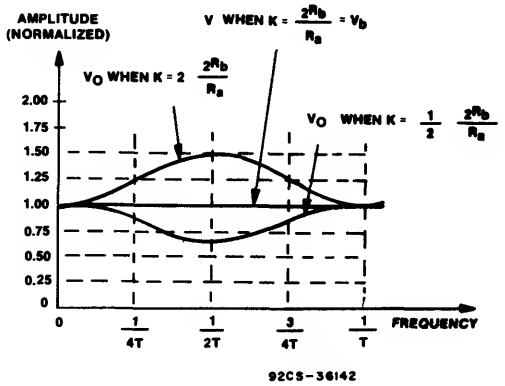


Fig. 17 - Transfer characteristic variation with peaker setting.

Appendix I

Referring to Fig. 9, and assuming

$$R_a, R_b >> Z_o$$

then $$e_L = \tfrac{1}{2}\left(\frac{2R_b}{R_a+2R_b}\right)(V_a+V_c)+\left(\frac{R_a}{R_a+2R_b}\right) V_b$$

and $$e_H = e_L - \frac{(V_a+V_c)}{2}$$

so $$e_o = e_L + Ke_H$$

With the delay line tap spacing of T, the following transfer characteristics are formed:

$$\frac{e_L}{e_i} = \frac{2R_b}{R_a+2R_b}\ \cos wT + \frac{R_a}{R_a+2R_b}$$

$$\frac{e_H}{e_i} = \frac{2R_b}{R_a+2R_b}\cos wT + \frac{R_a}{R_a+2R_b} - \cos wT$$

$$\frac{e_o}{e_i} = \frac{2R_b}{R_a+2R_b}\cos wT + \frac{R_a}{R_a+2R_b} + K\left(\frac{2R_b}{R_a+2R_b}\ \cos wT + \frac{R_a}{R_a+2R_b} - \cos wT\right)$$

The RCA CA1524E Pulse-Width Modulator-Driver for an Electronic Scale

C. P. Salerno - RCA Solid State Division, Somerville, N.J.
P. J. Stabile - RCA Princeton Labs, Princeton, N.J.

The CA1524E pulse-width modulator integrated circuit presently in use in voltage-regulator applications can also be employed as the driving source for an electronic scale. As shown in the block and schematic diagrams of Figs. 1 and 2, half of the output of the CA1524E, Q2, is used in a low-voltage (2.2 volts) switching regulator that drives the LEDs displaying the weight measured. The remaining output stage, Q1, is used as a driver for the sampling plates PL1 and PL2. Since the CA1524E contains a 5-volt internal regulator and is able to operate over a wide voltage range, 8 to 40 volts, a single 9-volt battery is sufficient to power the total system. The two sampling plates, PL1 and PL2, are driven by oppositely phased signals (the frequency is held constant but the duty-cycle may change) from the pulse-width modulator integrated circuit CA1524E. The sensor, S, located between the two plates forms with them an effective divider network of the capacitance-bridge type.

As the plate S is moved, the amount of movement depending on the weight of the object on the scale, a change in capacitance occurs. This change is reflected as a voltage to the ac amplifier, the integrated circuit CA3160. At the null position, the signals for PL1 and PL2, as detected at S, are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A detector of this type is needed because the duty cycle of the sampled waveform is subject to change. The detector signal is filtered further and displayed, by means of the CA3161E and the CA3162E digital readout system, as the weight of the object on the scale.

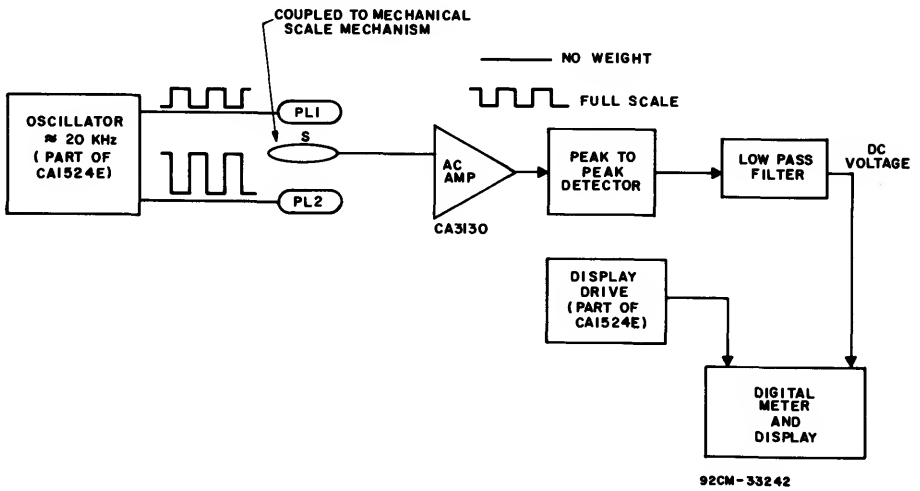


Fig. 1 - Block diagram - digital readout scale circuit.

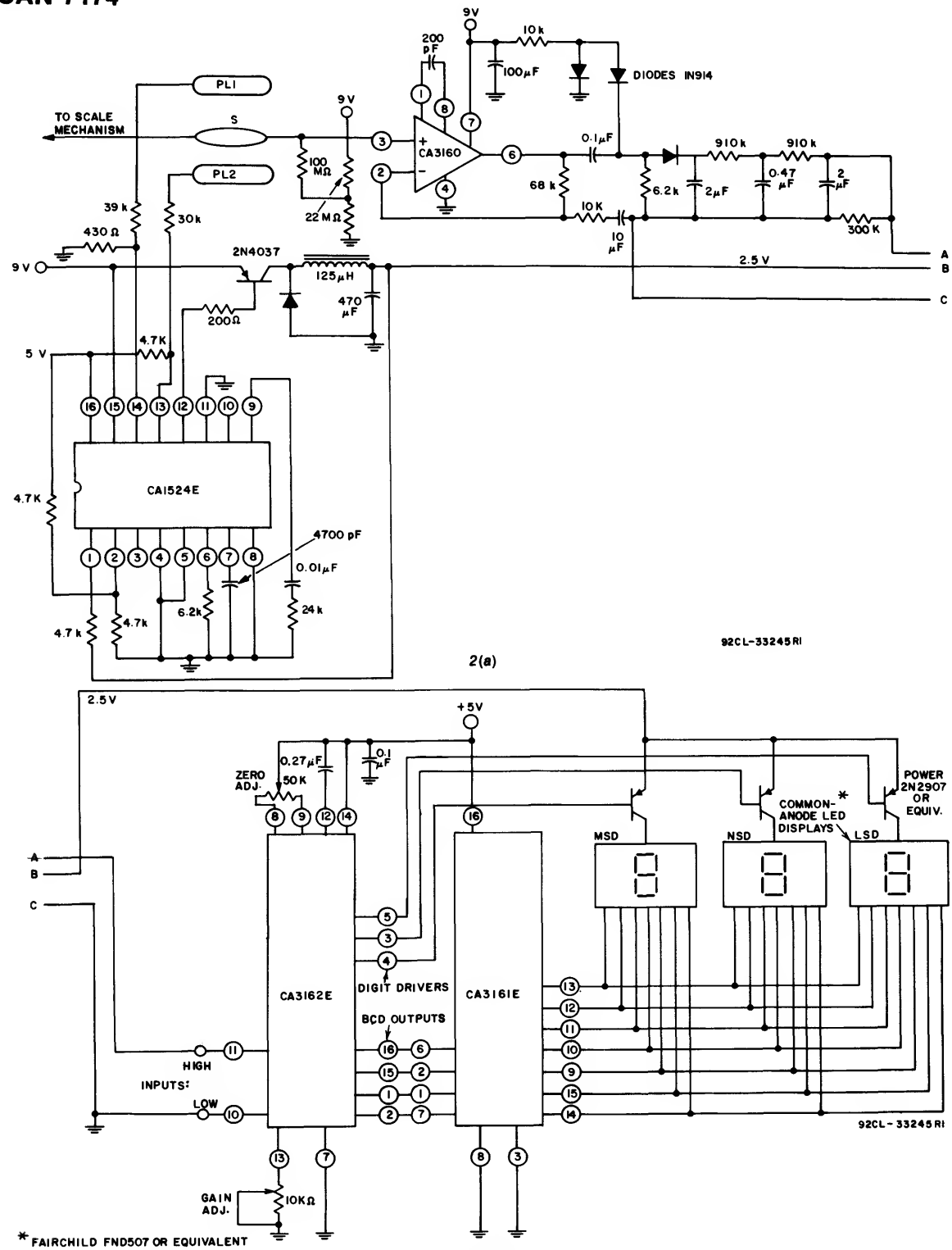


Fig. 2 - Schematic diagram of digital readout scale.

Integrated NTSC Chrominance/Luminance Processor

L.A. Harwood and E.J. Wittman, RCA Labs, Princeton, N.J.
J. Hettiger and R.L. Shanley, RCA Consumer Electronics, Indianapolis, IN

An intensive engineering effort in the past decade produced color TV receivers with a high degree of maturity. Although the price of receivers remained essentially unchanged, their performance and reliability were improved substantially. Among the many improvements in all sections of the receiver are not only those that relate to a better picture quality but also those responsible for reduced energy consumption, the simplified operation of controls, and reduced weight. In this Note attention will be focused on improvements in the chroma/luma area.

A brief historical review is appropriate for a better understanding of the RCA CA3217E integrated circuit developed for this application. Ten years ago vacuum tubes were still used in many color TV receivers, as efforts to fully transistorize receivers proved too costly. At first integrated circuits, primarily in the sound area, were not readily accepted, mainly because of power supply and vacuum tube interface problems.

A major breakthrough for consumer ICs occurred in 1969, with RCA's solid-state color TV receiver. This receiver contained five ICs, which performed key functions in the areas of PIX-IF, AFT, sound IF, chroma processing, and chroma demodulation. Although overall performance improvement was marginal and a substantial number of external components was still required, integrated circuits clearly emerged as the key elements in the batch-manufacture of pretested key components for a color TV receiver.

The major goals in subsequent designs were improvements of performance and reliability, the introduction of new features, and the simplification of manufacturing.

The improvements subsequently achieved[1-3] in the chroma/luma section of the receiver were in the areas of color signal synchronization, automation of controls to minimize the need for frequent adjustments of saturation, hue controls (overload detector, dynamic flesh correction), black-level control, and picture control. To reduce the number of components (ICs and discrete parts) as well as testing time, the chroma circuits performing the chroma processing and chroma demodulation were combined on one chip, the RCA CA3151. This helped simplify manufacturing and also resulted in better performance, since fewer interface problems exist when more functions are combined on one chip.

Similar considerations led to the newly developed RCA CA3217E chroma/luma integrated circuit. In addition to all the functions available in the one-chip chroma, the RCA CA3217E also contains the essential luminance functions. Briefly, it decodes the chrominance signal and produces three color-difference signals which combine internally with the luminance to develop the RGB signals. The chrominance signal is gain controlled by an automatic chroma control (ACC) and overload detector and by a customer-operated saturation control. A separate control tracks the gain of the luma and chroma amplifiers and serves as a customer-operated picture control. The viewer sets the hue by means of a control; an automatic dynamic flesh-correction circuit maintains proper flesh color without noticeably affecting the three primary colors. The luminance peak-to-peak level is set by a previously described picture control; a comparator circuit sets the black level to a potential set by a viewer-operated brightness control. Picture and brightness levels are also controlled by an automatic beam limiter. A signal derived from the kinescope beam current reduces first the picture amplitude to a predetermined level and then operates on the brightness control to prevent excessive drive to the picture tube. The composite video signal is gated by a clamp circuit during the horizontal and vertical retrace intervals to prevent undesired signals from appearing on the screen during those intervals. An externally generated sandcastle signal provides the timing for the burst gating and blanking signals. Technical information for the one-chip chroma/luma processor is summarized in Table I.

Major Functions and Signal Flow

The block diagram of the major functions of the RCA CA3217E and the external components are shown in Fig. 1. The chip was designed to maintain the performance and economy of a single-chip design with the chroma and luminance functions together to provide an integrated circuit with complete video processing.

The chrominance and luminance signals, derived from the composite video signal at the second detector, are applied to terminals 3 and 27, respectively. Both signals must be appropriately filtered, and the luminance signal must be adequately delayed with respect to the chrominance signal.

The composite chrominance signal is amplified in the first chroma amplifier; the gain of this stage is controlled by a servo loop to maintain an essentially constant burst output level. Upon amplification the burst and chrominance signals are separated for further processing.

The burst signal is applied to two synchronous detectors. An in-phase detector (ACC) produces an error signal to control the gain of the first chroma amplifier so as to maintain an essentially constant burst output level. The detected burst signal from the ACC detector passes through a sample-and-hold stage that improves the efficiency and dc stability of the servo loop.

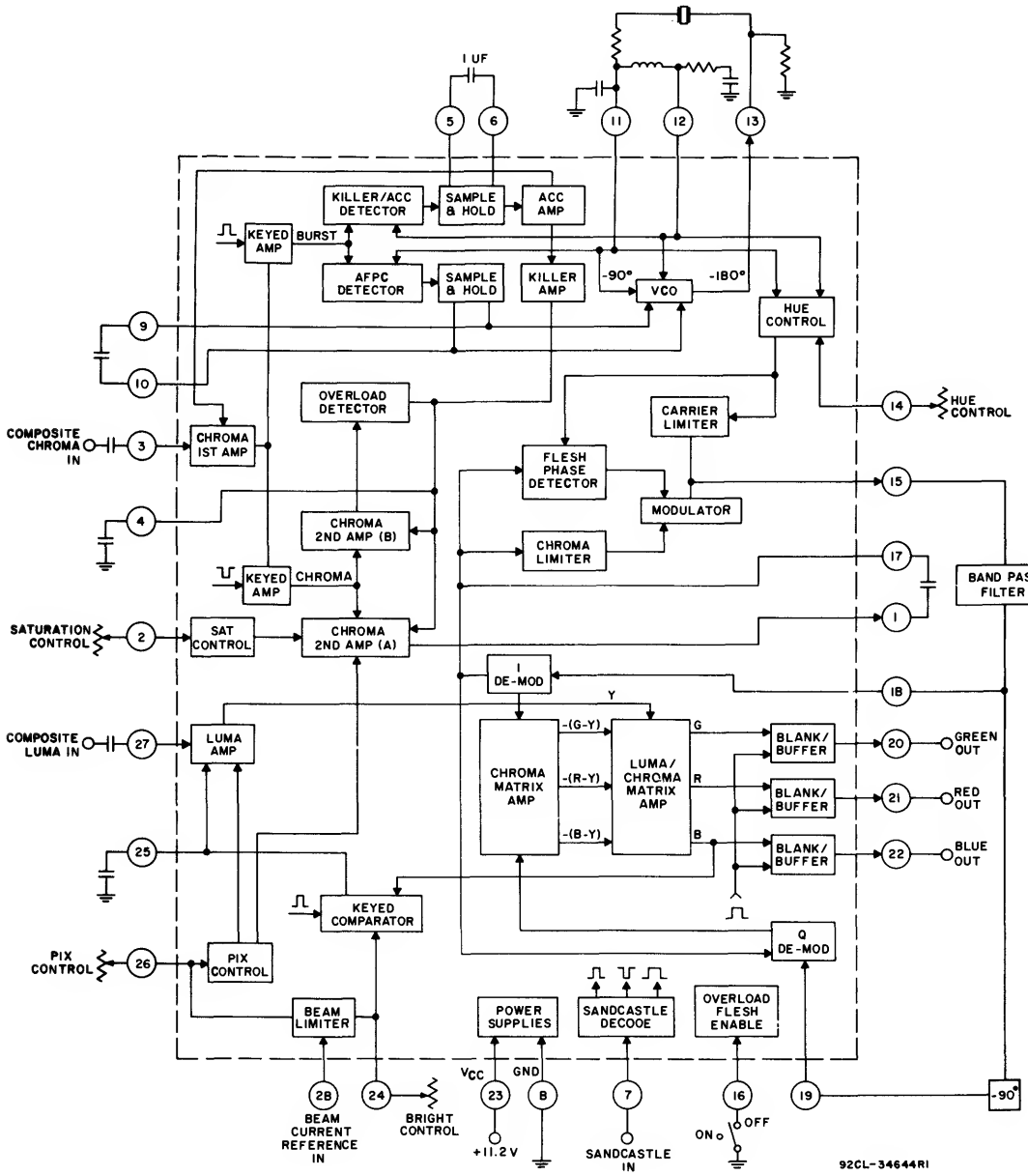


Fig. 1 - Block diagram of the RCA CA3217E chroma/luma integrated circuit.

Table I - Performance of the CA3217E Chroma/Luma Processor (Refer to Fig. 1)

Function	Typical Data		
IC Package	28-terminal DIP		
Chip Area	15,250 $(mil)^2$		
Approx. No. of IC Components	490		
Nominal Supply	11.2 V		
Nominal Dissipation	500 mW		
Oscillator Stability			
Supply Variation 10-14 V	5 Hz		
Variation with Temperature (ΔT=50° C)	25 Hz		
AFPC Characteristics			
DC Loop Gain	33 Hz/degree		
Pull-in Range	±500 Hz (±300-Hz Limit)		
ACC Characteristic			
100% Chroma Input Level	250 mV p-p		
3-dB Point	at 20% nominal input level		
Hue-Control Range	100°		
Saturation-Control Range	40 dB min.		
Demodulator Characteristics:		**Relative Amplitude**	**Angle**
R-Y		1	93°
B-Y		1.2	2°
G-Y		0.3	258°
Bandwidth (Chroma)	900 kHz		
Flesh Control	Restricted to signals in the +1 half-plane		
Chroma Overload Control	Two levels		
Picture Control	> 40 dB		
Brightness Control	Black level clamped on 3- to 5-V level		
Beam Limiting	On picture and brightness controls		
Luma Bandwidth	5 MHz min.		
Sandcastle Input			
1.2-2.3 V	Blanking		
> 3.3 V	Burst gate		
Maximum Linear Output			
R	5 V		
G	3 V		
B	3.7 V		

The burst-separated chrominance signal is applied to a second chroma amplifier, and the amplified signal is available on terminal 1. Four controls regulate the gain of this stage. A killer stage amplifies the detected and filtered burst signal, as explained above and, in presence of a burst signal, enables the second chroma amplifier. An R-C filter on terminal 4 stabilizes the killer action. A viewer-operated saturation control, connected to terminal 2, permits adjustment to a desirable saturation level. A picture control at terminal 26, also available to the viewer, operates on the luminance and second chroma amplifier and maintains a constant chrominance-to-luminance ratio. A two-level overload detector monitors the peak chrominance level and, in the presence of excessive chrominance or noise signals, reduces the gain of the second chroma amplifier to prevent oversaturation of the picture tube. Two modes of operation are possible and can be selected by the viewer by means of a switch on terminal 16. In one mode the detector reduces the gain of the second chroma amplifier in the presence of large noise peaks only; thus the operation of this stage remains essentially linear. In the second mode the average chrominance level is kept relatively constant to avoid the need for frequent adjustments of saturation control This problem arises when channels are being switched on during program changes, and results from variations in burst-to-chroma level.

The burst signal also serves to synchronize the subcarrier generator. A doubly balanced phase detector in the automatic frequency and phase control (AFPC) loop compares the instantaneous phase of the burst and subcarrier signals. The detected error gated by a sample-and-hold circuit and filtered by an external network on terminals 9 and 10 is applied to a voltage-controlled oscillator (VCO). Two orthogonal carrier signals are generated in this stage. The VCO output signal, on terminal

13, passes through a crystal filter and is applied to the VCO input terminal 11. The 90° phase-shifted component is obtained by means of an external phase-shift network connected to terminals 11, 12, and ground. The two orthogonal signals also provide reference signals for ACC and AFPC detectors and for the hue-control circuit.

In the hue circuit the two carriers are matrixed to generate a resultant signal oriented in the I phase direction. A dc control at terminal 14 allows a ±50° phase adjustment from the nominal position. A dynamic flesh-correction circuit, enabled by means of a switch on terminal 16, simplifies the hue adjustment and reduces the need for frequent adjustments of the hue control by the viewer. In this circuit a phase detector compares the phase of the chrominance signal with the I phase carrier generated in the hue circuit; the resulting signal controls the conduction of a modulator stage. This stage passes an amplitude-limited chrominance signal that is added to the original carrier from the hue circuit. The signal thus produced is a carrier that is phase modulated by the chrominance phase information, the modulation being restricted to chrominance signals in the +I half plane. This preserves the original colors in the -I half plane; the signals of the +I plane are shifted toward the +I axis.

The processed subcarrier is available on terminal 15, from which it is applied to terminal 18, the carrier terminal of the I demodulator. A 90° phase-shift network is employed to produce the correct carrier for the Q demodulator (terminal 19).

The I and Q demodulators decode the chrominance signal supplied externally from terminal 1 to 17. Demodulated I and Q signal components are matrixed and amplified to produce three color-difference signals.

The luminance signal, whose amplitude can be adjusted by a viewer-operated picture control (terminal 26), is applied to terminal 27. As previously described this control also operates on the second chroma amplifier to maintain a constant chrominance-to-luminance ratio regardless of the position of the control. Upon amplification the luminance and three color-difference signals are combined in three separate matrix stages to generate RGB signals. The output from the B stage is used to establish a black level for the video signal. A keyed comparator, activated during the horizontal burst keying interval, compares the back-porch synchronization signal level with an externally applied dc reference; the resulting signal, filtered at terminal 25, corrects the dc level of the RGB outputs. Thus the external bias reference, connected to terminal 24, establishes the picture black level and is used by the viewer as a brightness control.

The picture and brightness controls are regulated by a beam-limiter servo loop. A signal, developed from the average beam current, is applied to terminal 28; as soon as it exceeds a predetermined threshold level, a beam-limiter circuit reduces the peak-to-peak video signal. The control of this signal continues until the video signal is reduced to one half of its maximum level and subsequently reduces the brightness. An overlap between the picture and brightness control regions secures a smooth transition of controls.

Horizontal and vertical blanking pulses gate the RGB outputs to eliminate spurious signals during retrace from the picture tube. The gating is applied in the signal path between the chroma/luma matrix and the RGB output stages.

An externally generated sandcastle signal is applied to terminal 7 to provide timing for burst keying and blanking.

THE CHROMINANCE SECTION

The chrominance section of the RCA CA3217E chroma/luma IC provides all the functions and features available in RCA's CA3151 "one-chip chroma" IC. The CA3151 has been employed in RCA TV receivers for the past several years; its established performance was duplicated in the RCA CA3217E.

In the chrominance section three major sections can be identified: subcarrier regeneration, chrominance processing, and chrominance decoding. These are described below.

Subcarrier Regeneration

A detailed block diagram of the subcarrier regeneration is shown in Fig. 2. The burst signal separated from the

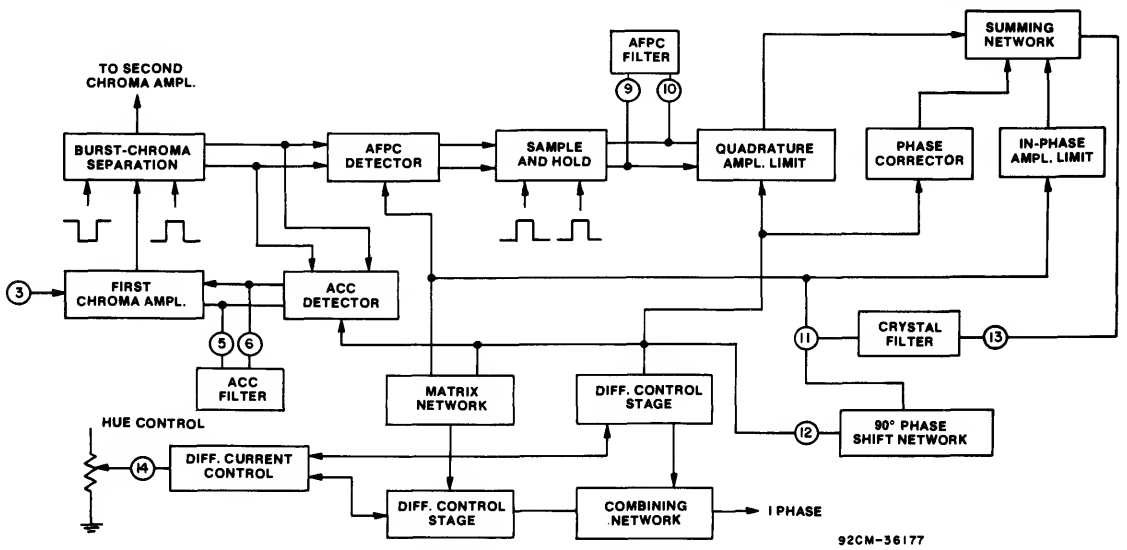


Fig. 2 - Subcarrier regeneration.

composite chrominance signal is applied to a doubly balanced detector, and the detected output is sampled during the burst keying interval and stored in filter capacitors at terminals 9 and 10. During the hold interval the switching arrangement disconnects the storage filter capacitors from the detector signal path, thereby increasing the efficiency of burst detection. The balanced switching assures good immunity to common-mode errors such as leakage or beta-dependent base current drains. The detected and filtered burst signal synchronizes a voltage-controlled oscillator (VCO).

VCO—The VCO consists of an in-phase amplifier, quadrature amplifier, phase corrector, summing network, externally connected crystal filter (between terminals 11 and 13), and a 90° phase-shift network connected between terminals 11 and 12. The in-phase amplifier, in conjunction with the external crystal filter, generates a 3,579,545-Hz cw signal. This signal, phase-shifted by 90°, passes through the quadrature amplifier and combines in the summing network with the signal generated by the in-phase amplifier. The quadrature amplifier, in response to the detected signal in the AFPC detector, controls the amplitude and polarity of the quadrature signal so as to synchronize the operation of the VCO with the burst signal. Parasitic capacitance associated with both amplifiers causes an undesired phase shift of approximately 20°, forcing the VCO to operate off design center. To compensate for this phase shift, a fraction of the quadrature carrier signal is bypassed through the phase corrector to the combining network, thus assuring a symmetrical operation of the VCO.

The two orthogonal carrier signals are also employed to generate an I phase reference signal, required for the operation of the I demodulator. To achieve this the signals are constructed according to the vector diagram in Fig. 3.

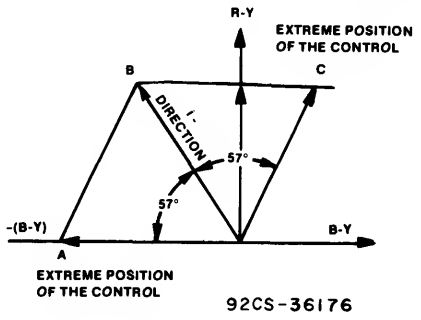


Fig. 3 - Hue-control signal components.

Referring again to Fig. 2, the burst-oriented carrier passes through a control stage to produce a burst-oriented signal A (Fig. 3). A matrix network combines the burst- and the (R-Y)-oriented carriers to produce a signal C. Signals A and C are symmetrically disposed with respect to the I signal (B vector). A customer-operated hue control allows a continuous phase adjustment from the extreme A to the extreme C signal direction by adding appropriate fractions of both signals. Circuit diagrams of the VCO and the hue control are shown in Figs. 4 and 5, respectively.

In the VCO, the in-phase amplifier limiter consists of transistors Q90 and Q91 and current source Q87, while the quadrature amplifier limiter is formed by devices Q80 to Q85 and current source Q79. The in-phase signal component generated by the oscillation of the in-phase amplifier in conjunction with the external crystal filter and the

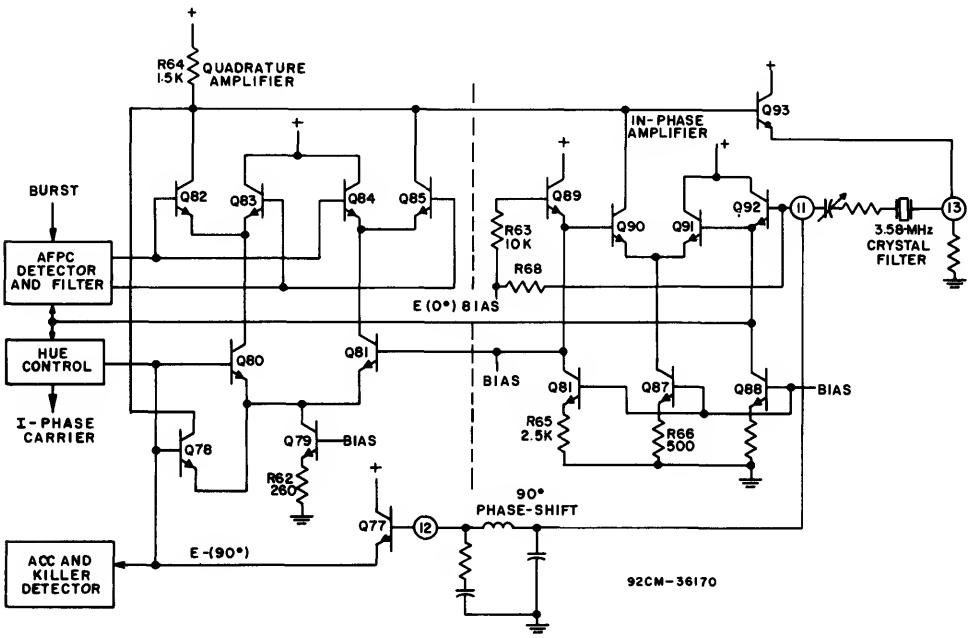


Fig. 4 - Voltage-controlled oscillator circuit.

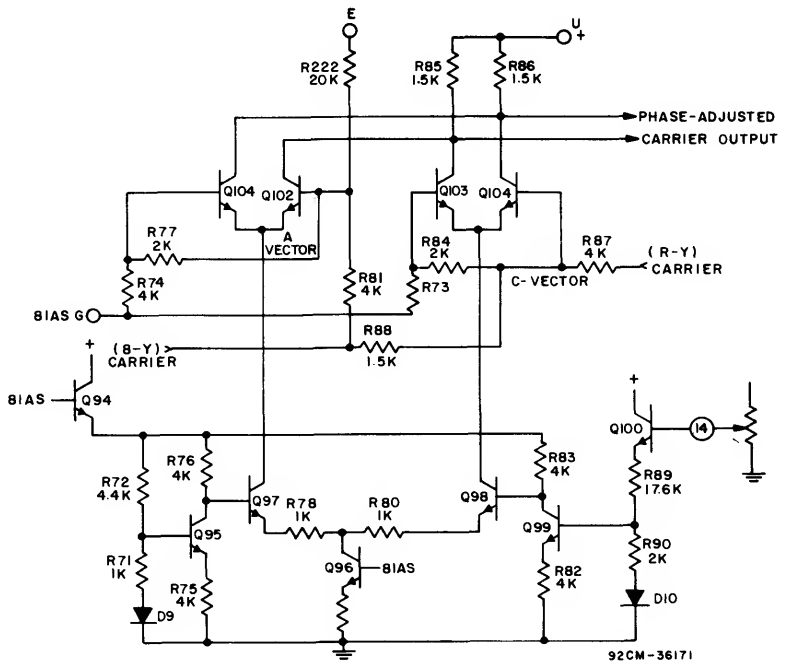


Fig. 5 - Hue-control circuit.

quadrature component produced by the external L-C phase shift network combine in the load resistor R64. The quadrature signal component, after passing through devices Q80 and Q81 is controlled by transistors Q82 to Q85. Depending on the output of the AFPC detector, the amplitude and polarity of the quadrature signal are adjusted by control transistors Q82 to Q85 so as to synchronize the VCO-generated signal to the frequency and phase of the color burst.

The previously explained phase delay, resulting from parasitic capacitances in the in-phase and quadrature amplifiers, is compensated by a signal arriving at the load resistor via transistor Q78. The emitter size of the transistor in relation to emitters of transistors Q80 and Q81 is adjusted to pass a fraction of the quadrature signal required for compensation of the delay in the other signal paths.

Hue Control—In the hue-control circuit the bias potential on terminal 14 (set by the viewer) determines the phase of the carrier signal developed across load resistors R85 and R86. The circuit is constructed to produce an I-oriented carrier with terminal 14 at one half of the V_{CC} supply, and equal (approx. 57°) phase shifts with terminal 14 at V_{CC} or ground potential. To achieve this, the following design requirements must be fulfilled:

1. With terminal 14 at one half V_{CC} potential, transistors Q97 and Q98 should conduct equal currents. This condition is satisfied by making resistors R78 and R80 equal and by setting equal voltage drops across resistors R76 and R83. Resistors R82 through R89 are so dimensioned that with terminal 14 at V_{CC} potential, the entire current from transistor Q96 passes through transistor Q97; with terminal 14 grounded, Q97 is cut off and the current passes through Q98.
2. Carrier signal -(B-Y) is adjusted to a nominal level at bases of transistors Q101 and Q102 by means of resistors R74, R77, and R81 to produce reference signal A (Fig. 3). Carrier (R-Y), adjusted by means of resistors R73, R84, and R87, and a fraction of -(B-Y) carrier matrixed with the (R-Y) carrier by means of resistor R88, produce reference carrier C. The amplitude of A and C signals are adjusted to produce a resultant I signal with terminal 14 set to one half of V_{CC} potential. The described circuit arrangement gives the viewer a reasonably linear and symmetrical hue-control circuit.

Chrominance Processing

This section describes the operation of the chroma amplifiers, the overload detector, and the dynamic flesh-correction circuit.

Two chrominance amplifiers control the amplitude of the color signal. The first amplifier is controlled by the ACC servo loop and maintains a substantially constant burst level at its output. This amplifier is gated by horizontal keying pulses that separate the burst and chrominance information. The separated burst signal is applied to the AFPC detector to synchronize the VCO, and to the ACC detector to control the gain of the first chrominance amplifier and to produce a signal for the killer amplifier. In the absence of color information, and for burst signals not exceeding a predetermined level, the killer amplifier disables the second stage.

The second amplifier, driven by the chrominance signal separated from the burst signal in the first stage, is gain controlled by three separate inputs: a viewer-operated picture control to adjust the luminance and chrominance, a manual saturation control that provides gain reduction with a greater than 40-dB range, and a dual-threshold overload detector.

The chrominance amplifiers and the overload detector are shown in Fig. 6. The composite chrominance signal amplified in the first chroma stage is applied to the bases of differential chroma amplifier Q20,Q21 and to those of

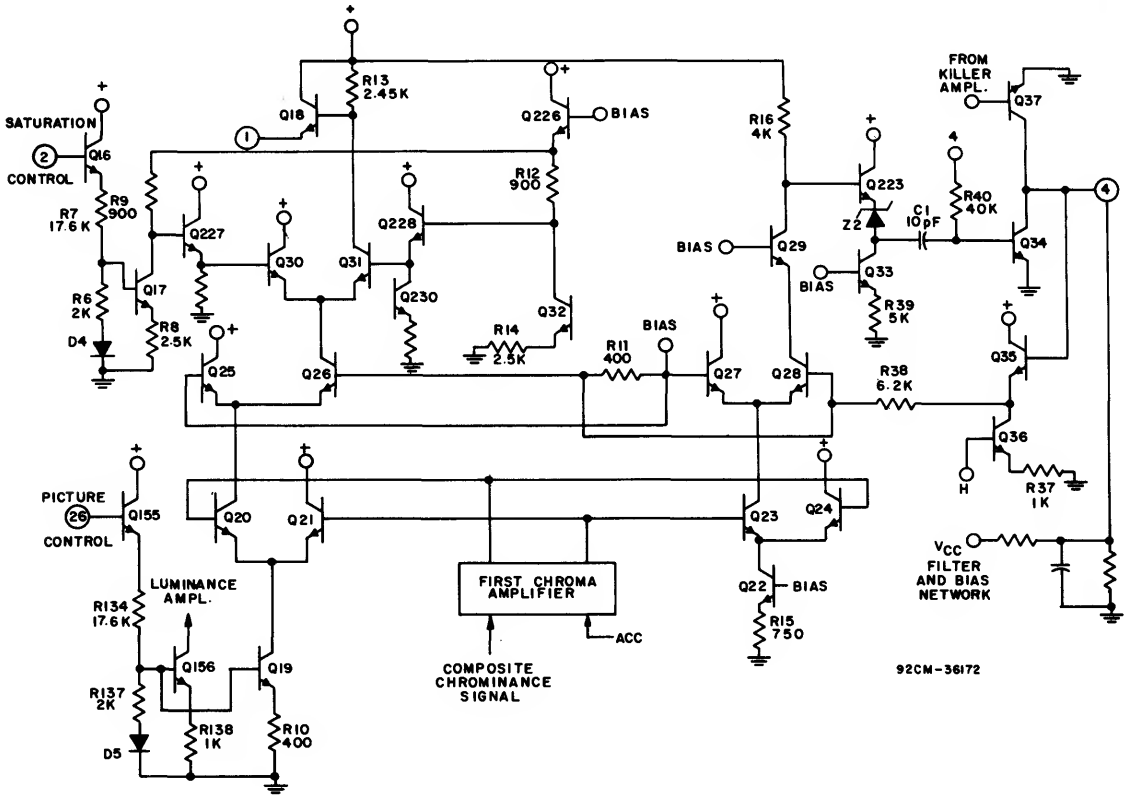


Fig. 6 - Second chrominance amplifier and overload detector.

differential overload amplifier Q23,Q24. The gain of stage Q20,Q21 is determined by the bias potential applied to terminal 26. This bias, set by a viewer-operated "picture control," determines the current in current sources Q156 and Q19. As shown in the diagram, current source Q19 controls the gain of the second chroma amplifier while current source Q156 determines the gain of the luma amplifier. Thus excellent tracking of both signals is maintained by the two current sources, operated in parallel. The chrominance signal developed in stage Q20,Q21 proceeds to stage Q25,Q26; the signal split between transistors Q25 and Q26 is determined by the control voltage developed in the overload detector. In this circuit section the chrominance signal amplified in stage Q23,Q24 proceeds through components Q28, Q29, Q223, Z2, and C1 to the internally prebiased two-level overload detector transistor Q34. An external bias network connected to terminal 4 sets the operating point for transistor Q35.

The filtered control signal proceeds through transistor Q35 and resistors R38 and R11 to control signal division in transistors Q27 and Q28 in the overload detector servo loop and also in the chroma amplifier by controlling bias potentials on bases of transistors Q25 and Q26. A manually adjustable saturation control, on terminal 2, operates on transistor pair Q30,Q31. The chrominance signal from transistor Q26 proceeds through Q31 and Q18 to the output terminal 1 to be coupled to demodulator stages.

A dynamic flesh-correction circuit modulates the instantaneous phase of the carrier in response to the phase of the incoming chroma signal. This signal processing is intended to reduce objectionable phase errors without frequent adjustments at the hue control.

The operation of the dynamic flesh-correction circuit is illustrated in Fig. 7. In the diagram the chrominance signal

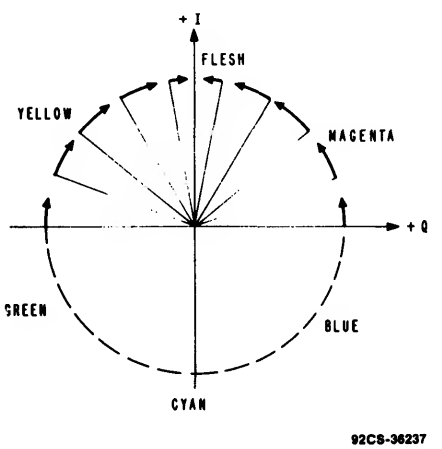


Fig. 7 - Chrominance signal modification by the dynamic flesh corrector.

is phase shifted toward the +I direction; actually, however, it is the phase of the subcarrier that is altered. The action of the dynamic flesh-correction circuit can be summarized as follows:

1. The phase of the subcarrier remains unchanged in the presence of a +I phase-oriented chrominance signal and also in the presence of chrominance signals having -I signal components.
2. In the presence of chrominance signals containing +I signal components, the original phase angle between the chrominance and the +I reference carrier is reduced. This phase shift is largest for chrominance signals corresponding to purple and yellow-green, and the shift is toward flesh colors. Primary colors such as red, blue, and green remain essentially unaffected by the action of the flesh-correction circuit.

Chrominance Decoding

Two doubly balanced demodulators are employed to generate I and Q signals. Demodulation along these axes simplified the design of the dynamic flesh correction. The demodulated signals are matrixed to generate color-difference signals suitable for combining with the luminance signal. In a dc-coupled system, such as the one employed in CA3217E, the predictability of the potentials at the output stages is important when the kine driver and the picture tube are being driven directly. Undesired voltage offsets may result from excessive gain and multiplicity of coupled stages. The matrix circuit in the CA3217E is designed to introduce a minimum of offset errors. As shown in Fig. 8, complementary I signals are applied to bases of transistors Q217 and Q225, while complementary Q signals are fed to bases of Q238 and Q237. Appropriate fractions of the signal (developed by means of resistor-dividers R223, R224, R225, R226, and R227) and fractions of the Q signal (developed by dividers R230 through R233) are combined in differential stages (Q241,Q242, Q143,Q144, and Q153,Q154) to produce the (B-Y), (G-Y), and (R-Y) signals, respectively. Since equal dc potentials exist on bases of transistors Q219 and Q225 and also in transistors Q228 and Q237, errors in the resistance values of the above described dividers may affect the accuracy of demodulated signals; however, they will not introduce any dc error.

Three color-difference signals, after filtering, are combined with the luminance signals in three separate amplifiers to produce RGB signals.

VIDEO SECTION

The video section shown in Fig. 9 consists of a luminance amplifier with viewer-operated gain (picture control), a summing amplifier that combines luminance and color-difference signals to produce RGB outputs, horizontal and vertical retrace blanking, and a blanking-level clamp with associated black-level control. The latter serves as brightness control. The picture control provides proportional adjustment of gain of both the chroma and luma channels. Retrace blanking operates on RBG signals to remove undesired or spurious signals from the luma and chroma channels. The gated black-level clamp compares the video signal during the burst-gate keying interval with an ex-

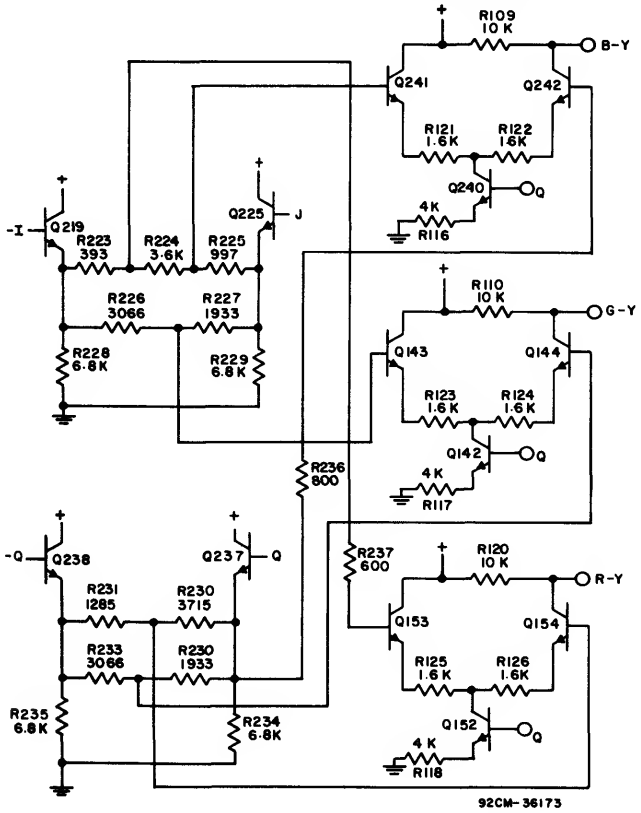


Fig. 8 - Color-difference matrix of the CA3217E.

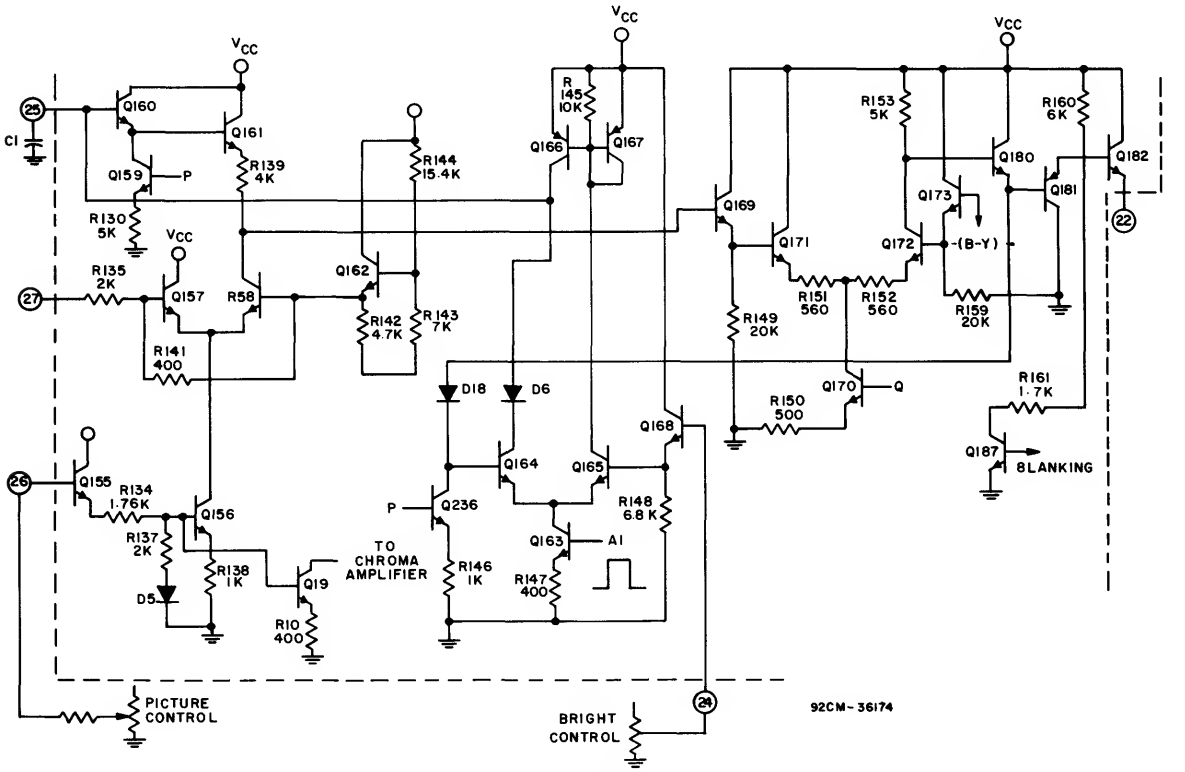


Fig. 9 - Video section (summing amplifier and blanking).

ternally adjustable reference potential, and maintains this level as a reference during the scan interval. This adjustment serves as the brightness control.

Luminance Processing

The luminance signal coupled through terminal 27 proceeds through resistor R135 to differential stage Q157,Q158. The gain of this stage is set by the potential on terminal 26. This potential is translated through Q151, R134, R137, and D5, and establishes the bias on the bases of Q156 and Q19. Current sources Q156 and Q19 determine the gain of the luminance and chrominance amplifiers, respectively, and thereby achieve excellent tracking. The luminance signal developed across R5 is applied to the summing amplifier.

Summing Amplifier and Blanking

In the summing amplifier the luminance signal proceeds through Q169, Q171, and the -(B-Y) color-difference signal through Q173 and Q172 to produce a resultant B signal across resistor R153. The B signal proceeds through devices Q180, Q181, and Q182 to terminal 22.

Horizontal and vertical retrace blanking is applied at the base of transistor Q182, and the blanking level is determined by the ratio of resistors R160 and R161. (Transistor Q187 is saturated during blanking.) Similar summing and blanking circuitry is employed for the red and green signals.

Black-Level Clamp

A gated servo loop maintains the black level at a preset potential as explained below:

The blue video signal at emitter of Q180 and an externally set reference potential at terminal 24 are compared during the gating interval in the comparator Q164,Q165. A storage capacitor C1 on terminal 25 is charged or discharged by devices Q164 and Q166 during a sampling interval to maintain the bases of Q164 and Q165 at approximately the same level. The dc potential established on terminal 25 during this sample interval is translated through Q160, Q161, and R139 to Q169 to maintain the black level of the video signal at a level consistent with the setting of the brightness control. The green and red output potentials are also controlled by the same control loop. The output of Q6 is coupled to all three summing amplifiers. The green and red amplifiers are arranged to match the blue amplifier; hence the potential of black level of all three output signals are essentially equal.

BEAM LIMITER

The beam-limiter circuit prevents the kinescope average electron-beam current from exceeding a predetermined level. Because the limiting action distorts the video information to be displayed, it is important to minimize the perceptibility of the distortion.

The beam-limiter characteristic is shown in Fig. 10, and the circuit in Fig. 11. The onset of limiting occurs in region 1 as the voltage on pin 28 decreases in response to excessive beam current. In region 1 the picture control voltage at pin 26 is lowered. This results in a corresponding decrease in picture amplitude (contrast). As explained above, the gain of both the luminance and chrominance channels decreases proportionately while the clamp maintains picture black level at the potential of the brightness control (pin 24). Further decrease in the voltage on pin 28 causes limiting to occur in region 2. Here limiting action at the picture control

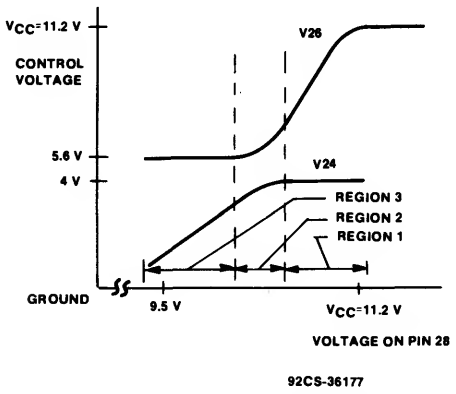


Fig. 10 - Beam-limiter characteristic.

decreases; at the same time brightness-control limiting action begins. This corresponds to a decrease in picture black level. Still lower voltages at pin 28, corresponding to strong limiting, cause operation in region 3 where the brightness-control voltage is lowered and essentially no action occurs at the picture control.

Most limiting takes place in region 1. Picture limiting was chosen because the viewer is relatively insensitive to changes in picture level (i.e., contrast). To avoid low-contrast ("washed out") pictures, the limiter can reduce gain only to one half of maximum. When strong limiting is needed, a smooth transition to brightness limiting is made.

As beam current increases further, the voltage across R171 increases to 0.7 V, and Q231 conducts. This is the beginning of region 3. The voltage at pin 26 is now clamped to 5.6. This is the half-gain point of the picture control. However, Q187 collector current continues to increase as I beam increases. This is mirrored to the brightness control. Near the start of region 3 the voltage across R172 reaches 0.7 V, and D17 conducts. R172 is effectively removed from the circuit; the current transfer ratio of this mirror increases to R179,R178.

The voltage gain from pin 28 to pin 26 can be externally adjusted by the Thevenin equivalent resistance of the picture circuit. Likewise, the gain from pin 28 to pin 24 can be adjusted by the brightness-circuit equivalent resistance. Hence loop-gain characteristics can be tailored to each receiver.

SANDCASTLE DECODER

The composite sandcastle signal and decoding circuitry is shown in Fig. 12.

The two-level signal is coupled through transistor Q231 to transistors Q187, Q188, Q189, and Q194. The first level produces blanking signals for the RGB output stages. Transistors Q187, Q188, and Q189 saturate whenever the sandcastle exceeds approximately 1.4 V.

The second level of sandcastle produces complementary horizontal burst-gate keying pulses at emitters Q195 and Q201 for the gating chroma circuits and the black-level clamp. Divider R171,R172 reduces the sandcastle level to maintain Q199 off during blanking interval; however, the second-level pulse is sufficiently large (> 2.3 V) to saturate Q199. This produces a negative pulse on the emitter of Q195. Transistor Q200, normally saturated, is cut off by this pulse, and a positive pulse appears on the emitter of Q201. A voltage divider (R179,R178) couples this pulse to the black-level clamp.

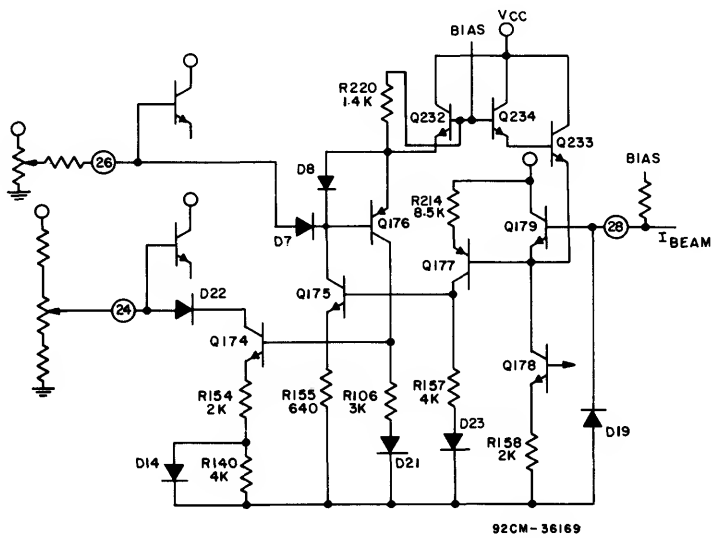


Fig. 11 - Beam-limiter circuit.

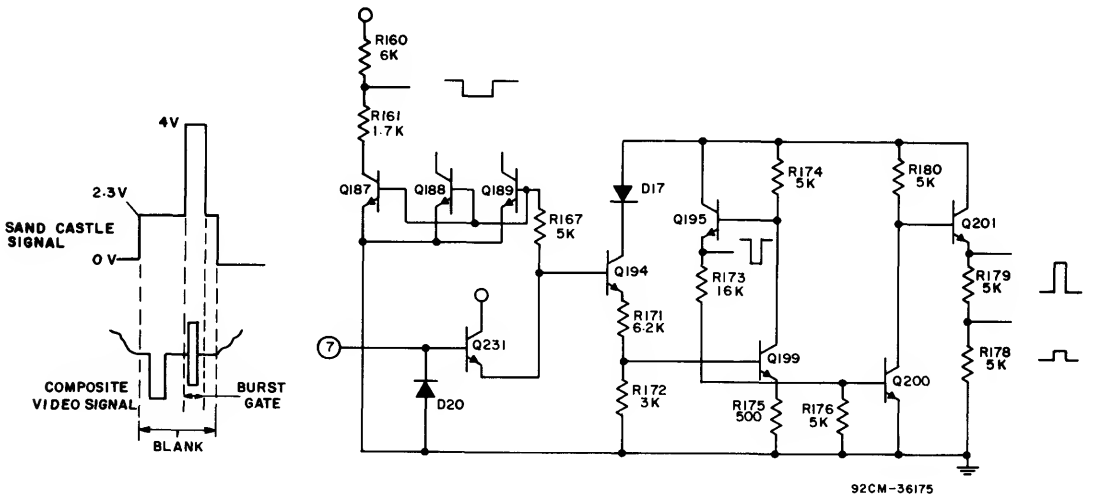


Fig. 12 - Sandcastle decoder.

SUMMARY

The CA3217E chroma/luma IC provides a complete subsystem for a color TV receiver. The composite video signal from the second detector is processed to provide RGB signals to the picture tube drivers. All customer-operated controls such as the picture control, saturation control, hue control, and brightness control are accessible at respective IC terminals. Several automatic servo loops are employed to stabilize the operation of the circuits and to reduce the need for frequent adjustments. The servo loops are the AFPC, ACC, dynamic flesh control, two-level overload control, beam limiting, and gated black-level control.

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